

MINIMIZING LEAKAGE POWER IN DUAL-THRESHOLD CMOS CIRCUITS USING INTEGER LINEAR PROGRAMMING

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ABSTRACT: This paper presents a novel technique, which uses integer linear programming (ILP) to significantly reduce the leakage power without sacrificing circuit performance. For each gate in the design library low and high threshold versions are characterized for leakage in various input states using Spice simulation. An ILP model first finds the shortest critical path delay corresponding to all low-threshold gates. A second ILP model then minimizes the total leakage power by optimally placing high-threshold devices for a user-specified critical path delay. The constraint set sizes for both ILP models are linear in the circuit size. Experimental results show a 96% reduction of leakage power with no delay increase for the benchmark circuit C7522 implemented in the 70nm BPTM CMOS technology. Some other ISCAS'85 benchmarks had lower power savings, but when a 25% increase in the critical path delay was allowed all had at least 90% leakage reduction. Using an example, we outline a possible extension of the dual-threshold method to simultaneously minimize the leakage power and the dynamic glitch power, which is under investigation.