

VLSI Power Estimation & Dual-Transition Glitch Filtering in Probabilistic Simulation

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Outline

- Introduction
 - Levels of power estimation techniques
- Gate-level Probabilistic Approach
 - Signal Probability
 - Transition probability
 - Transition density
 - Probability waveform
- Dual-transition glitch filtering
 - Idea and examples
 - Detailed algorithm
 - Experimental results
- Summary



Introduction

- Power estimation is critical to IC (low power) design
 - Total power consumption must be estimated during the design phase.
 - Helps identifying hot-spot on the chip, useful for thermal design
- Levels of power estimation
 - Transistor Level
 - Gate Level
 - RTL Level
 - Behavior Level
 - Software Level
- Two approaches
 - Simulation based
 - Non-simulative



Simulation based approach

- Transistor Level Simulation
 - Circuit level
 - SPICE
 - Solving a large matrix of node current using KCL
 - Components - Resistor, capacitor, inductors, current sources and voltage sources.
 - Diodes and transistors are modeled by basic components
 - PowerMill
 - Table based device model
 - Event driven timing simulation
 - 2-3 orders of magnitude faster than Spice



Simulation based approach

- Switch level
 - Transistor as a on-off switch with a resistor
 - Short circuit power - observing the time in which the switches form a power-ground path
- Gate Level Simulation
 - Components - logic gates
 - Logic simulation to find switching activity,
 $P = 1/2CV^2f_{\text{active}}$
 - Monte Carlo simulation, statistical method
 - Each sample has N Random input vector
 - Energy consumption has a normal distribution
 - Stopping criterion derived from sample average and sample standard deviation



Simulation based approach

- RTL level simulation
 - Components - register, adder, multiplier, etc.
 - Macro-modeling of each component based on simulation
 - Simulating the component with random input
 - Fitting a multi-variable regression curve (power macro model equation) using a least mean square error fit.
 - RT-level simulation collect input statistics of each module



High level estimation

- Behavior level estimation
 - No much information about gate level structure of design component
 - Information theoretic models
 - Average switching activity for each line is approximated by $\frac{1}{2}$ its entropy
 - Total capacitance estimated based on output entropy
 - Complexity based models, “equivalent gate”
- Software level estimation
 - Energy consumption by a application program
 - Instruction level power macro-modeling
 - Profile-driven program synthesis with RT level simulation



Non-simulative approach

- Gate level probabilistic approach
 - Concepts
 - Signal Probability
 - Transition probability
 - Transition density
 - Probability waveform
 - Factors in building up a model
 - Spatial, temporal correlation
 - Zero delay or real delay (glitch power)
 - With or w/o glitch filtering



Gate level probabilistic approach - concepts

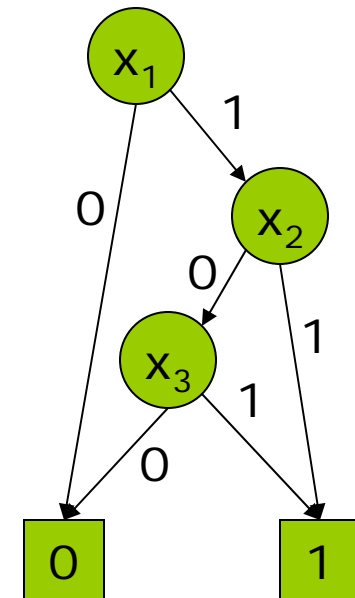
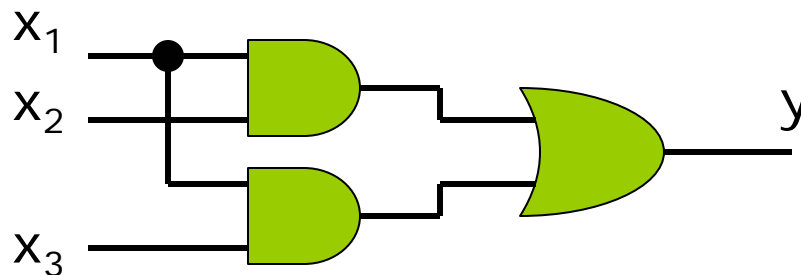
○ Signal Probability

- $P_s(x)$, the fraction of clock cycles in which the steady-state value of signal x is high
- Spatial independence, the logic value of an input node is independent of the logic value of other input nodes
- Under spatial independence
 - Inverter: $c=a$, $P_s(c)=1-P_s(a)$
 - AND gate: $c=ab$, $P_s(c)=P_s(a)P_s(b)$
 - OR gate: $c=a+b$, $P_s(c)=1-[1-P_s(a)][(1-P_s(b))]$
- Signal correlation
 - S. Ercolani, etc. Estimate of signal probability in combinational logic networks. In Proc. the First European Test Conference, 1989, 132–138.
 - $P_s(x_1, x_2) = P_s(x_1)P_s(x_2)W_{x_1, x_2}$

Signal probability with spatial correlation

- Global OBDD

- Ordered binary decision diagram corresponding to the global function of a node (function of node in terms of circuit input)
- Give exact signal correlation
- Example, function $y = x_1x_2 + x_1x_3$



- $$P_s(y) = P_s(x_1)P_s(f_{x_1}) + P_s(\overline{x_1})P_s(f_{\overline{x_1}})$$

- Traversal from bottom to top to derive signal probability



Gate level probabilistic approach - concepts

- Transition probability
 - $P_t(x)$, average fraction of clock cycles in which the steady state value of x is different from its initial value
 - Temporal independence, the signal value of a node at current clock cycle is independent to its signal value at previous clock cycles
 - Under temporal independence assumption
 - $P_t(x) = 2P_s(x)[1 - P_s(x)]$
 - Transition correlation
 - R. Marculescu, etc. Logic level power estimation considering spatiotemporal correlations. In *Proc. ICCAD*, Nov. 1994, 294–299.
 - Zero delay assumption, lag one markov chain
 - $TC_{xy}(ij, mn) = P(x_{i \rightarrow j}, y_{m \rightarrow n}) / P(x_{i \rightarrow j})P(y_{m \rightarrow n})$ where $i, j, m, n \in \{0, 1\}$



Gate level probabilistic approach - concepts

- Transition density

- F. N. Najm, Transition density: a new measure of activity in digital circuits. *IEEE Trans. on CAD*, 12, 2 (Feb. 1993), 310–323.
- $D(x)$, average number of transitions a logic signal x makes in a unit time (one clock cycle)
- Boolean difference, if y is a function depending on x then

$$\frac{\partial y}{\partial x} = y|_{x=1} \oplus y|_{x=0}$$

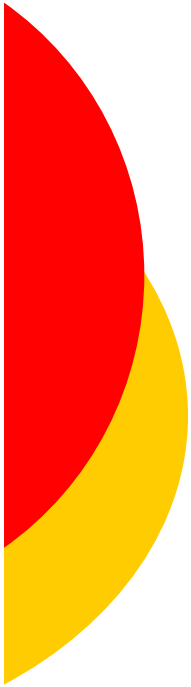
and
$$D(y) = \sum_{i=1}^n P\left(\frac{\partial y}{\partial x_i}\right) D(x_i)$$

- Assume no two signal transit simultaneously.
- Assume spatial independence
- Glitch power included w/o glitch filtering effect



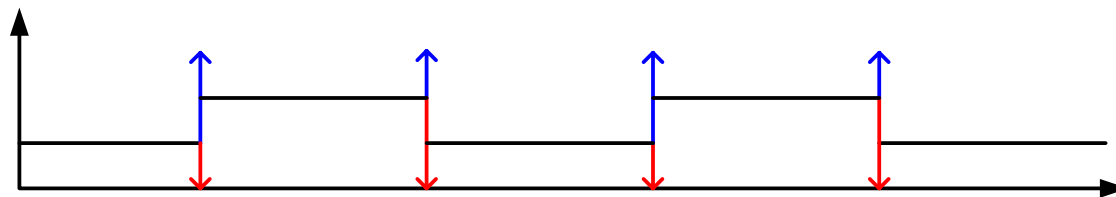
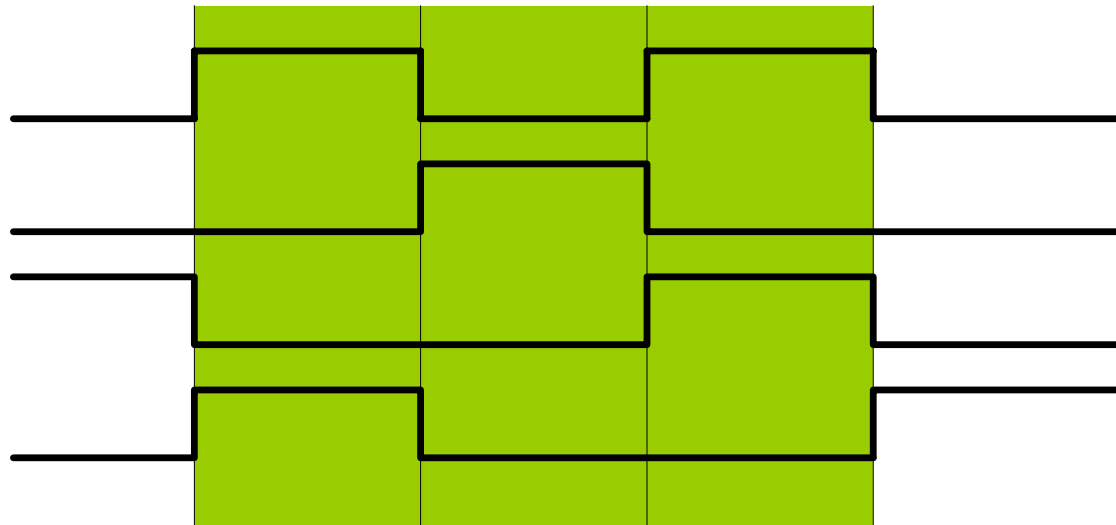
Gate level probabilistic approach - concepts

- Probabilistic simulation
 - F. N. Najm, etc. CREST - a current estimator for CMOS circuits. In *Proc. ICCAD*, Nov. 1988, 204–207.
 - **Probability waveform**, a sequence of signal probability and transition probability over signal transition interval
 - Real delay model, spatial independence
 - Transition density, sum of transition probabilities
 - Our refined definitions
 - **Signal probability** $sp_n(t)$, probability of node n having logic 1 at time t
 - **Transition probability** $P_n^s(t)$, probability that node n has a logic transition state s ($s \in \{00, 01, 10, 11\}$) at time t
 - Properties: $sp_n(t-) = P_n^{10}(t) + P_n^{11}(t)$, $sp_n(t+) = P_n^{01}(t) + P_n^{11}(t)$



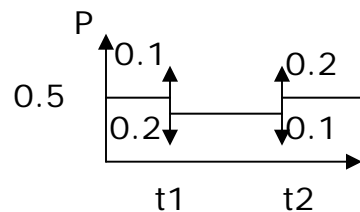
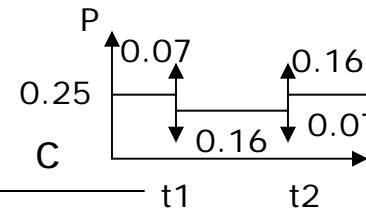
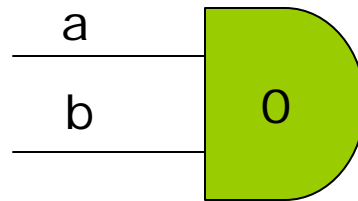
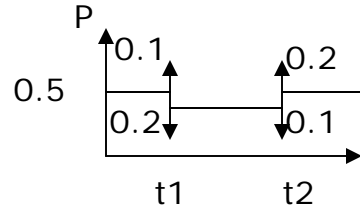
Probability waveform

- An example



Probability waveform propagation

○ AND gate, $c=ab$



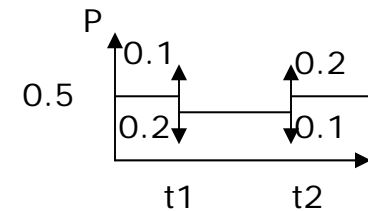
$$\begin{aligned}
 P_c^{01}(t_1) &= P_a^{01}(t_1)P_b^{01}(t_1) + \\
 &P_a^{01}(t_1)P_b^{11}(t_1) + P_a^{11}(t_1)P_b^{01}(t_1) \\
 &= 0.1 \times 0.1 + 0.1 \times 0.3 + 0.3 \times 0.1 \\
 &= 0.07
 \end{aligned}$$

$$\begin{aligned}
 P_c^{10}(t_1) &= P_a^{10}(t_1)P_b^{10}(t_1) + \\
 &P_a^{10}(t_1)P_b^{11}(t_1) + P_a^{11}(t_1)P_b^{10}(t_1) \\
 &= 0.2 \times 0.2 + 0.2 \times 0.3 + 0.3 \times 0.2 \\
 &= 0.16
 \end{aligned}$$

$$P_c^{11}(t_1) = sp_c(t_1-) - P_c^{10}(t_1) = 0.25 - 0.16 = 0.09$$

$$sp_c(t_1+) = P_c^{01}(t_1) + P_c^{11}(t_1) = 0.07 + 0.09 = 0.16$$

Probability waveform

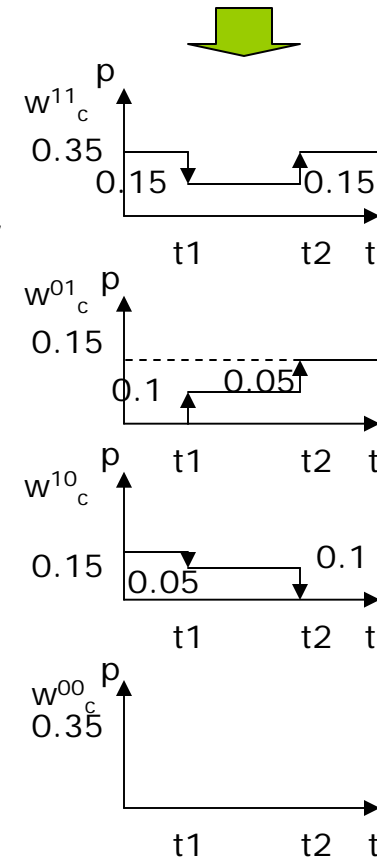


o Tagged Probabilistic Simulation

- C.-S. Ding, et al. Gate-level power estimation using tagged probabilistic simulation. *IEEE Trans. on CAD*, 17, 11, (Nov. 1998), 1099–1107.
- Partition of probability waveform according to the steady state signal values, w_{n}^{00} , w_{n}^{01} , w_{n}^{10} , w_{n}^{11}
- Approximate exact spatial correlations with the macroscopic spatial correlations between steady state signal values (tags)

$$\omega_{a,b}^{xy,wz} = \frac{P(w_a^{xy} \wedge w_b^{wz})}{P(w_a^{xy})P(w_b^{wz})}$$

- Glitch filtering effect attempted





Tagged probability waveform

- Definitions

- **Signal probability**, $sp^{xy}_n(t)$, probability of node n having logic 1 at time t on waveform w^{xy}_n . $x, y \in \{0, 1\}$
- **Transition probability**, $P^{s}_{n,xy}(t)$, probability that node n has a logic transition state s ($s \in \{00, 01, 10, 11\}$) at time t on waveform w^{xy}_n

- Propagation of waveform

- Similar to untagged waveform
 - Two input gates, 16 joint tagged waveform combined to 4 output waveform
- For an two inputs AND gate, $c=ab$

$$P^{01}_{c,(xy,wz)}(t+d) = (P^{01}_{a,xy}(t)P^{11}_{b,wz}(t) + P^{01}_{a,xy}(t)P^{01}_{b,wz}(t) + P^{11}_{a,xy}(t)P^{01}_{b,wz}(t))\omega_{a,b}^{xy,wz}$$

$$P^{10}_{c,(xy,wz)}(t+d) = (P^{10}_{a,xy}(t)P^{11}_{b,wz}(t) + P^{10}_{a,xy}(t)P^{10}_{b,wz}(t) + P^{11}_{a,xy}(t)P^{10}_{b,wz}(t))\omega_{a,b}^{xy,wz}$$

where $x, y, w, z \in \{0, 1\}$



New glitch filtering method

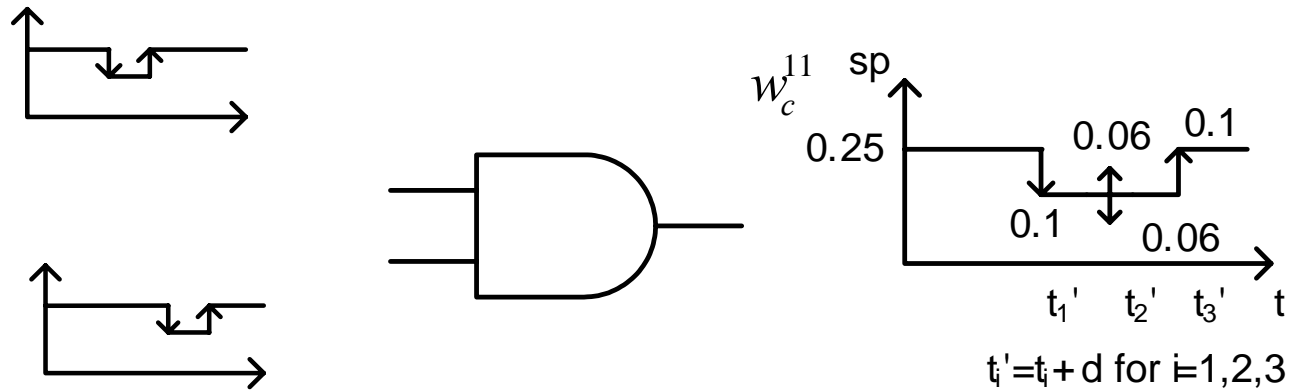
- Original glitch filtering scheme in TPS
 - If pulse width less than gate inertial delay d , it is subject to glitch filtering
 - Example, two input AND gate for time $t1$

for all $t2$, where $t2-t1 < d$

$$P_{c,(xy,wz)}^{01}(t1+d) = P_{a,xy}^{01}(t1) P_{b,wz}^{10}(t2) \omega_{a,b}^{xy,wz}$$
$$P_{c,(xy,wz)}^{10}(t2+d) = P_{a,xy}^{01}(t1) P_{b,wz}^{10}(t2) \omega_{a,b}^{xy,wz}$$

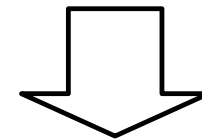
- Limitations
 - Imprecise, not an accurate description of glitch
 - Can't filter glitch coming from single input

Original glitch filtering in TPS

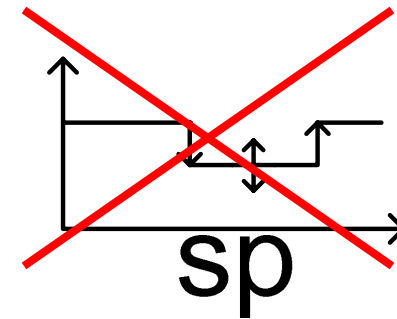
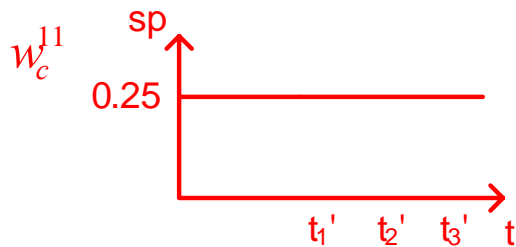


$$t_1 < t_2 < t_3 < t_1 + d$$

TPS Glitch filtering

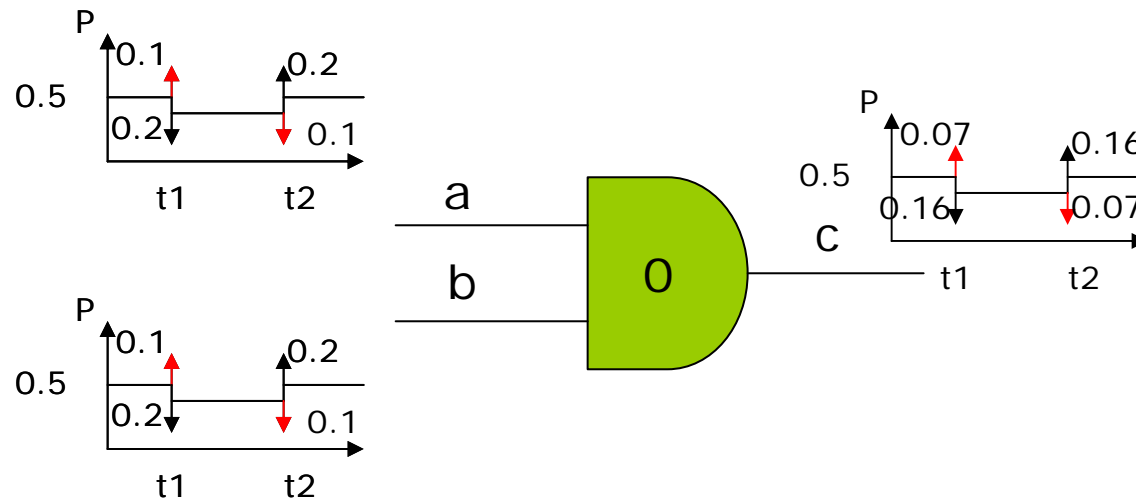


Actual waveform



New glitch filtering method

- Dual-transition probability
 - Find the exact condition for a pulse, knowing that each signal has 4 possible state at t_1, t_2
 - In probability waveform



- $P^{01,10}_c(t_1, t_2) = P\{c \text{ is } 0 \rightarrow 1 \text{ at } t_1 \text{ and } 1 \rightarrow 0 \text{ at } t_2\}$
 $= P\{(a, b) \text{ at } t_1 \text{ is } (01, 11) \text{ or } (11, 01) \text{ or } (01, 01) \text{ and } (a, b) \text{ at } t_2 \text{ is } (10, 11) \text{ or } (11, 10) \text{ or } (10, 10)\}$

Dual-transition probability

a	01	11	01
b	11	01	01

and

a	10	11	10
b	11	10	10

t1

t2



a	01,10	01,11	01,10	11,10	11,11	11,10	01,10	01,11	01,10
b	11,11	11,10	11,10	01,11	01,10	01,10	01,11	01,10	01,10

t1, t2

- $P^{01,10}_c(t1,t2)$ is a sum of 9 product terms
 - Example term: $P^{01,10}_a(t1,t2)P^{11,11}_b(t1,t2)$

Dual-transition probability

- In TPS, use macroscopic spatial correlations to approximate spatial correlations

$$P_{c,(xy,wz)}^{01,10}(t_1 + d, t_2 + d) = \sum_{i=1}^3 \sum_{j=1}^3 P_{a,xy}^{sa1_i,sa2_j}(t_1, t_2) P_{b,wz}^{sb1_i,sb2_j}(t_1, t_2) \omega_{a,b}^{xy,wz}$$

$$(sa1_i, sb1_i) \in \{(01,11), (11,01), (01,01)\}$$

a	01	11	01
b	11	01	01

t1

$$(sa2_j, sb2_j) \in \{(10,11), (11,10), (10,10)\}$$

a	10	11	10
b	11	10	10

t2

$$x, y, w, z \in \{0,1\}$$



New glitch filtering method

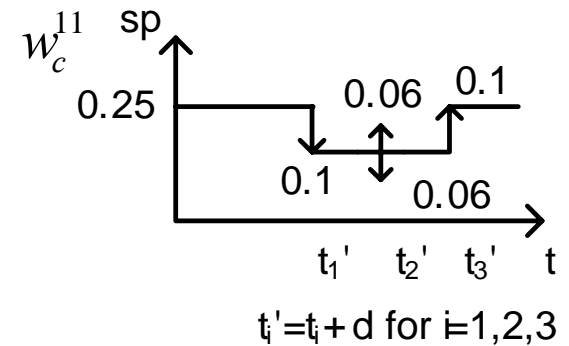
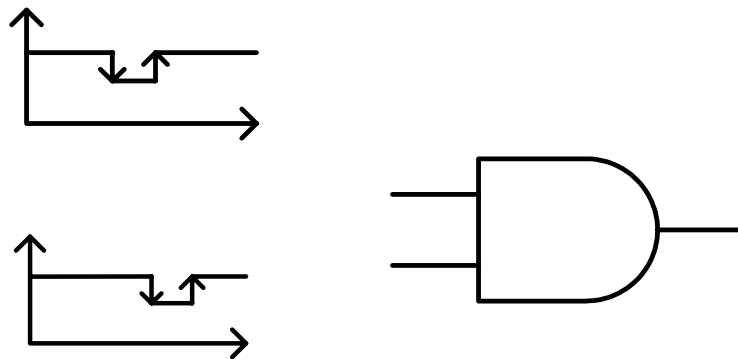
- Dual-transition glitch filtering
 - If pulse width less than gate inertial delay d , it is subject to glitch filtering
 - For a two input AND gate for time $t1$

for all $t2$, where $t2-t1 < d$

$$P_{c,(xy,wz)}^{01}(t1) = P_{c,(xy,wz)}^{01,10}(t1,t2)$$
$$P_{c,(xy,wz)}^{10}(t2) = P_{c,(xy,wz)}^{01,10}(t1,t2)$$

$$P_{c,(xy,wz)}^{10}(t1) = P_{c,(xy,wz)}^{10,01}(t1,t2)$$
$$P_{c,(xy,wz)}^{01}(t2) = P_{c,(xy,wz)}^{10,01}(t1,t2)$$

Dual-transition glitch filtering

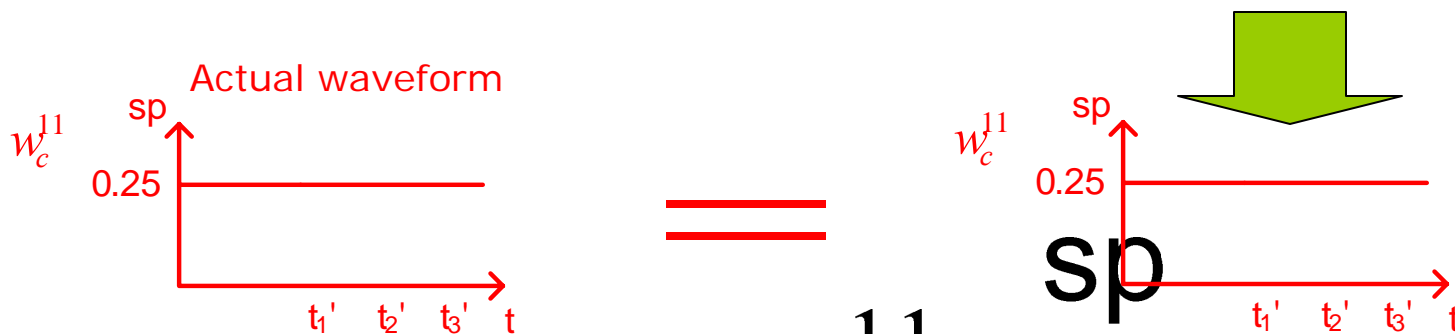


$$t_1 < t_2 < t_3 < t_1 + d$$

$$P_{c,11}^{10,01}(t_1', t_2') = 0.2 * 0.3 + 0... + 0 = 0.06$$

$$P_{c,11}^{10,01}(t_2', t_3') = 0.2 * 0.3 + 0... + 0 = 0.06$$

$$P_{c,11}^{10,01}(t_1', t_3') = 0.2 * 0.2 + 0... + 0 = 0.04$$



w_a^{11} 0.5

0.2

0.2



Dual-transition probability propagation

- Dual-transition probability

- Propagated from primary inputs towards output
- General equation

$$P_{c,(xy,wz)}^{sc1,sc2}(t_1 + d, t_2 + d) = \sum_{i=1}^k \sum_{j=1}^l P_{a,xy}^{sa1_i,sa2_j}(t_1, t_2) P_{b,wz}^{sb1_i,sb2_j}(t_1, t_2) \omega_{a,b}^{xy,wz}$$

- For primary inputs, transition only occur at time 0

- $P_{n,xy}^{sn1,sn2}(0, t) = P_{n,xy}^{sn1}(0)$ if $sn1, sn2$ is a valid sequence of state,

- e.g. $P_{n,xy}^{01,11}(0, t) = P_{n,xy}^{01}(0)$

- Otherwise, $P_{n,xy}^{sn1,sn2}(0, t) = 0$



Update dual-transition probability

- No two transition can occur within gate delay d after the filtering
- Dual-transition correlation coefficient

$$\omega_{n,xy}^{sn1,sn2}(t_1,t_2) = \frac{P_{n,xy}^{sn1,sn2}(t_1,t_2)}{P_{n,xy}^{sn1}(t_1)P_{n,xy}^{sn2}(t_2)}$$

- After the filtering
 - If $t_2 - t_1 < d$,
 - $P_{n,xy}^{01,10}(t_1,t_2), P_{n,xy}^{10,01}(t_1,t_2)$ set to 0
 - $P_{n,xy}^{01,11}(t_1,t_2)$ set to $P_{n,xy}^{01}(t_1)$
 - Otherwise
 - Update $P_{n,xy}^{sn1,sn2}(t_1,t_2) = P_{n,xy}^{sn1}(t_1)P_{n,xy}^{sn2}(t_2)\omega_{n,xy}^{sn1,sn2}(t_1,t_2)$

where $P_{n,xy}^{sn1}(t_1), P_{n,xy}^{sn2}(t_2)$ are transition probability after the filtering



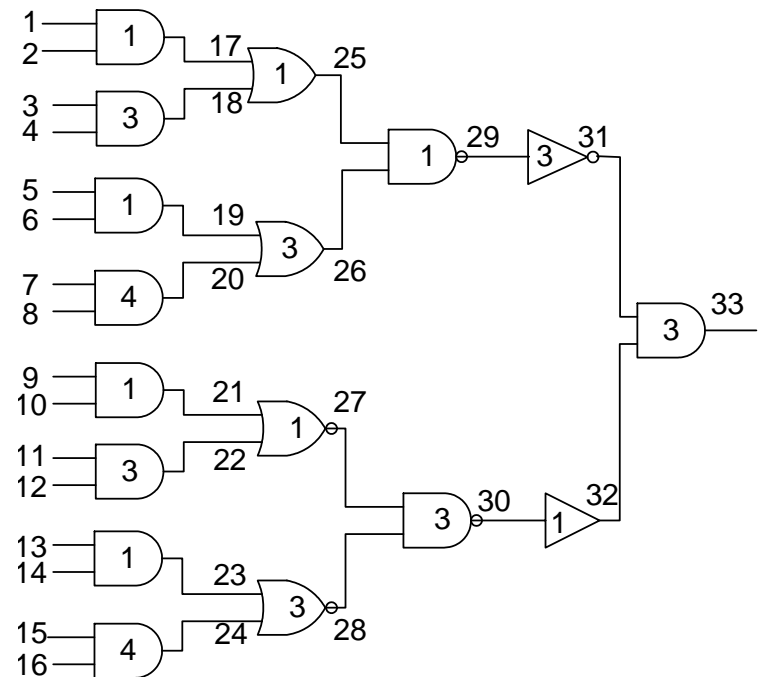
Experimental results

- Dual-transition glitch filtering is implemented in both probabilistic simulation and TPS
 - ProSim+DT
 - TPS+DT
- Stand alone software implemented in C++
 - Input - circuit netlist, signal probabilities
 - Output – power (transition density) for each node and the total power
- Results compared to event driven logic simulation
 - Assuming spatial and temporal independence for primary inputs
 - 40,000 randomly generated vectors
- Steady state signal probability and macroscopic correlations are obtained from a zero delay simulator

Experimental results

○ Small tree structure circuit

- No spatial correlations
- Arbitrarily specified delay
- Input signal probability = 0.5
- $P_{switching}$, switching power in terms of transition density D_x

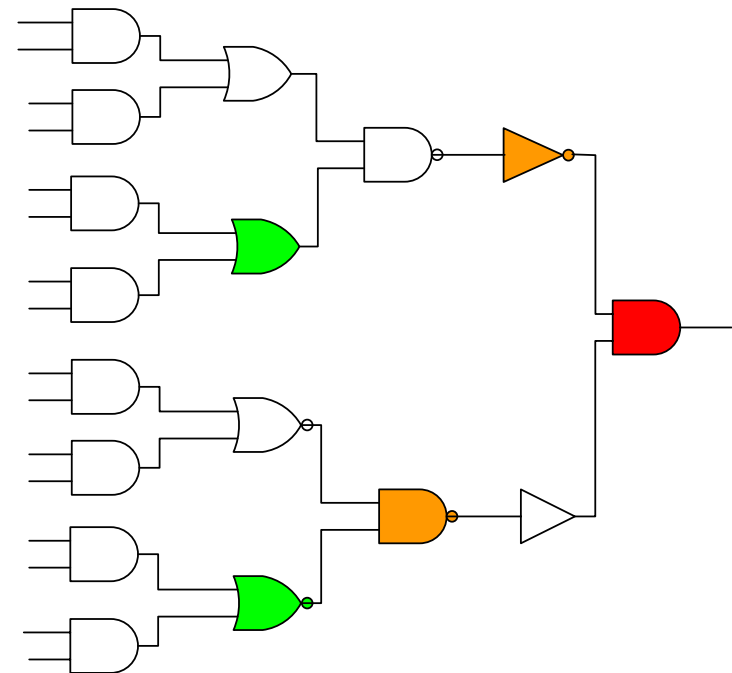


Experimental results – tree circuit

Nd	Logic Sim.	ProSim		ProSim+DT		TPS		TPS+DT	
	$P_{switch}(D_x)$	$P_{switch}(D_x)$	Err. (%)	$P_{switch}(D_x)$	Err. (%)	$P_{switch}(D_x)$	Err. (%)	$P_{switch}(D_x)$	Err. (%)
26	0.491	0.563	14.6	0.492	0.3	0.492	0.3	0.492	0.3
27	0.564	0.563	0.2	0.563	0.2	0.564	0.1	0.564	0.1
28	0.489	0.563	15.0	0.492	0.6	0.493	0.7	0.493	0.7
29	0.434	0.453	4.4	0.432	0.4	0.434	0.0	0.434	0.0
30	0.450	0.593	31.8	0.455	1.0	0.483	7.2	0.453	0.6
31	0.351	0.453	29.1	0.339	3.2	0.434	23.8	0.346	1.2
32	0.450	0.593	31.8	0.455	1.0	0.483	7.2	0.453	0.6
33	0.263	0.375	42.4	0.256	2.8	0.306	16.4	0.263	0.2

Experimental results – tree circuit

- Observations
 - ProSim gives large error because it neglects glitch filtering at nodes 26,28,30,31
 - Original TPS gives large error at node 30, 31 because of inaccurate glitch filtering
 - For tree structure circuit, ProSim+DT and TPS+DT has similar accuracy because there is no spatial correlations





Experimental results – benchmark circuits

- ISCAS 85' benchmark circuits
- Input signal probability 0.5
- Gate delay is proportional to number of fanouts
- Error statistics
 - E_{avg} , average node error, percentage error with respect to average node power obtained from logic simulation
 - σ , standard deviation of node errors
 - E_{tot} , percentage error of total power
- Results from ProSim+DT, TPS, TPS+DT are compared with logic simulation results

Experimental results – benchmark circuits

Circuits	ProSim+DT			TPS			TPS+DT		
	E_{avg} (%)	σ (%)	E_{tot} (%)	E_{avg} (%)	σ (%)	E_{tot} (%)	E_{avg} (%)	σ (%)	E_{tot} (%)
c17	5.8	7.8	0.7	2.3	2.6	0.1	2.3	2.6	0.1
c432	14.7	17.3	8.5	29.9	38.8	35.8	9.5	11.8	6.5
c499	6.2	11.6	6.6	6.8	14.0	7.0	3.6	8.2	0.6
c880	11.2	18.3	7.3	8.3	15.3	1.6	8.0	15.7	5.2
c1355	16.8	21.5	18.3	24.2	31.6	32.9	5.8	11.2	5.4
c1908	21.9	33.8	19.7	15.0	23.1	4.1	17.7	27.9	11.2
c2670	20.6	29.7	15.0	16.6	29.8	7.2	16.7	28.3	9.9
c3540	16.6	36.3	10.0	13.8	26.3	9.8	10.3	25.6	2.4
c5315	20.2	40.1	17.2	11.8	24.4	2.3	13.4	31.5	10.1
c6288	29.6	29.9	26.4	27.4	27.5	32.1	15.7	18.8	4.1
c7552	21.6	39.9	16.4	14.5	27.5	3.2	14.8	31.4	7.8
Avg.	16.6	25.6	13.1	15.6	23.7	12.0	10.7	18.8	5.7
Max.	29.6	40.1	26.4	29.9	38.8	35.8	17.7	31.5	11.2



Experimental results – benchmark circuits

○ Observations

- ProSim+DT gives large error because it neglects spatial correlations
- TPS+DT has up to 29% improvement on E_{tot}
 - c432, c1355, c6288 contains a large component of glitch power
 - Estimation accuracy is improved due to the new glitch filtering method
- TPS+DT gives a more consistent estimation in terms of average and maximum errors
- TPS+DT gives larger error for certain circuits
 - Estimation accuracy is jointly decided by TPS and DT
 - Effectiveness of DT is limited by the inherent errors in TPS



Experimental results – computation cost

- TPS+DT is 2-3 times faster than the logic simulation over all input vectors
- ProSim+DT is 20-30 times faster than the logic simulation
- Original TPS is 2 order of magnitude faster than logic simulation
- TPS+DT is much slower due to the propagation of dual-transition probabilities
- ProSim+DT is faster since it only has one probability waveform for each node
 - Idea for tree structure circuit where no spatial correlation exists



Summary

- Intro. to different Levels of power estimation
- Gate-level Probabilistic Approach
 - Signal Probability, Transition probability, Transition density
 - Probabilistic simulation, tagged probabilistic simulation
- A improved glitch filtering method
 - A new concept of dual-transition probability
 - Can be applied to both probabilistic simulation and Tagged probabilistic simulation
 - Enhanced TPS achieves a more accurate and consistent estimation, with up to 29% improvement on estimation accuracy
 - Accuracy and computation cost needs to be improved



Recent works

- Some more improvements on estimation accuracy is obtained

Circuits	TPS			TPS+DT			New method		
	E_{avg} (%)	σ (%)	E_{tot} (%)	E_{avg} (%)	σ (%)	E_{tot} (%)	E_{avg} (%)	σ (%)	E_{tot} (%)
c17	2.3	2.6	0.1	2.3	2.6	0.1	2.3	2.6	0.1
c432	29.9	38.8	35.8	9.5	11.8	6.5	11.5	16.6	11.5
c499	6.8	14.0	7.0	3.6	8.2	0.6	2.3	3.0	3.0
c880	8.3	15.3	1.6	8.0	15.7	5.2	4.8	9.0	0.0
c1355	24.2	31.6	32.9	5.8	11.2	5.4	5.0	9.5	0.5
c1908	15.0	23.1	4.1	17.7	27.9	11.2	7.0	16.3	2.0
c2670	16.6	29.8	7.2	16.7	28.3	9.9	13.2	23.6	6.2
c3540	13.8	26.3	9.8	10.3	25.6	2.4	10.5	26.4	3.7
c5315	11.8	24.4	2.3	13.4	31.5	10.1	11.3	27.0	3.4
c6288	27.4	27.5	32.1	15.7	18.8	4.1	12.7	15.4	0.2
c7552	14.5	27.5	3.2	14.8	31.4	7.8	14.1	27.6	1.3
Avg.	15.5	23.7	12.4	10.7	19.4	5.7	8.6	16.1	2.9



Questions ?

For questions and comments, please contact me at
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