

**Title:** VLSI Power Estimation & Dual-Transition Glitch Filtering in Probabilistic Simulation

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**Abstract:**

Power estimation methods are critical to IC designs since power consumptions for each module must meet the specification during the design phase in order to avoid a costly redesign process. We will first discuss briefly common power estimation methods on different level of VLSI design and then we will concentrate on gate level dynamic power estimation techniques. Gate level power estimation, the major power component is the switching power when signal transitions charge and discharge load capacitors. Although leakage power (due to sub-threshold leakage current of transistors) is becoming more and more significant as the device size keeps shrinking, an accurate estimation of switching power is always of great interests.

Switching power estimation at gate level normally has two approaches, simulation-based and probabilistic methods. The event-driven logic simulation can give the precise switching activity at each node. However, a large number of typical input vectors have to be simulated in order to get a meaningful average power. On the other hand, probabilistic methods only require one analysis to derive the power given input probabilities and are more preferred. Most of early probabilistic approaches for power estimation are under zero delay models, which mean only steady state signal values are analyzed. Premature signal transitions during the transient stage, so called glitches or hazards, are ignored in this model. Some of the later works tried to include the glitch power for a more accurate estimation. *Transition density* approach included glitch power into the total switching power assuming no two signals arrive at a gate at the exactly same time instance. Probabilistic simulation (CREST) and tagged probabilistic simulation (TPS) were proposed, where *probability waveforms* are used to model the signal activities, including glitch activities, statistically.

A major drawback for most of above techniques is that *glitch filtering effect* is not considered. Glitch filtering effect refers to the fact that glitches with pulse width less than the gate inertial delay will be "filtered" out by the gate. This effect can change the switching activities of gates dramatically; therefore, it can have a significant impact on the power dissipation of a circuit. No accurate glitch filtering method has been proposed so far in gate-level power estimation. Even in the tagged probabilistic simulation, where the modeling of glitch filtering has been attempted, the filtering effect is approximated aggressively.

We propose an accurate glitch filtering method in probabilistic simulation based on a new measure of dual-transition probability that captures the states of a node at two different time instance. Our technique can be applied to both probabilistic simulation (CREST) and tagged probabilistic simulation. Experimental results show our new method, when applied to the tagged probabilistic simulation, achieves a more accurate and consistent power estimation. For certain circuits with a large component of glitch power, up to 29% improvement on estimation accuracy is obtained.