

Enhanced Dual-Transition Probabilistic Power Estimation with Selective Supergate Analysis

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Abstract:

Consideration of pairs of transition in probabilistic simulation allows power estimation for digital circuits in which inertial delays can filter glitches [5]. However, the merit of the method is not fully realized because of the way probabilistic simulation approximates spatial correlations of signals in the presence of delays. In this paper, we use supergate partitions (enclosing reconvergent fanouts) and timed Boolean functions (TBF) to obtain the dual-transition probabilities that correctly deal with glitches and filtering as they affect power estimation. Experimental results on ISCAS'85 benchmarks show significant improvements in estimation accuracy as the average estimation error on total power consumption remains under 5%.