Built-In Self-Test for Regular Structure Embedded Cores in System-on-Chip

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Abstract:

Many of today's chips demand more embedded memory than ever before. SoCs and FPGAs are also moving from logic-dominant to memory-dominant chips. The addition of memory, while it creates a more powerful chip, increases die size and results in poor yield. As the percentage of embedded memory continues to increase, so does the chip's complexity, density, speed and of course, the probability of failures due to wafer defects. For SoCs to keep up their momentum and remain a viable option for improving system integration and performance, the problems relating to testing multiple high-density, multi-megabit memories must be solved.

Two BIST approaches are presented for testing embedded memories in SoCs and FPGAs. The first approach uses a portable HDL and focuses on reducing BIST development time. Similar approach can be used for testing other regular structure cores like adders, multipliers. The second approach focuses on using partial reconfiguration capability of the embedded microcontroller to reduce downloads between test configurations and hence reduce the total-test time significantly. Experimental results are presented from actual implementation of BIST approaches used to test memory cores in Atmel AT94K series SoCs, Virtex I, Virtex II and Spartan II FPGAs and Virtex II pro SoCs.