# Modifying Multi-Mode Scan to Handle Hard-to-Detect Faults and X-States in Sequential Circuits

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Date: Wednesday, March 8, 2005
Time: 3:00 pm
Room: Broun 235

**ABSTRACT:** This work is continuation of the work that Dr. Singh presented ("Multi-Mode Scan: Test-per-Clock BIST for IP Cores") last semester and I am taking it a little further and the circuits used for experiments are ITC'99 Benchmark circuits (Torino).