LOW COST ALTERNATE TESTING OF ANALOG/MIXED-SIGNAL/RF CIRCUITS AND SYSTEMS

Speaker: **Abhijit Chatterjee**, Professor , School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA
Date: Thursday, Feburary 17, 2005
Time: 3:00 pm
Room: Broun 238

ABSTRACT: As opposed to testing of digital circuits which has traditionally been "fault-driven", production testing of analog systems has continued to be specification-driven. This means that analog circuits continue to be tested against their original design specifications. As an example, production tests for an operational amplifier may include tests for slew rate, common-mode rejection ratio, etc. The key problems with specification-based testing of analog circuits are that the test procedures are very complicated and the time taken to measure all the test specification values is high because special test circuitry needs to be switched on and off to measure all the different test specification values. To solve this problem, the approach of alternate testing of analog circuits is proposed. In this approach, a short AC, DC or transient test stimulus is applied to the circuit-under-test and its response to the applied stimulus is characterized via "response feature extraction". The extracted response features are fed to a mapping module which generates all the desired test specification values from the observed response. Besides test time savings, "alternate test" provides a mechanism for testing multi-GHZ systems with limited test access. The state of the art in analog/RF testing will be first summarized and "burning" issues related to fault modeling and test generation will be discussed. Then alternate test techniques that alleviate some of the above test issues will be presented. The results of pilot studies from production deployment of the technology will be discussed.

Biographical Sketch: Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. He worked with the General Electric Corporate Research and Development Center in Schenectady, N.Y. from 1983 to 1992, taking leave to do his Ph.D from 1985-1989. Since 1993, he has been a faculty member of the School of Electrical and Computer Engineering at the Georgia Institute of Technology. Chatterjee's research interests are in the fields of computer algorithms, reliable design and test of analog and mixed-signal ICs/systems-on-packages/printed wiring boards and design of low-power ICs and systems. He received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received three Best Paper Awards and three Best Paper Award nominations. In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. Chatterjee has published over 185 papers in refereed journals and conferences, has 6 patents and serves on the program committees of several conferences and workshops. He served as Associate Editor of IEEE Design and Test of Computers from 1996 to 2001. Chatterjee is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as Chairman and Chief Scientist from 2002 – 2002. Chatterjee is currently directing research at Georgia Tech in mixed-signal design and test funded by DARPA, NSF, SRC, MARCO and industry.