Gate-Level Timing Analysis

Smith Chapter 13

Outline

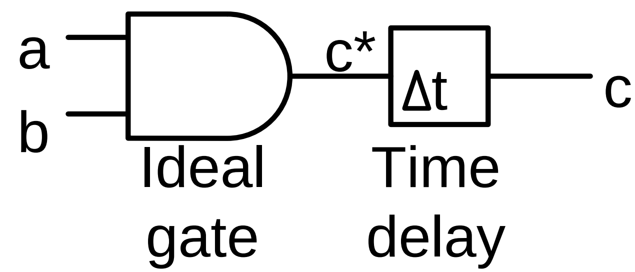
- Gate-delay models
- Circuit timing constraints
- After Synthesis:
  - VITAL models for gate-level simulation
  - VHDL netlist simulation with VITAL models and Standard Delay Format (SDF) files

Logic cell delay models

- "Delay" = time from the occurrence of an event until the occurrence time of a 2nd event caused by the first
  - depends on circuit structure & technology
  - may also depend on cell interconnects
  - model delays with different levels of detail/accuracy
  - may have a range of possible values (process/condition dependent)

Primitive device delay models

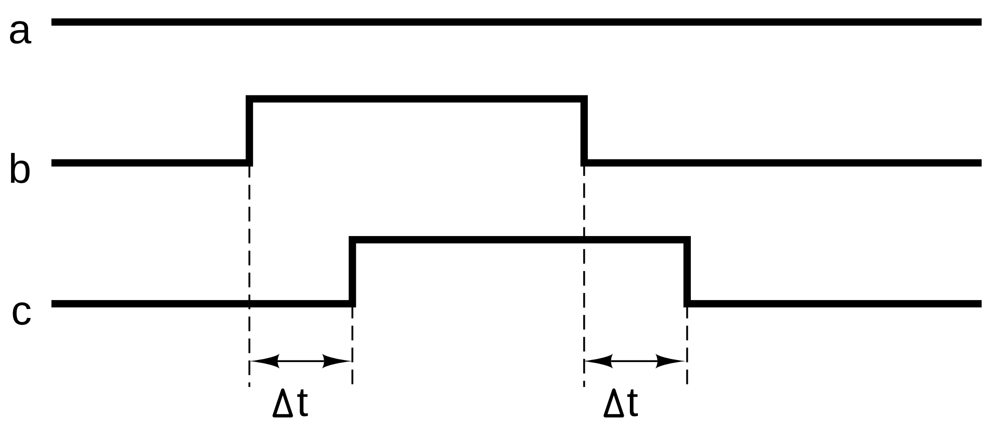
- A primitive logic gate has an intrinsic delay.
  - model as an ideal (zero-delay) gate and a "transport delay" element.
  - transport delay models:
    - unit/nominal delay
    - rise/fall delay
    - ambiguous or min/max delay



Unit/nominal delay

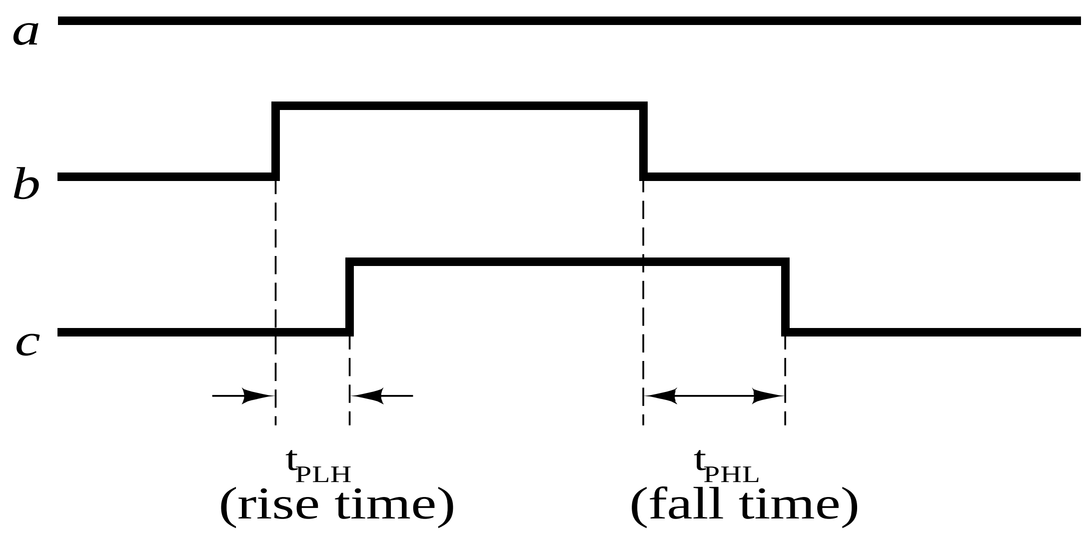
- Unit delay: each gate has delay of one "unit" of time.
- Nominal delay: delays determined separately for each type of gate

  (e.g., on time unit for NOR and two time units for XOR).



Rise/fall delay

- Delays for 0 to 1 and 1 to 0 transitions.
  - t_{PLH} (rise time): propagation delay for signal changing from low to high.
  - t_{PHL} (fall time): propagation delay from high to low.

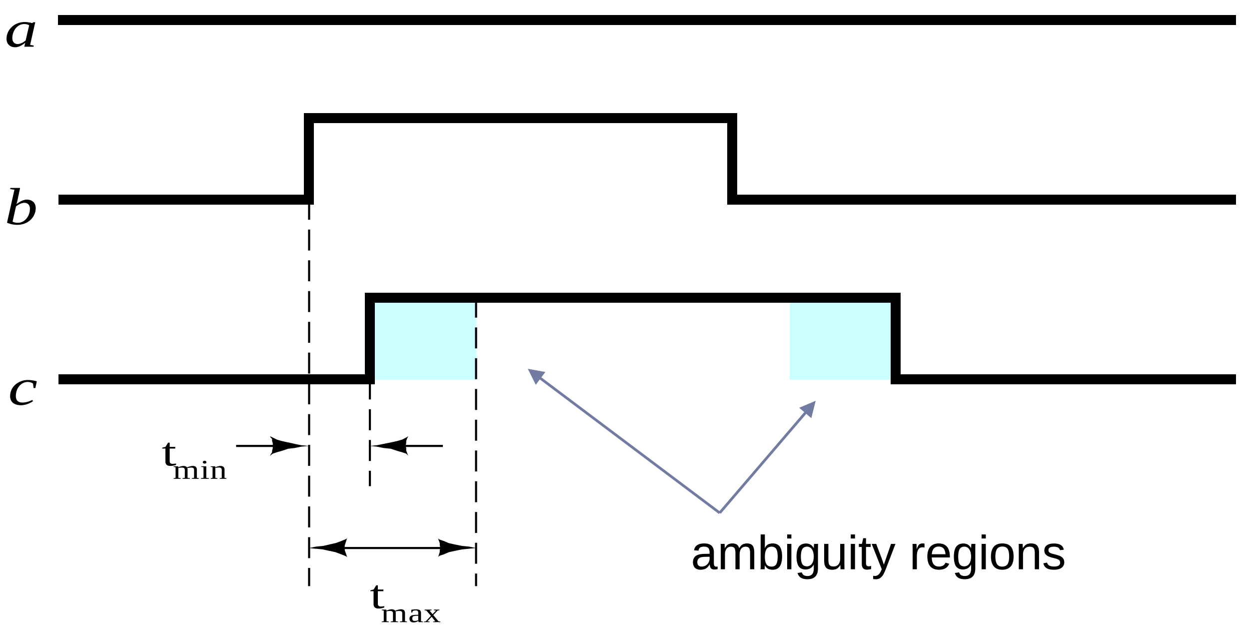


Example: ADK tsmc035 technology

- nand02 cell:
  - tP=0.537466 (ns) INV on A0(RI) to Y(FA)
  - tP=0.810693 (ns) INV on A0(FA) to Y(RI)
  - tP=0.421754 (ns) INV on A1(RI) to Y(FA)
  - tP=0.868593 (ns) INV on A1(FA) to Y(RI)
- and02 cell:
  - tP=0.726188 (ns) INV on A0(RI) to Y(FA)
  - tP=0.828392 (ns) INV on A0(FA) to Y(RI)
  - tP=0.679021 (ns) INV on A1(RI) to Y(FA)
  - tP=0.921874 (ns) INV on A1(FA) to Y(RI)

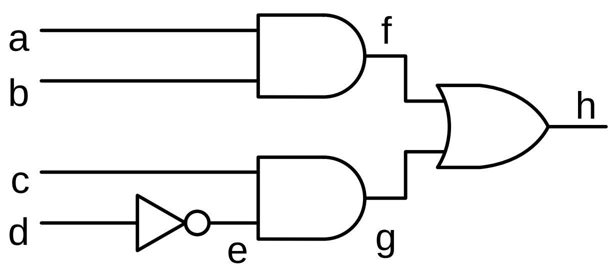
Ambiguous or Min/Max Delay

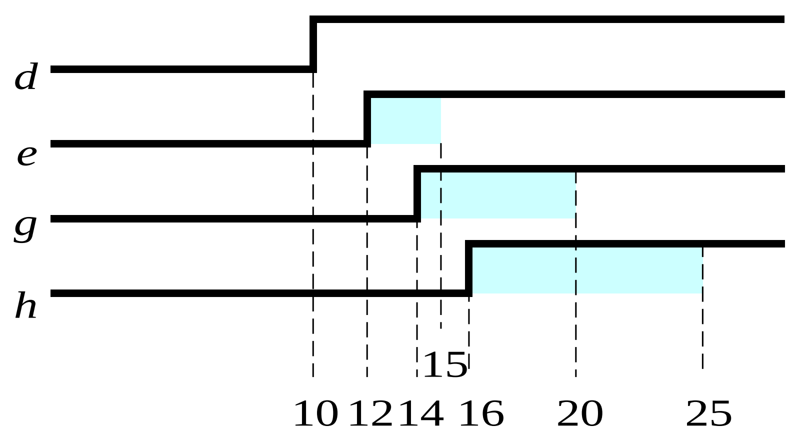
- Difficult to predict exact rise or fall time of a signal.
- For worst-case performance analysis, $\{t_{min}, t_{max}\}$ is specified for each timing parameter.



Accumulated min/max delays

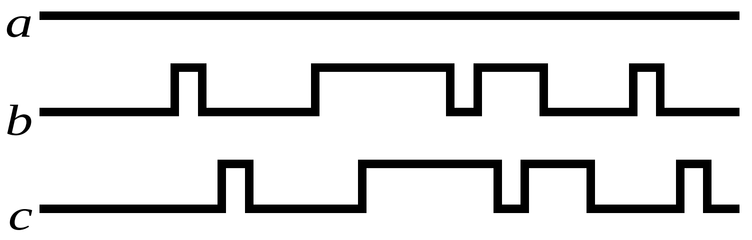
- Simulation producing min/max delay results tend to be pessimistic.
  - ambiguity region larger at each level



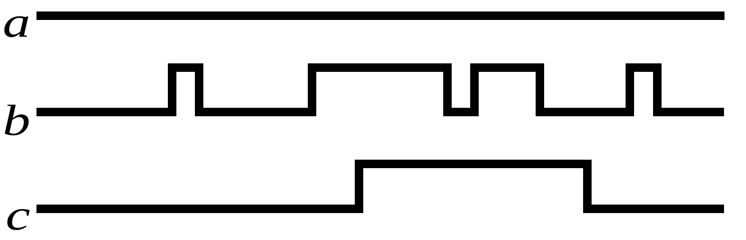


Inertial Delay

- An input value must persist for some minimum duration of time to provide the output with the needed inertia to change.
  - The minimum duration is called *inertial delay*.

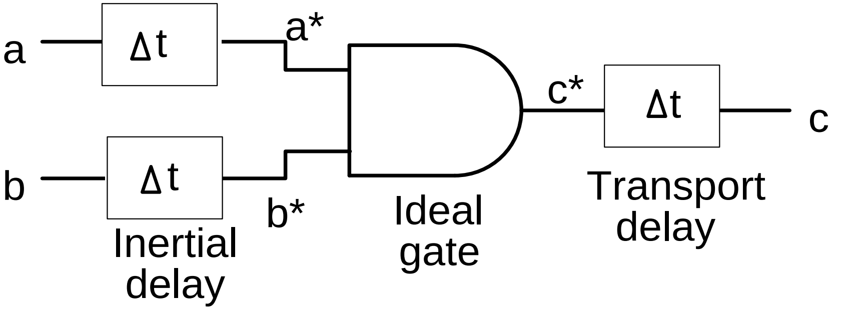


(a) Transport delay model



(b) Inertial delay model

Model with both inertial and transport delays:



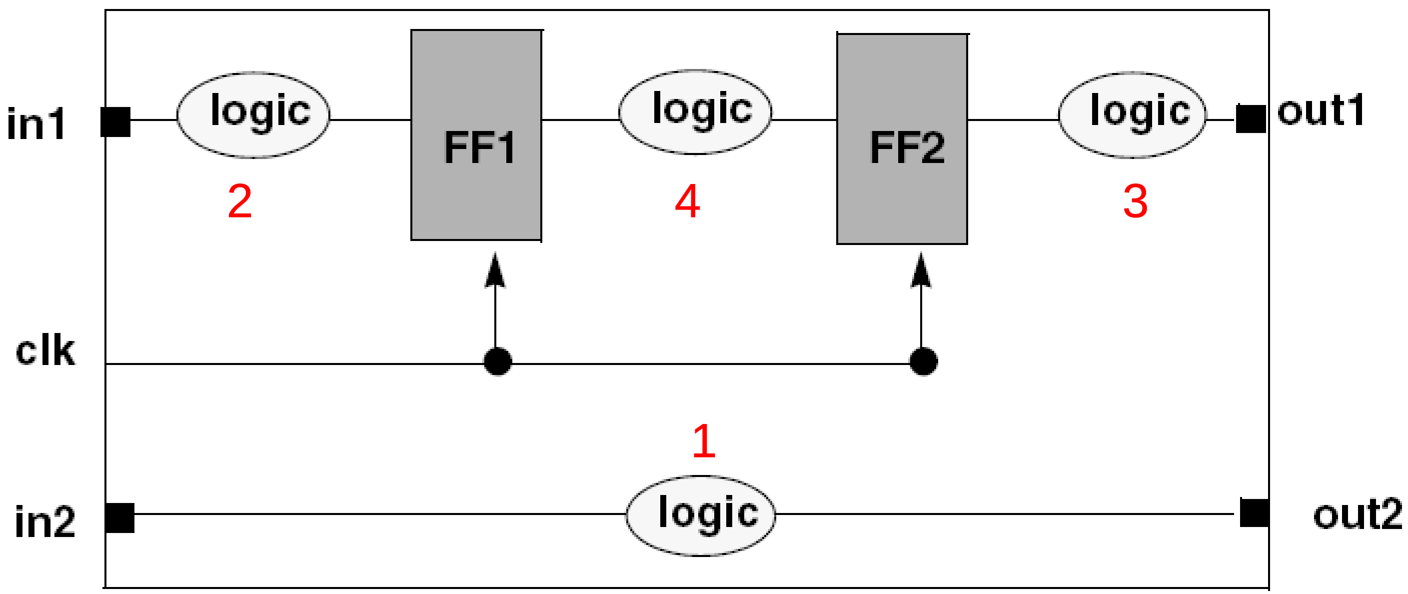
VHDL transport/inertial delays

- Default is "inertial" - reject pulses shorter than circuit switching time (cancel pending "events")
  - Op <= Ip after 10 ns;
  - Op <= inertial Ip after 10 ns;
  - Op <= reject 10 ns inertial Ip after 10 ns;
- "Transport" delay – transmit all pulses, of any duration
  - Op <= transport Ip after 10 ns;
  - Op <= transport Ip after 10 ns, not Ip after 20 ns

  Equivalent:
  - Op <= reject 0 ns inertial Ip after 10 ns;
  - Op <= reject 0 ns inertial Ip after 10 ns, not Ip after 20 ns

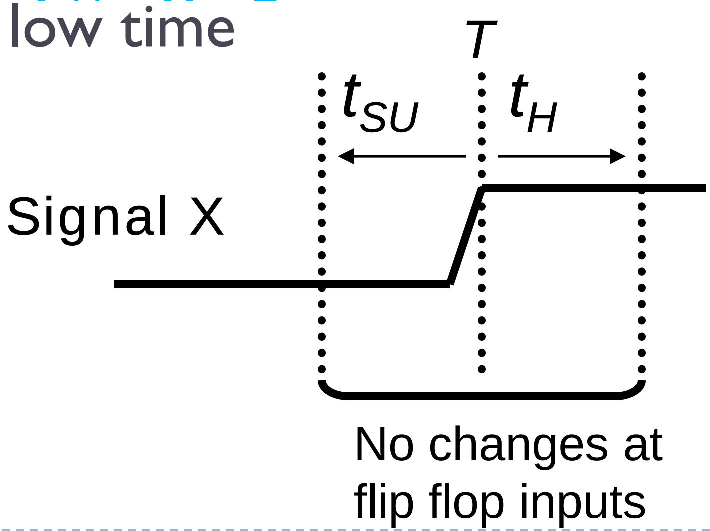
Path delays of interest

1. Combinational: primary input to primary output: in2->out2
2. Primary input to register input: in1 -> FF1/D1
3. Clock/register output to primary output: clk -> Q2 -> out1
4. Clock/register output to register input: clk -> Q1 -> D2



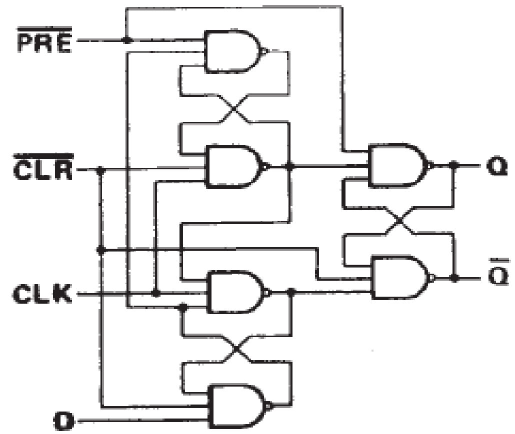
Timing Constraints: Flip flop setup, hold & clock times

- Constrain signal transitions to ensure reliable operation
  - **t_{SU} (setup time)** of signal X with respect to signal Y = time prior to active change on Y by which X must be stable
  - **t_H (hold time)** of signal X with respect to signal Y = time following active change on Y during which X must be stable
  - **t_{PW}, t_H, t_L** = clock signal minimum pulse width, high time, low time



T = time of clock transition
t_{SU} = flip flop setup time
t_H = flip flop hold time

SN74LS74A (D flip flop) parameters



			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$R_L = 2\ k\Omega$, $C_L = 15\ pF$	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

Source:http://focus.ti.com/lit/ds/symlink/sn74ls74a.pdf

ADK tsmc035 technology D flip flop

Report Timing Info for Instance /DFFR1 of TYPE QPT

tP = 0.637972 (ns) NONINV ON CLK(RI) TO Q(RI) --delays from CLK rise
tP = 0.746466 (ns) INV ON CLK(RI) TO QB(FA)
tP = 0.752151 (ns) INV ON CLK(RI) TO Q(FA)
tP = 0.896604 (ns) NONINV ON CLK(RI) TO QB(RI)
tP = 0.828865 (ns) INV ON R(RI) TO Q(FA) --delays from Reset active
tP = 0.973914 (ns) NONINV ON R(RI) TO QB(RI)

tS = 0.688299 (ns) ON D(H) TO CLK(RI) -- setup times
tS = 0.583595 (ns) ON D(L) TO CLK(RI)
taS = 0.579838 (ns) ON R(FA) TO CLK(RI)

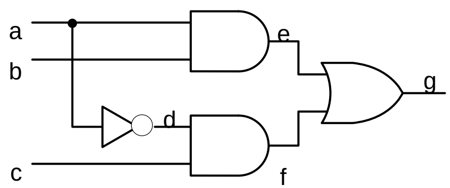
tH = -0.0942826 (ns) ON D(H) TO CLK(RI) -- hold times
tH = -0.052878 (ns) ON D(L) TO CLK(RI)
taH = 0.330582 (ns) ON R(FA) TO CLK(RI)

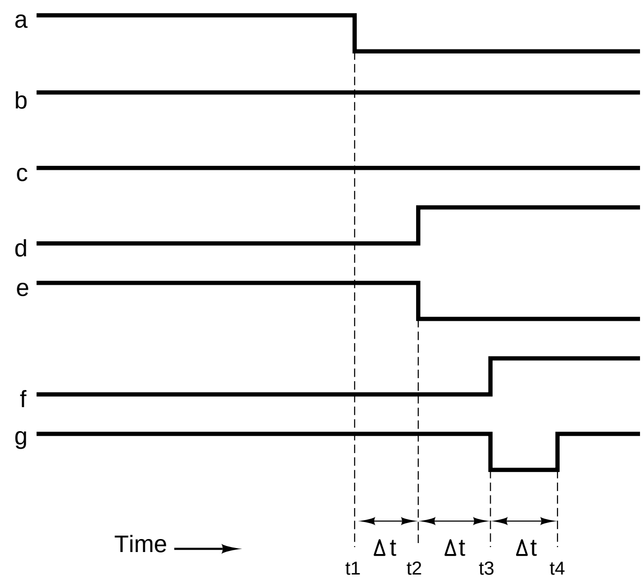
Methods for timing anaysis

- Timing simulation
  - Primitive element models include delay and constraint parameters
    - Gate and/or transistor level
  - Delays and constraint violations detected in simulation results
- Static timing analysis
  - Path delays calculated from primitive models
  - Determine max operating frequency by finding "critical path" = longest delay between successive flip flops

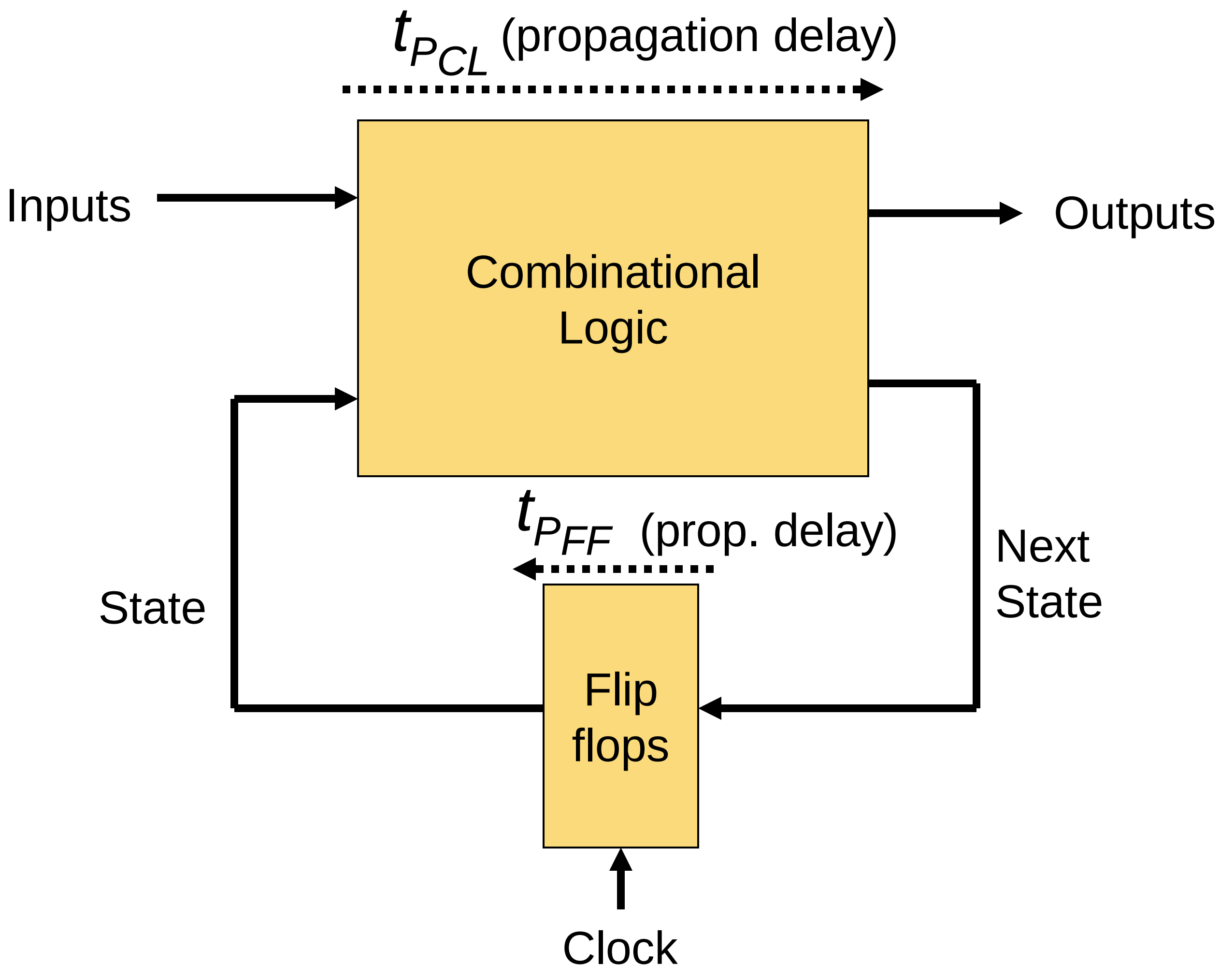
Detection of static hazards

- A glitch in *g* at time t_3 can be detected from the output waveforms.
- This occurs because both *e* and *f* become 0 momentarily between t_2 and t_3.

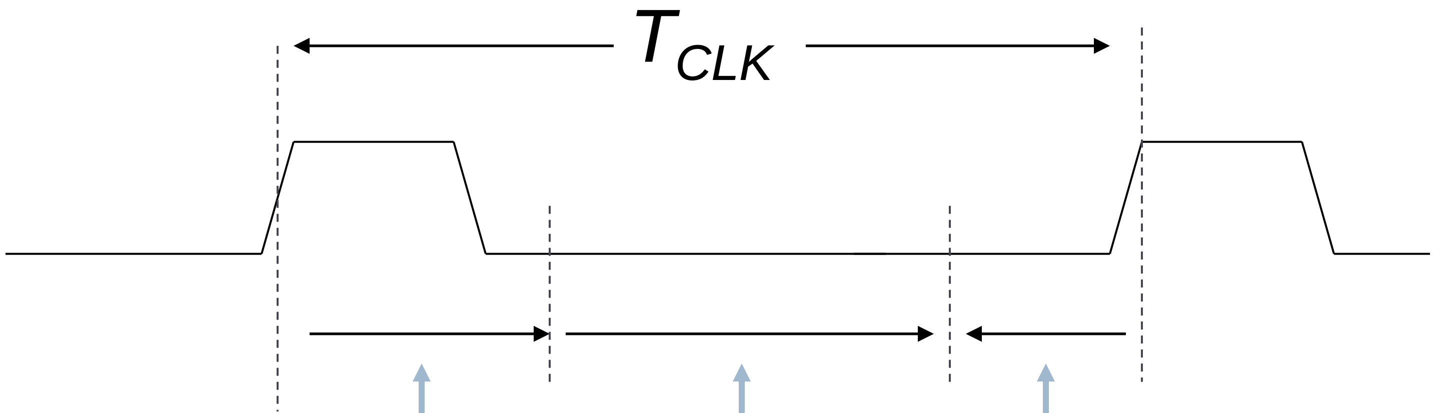




Circuit-level timing constraints



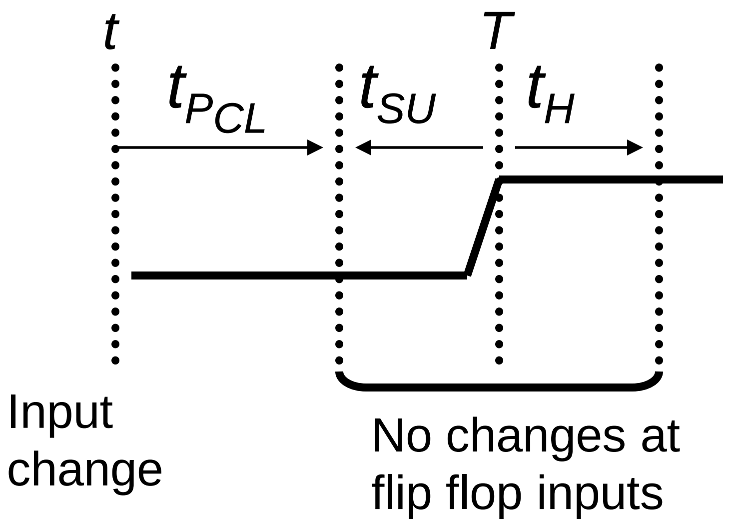
Minimum clock period



$$T_{CLK\,\min} = t_{P_{FF}} + t_{P_{CL}} + t_{su}$$

- $t_{P_{FF}}$: Flip flop propagation delay (max)
- $t_{P_{CL}}$: Combinational logic propagation delay (max)
- t_{su}: Flip flop setup time

External input setup/hold times



t_{PCL} = max, propagation delay from ext. signal to FF inputs
t_{SU} = flip flop setup time
t_H = flip flop hold time
T = time of clock transition
t = time of input change (Δx)

For reliable operation, constrain time t of external input changes, relative to the time T of the active clock transition:

$$\Delta x : t < T - t_{P_{CL}} - t_{su}$$ ← Satisfy setup time constraint

$$\Delta x : t > T + t_H - t_{P_{CL}}$$ ← Satisfy hold time constraint