

ELEC 5250_6250 Project 7 (Option #2)

Due: Tuesday, October 18, 2011

The purpose of this assignment is to compare an FPGA implementation of your divider circuit with the standard cell version synthesized previously by LeonardoSpectrum. Use the Xilinx ISE tools (in the ECE PC Labs in rooms 308/310, or you may download the free “Web Pack” from Xilinx for your own PC) to implement your divider circuit in a Spartan 3 FPGA (select the smallest available component in the Spartan 3 family.)

1. Create a project, with your divider circuit VHDL behavioral models as the “source”.
2. Run the full implementation process of synthesis, map, place and route, including the generation of a post place and route simulation model that can be used later to verify the final design and timing. You do not need to generate a “configuration file”, since we will not be downloading to an actual device.
3. Record the FPGA resources used (LUTs, slices, flip-flips, I/O blocks, etc.), and the maximum clock frequency at which the circuit can be operated.
4. Compare the FPGA resources and clock frequency to those of the standard cell circuit implemented by LeonardoSpectrum.
5. Simulate the synthesized circuit, and compare the simulation results with those obtained with the Leonardo-synthesized circuit.

To be submitted:

1. A summary of the synthesized circuit (FPGA components, number of cells) for the FPGA and Synopsys synthesized circuits, with a brief discussion of the differences.
2. A summary of the worst-case path and max clock frequency, for the standard cell and FPGA synthesized circuits.
3. Two pages of the simulation listing window, showing the operation of the synthesized circuit, including delays.

Reference materials on using the Xilinx ISE tools and Modelsim for FPGA design are available on Professor Stroud’s web site for ELEC 4200.

<http://www.eng.auburn.edu/~strouce/elec4200.html>