

## **ELEC 5250\_6250 Project #6**

### **Due: Tuesday, October 4, 2011**

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.

ELEC 6250 Students: Do this assignment with the divider circuit.

In this exercise, timing characteristics of the post-synthesis netlist will be studied and verified in *LeonardoSpectrum* and *Modelsim*. The following parameters are to be determined and verified, as if you were preparing a datasheet for your circuit.

1. The minimum clock period (and maximum clock frequency) for reliable operation. This should be determined from the longest reported delay path from a clock transition to all flip flop inputs stable, added to flip flop setup time. (If you set a clock period constraint, this should be the path with the worst “slack”.)
2. The worst case setup time for the circuit inputs. This can be determined from the worst case (longest) propagation delay from a circuit input pin to the flip-flop D inputs, including flip flop setup time.
3. The worst case delay from a clock transition to a circuit output pin.

Determine the above parameters from LeonardoSpectrum static timing analysis (delay) reports. Then, verify items 1, 2 and 3 by simulating the synthesized netlist in Modelsim with the standard delay format (SDF) file for the synthesized circuit, and measuring the parameters of interest in the simulation list window (use a list window rather than a wave window.) Highlight these on the printed listing. **Please “edit” the listing to save paper, printing only the lines of the simulation list window that show the events and parameters of interest.** Note that this requires determining the end points of the three worst case paths identified above, displaying these in the simulation list window, and executing an appropriate test sequence to exercise these paths. You may use either a testbench or a macro file to drive the simulation.

Report the parameters from items 1-2-3 in a table, listing the values predicted by LeonardoSpectrum in one column, and the values measured in the simulation list window in a second column.

Finally, re-verify items 1 and 2 by purposely creating violations of at least one flip flop setup time for each. Violations should be reported in a message window. Print the lines from the simulation list window showing these violations, plus the generated messages.