ELEC 5250/6250 Project #5 – Synthesis
Due Thursday, September 29, 2011

A. For the Modulo-6 counter designed previously:

1. Use "LeonardoSpectrum" to synthesize a gate-level netlist of ADK standard cells (tsmc025 technology), producing both VHDL and Verilog netlist files.

2. Repeat the structural simulation performed previously, but using the synthesized netlist, and verify that the synthesized circuit produces the same results as the behavioral model. If the results do not agree, comment on the differences. Use the previously-designed testbench to perform the simulation. Submit your simulation results for each of the following.
   a. Simulate the synthesized VHDL netlist.
   b. Repeat for the synthesized Verilog netlist.

   NOTE – We will save the "timing simulation" with the VITAL models and SDF file information for a future assignment.

3. Write a short comparison of the synthesized circuit and the schematic you designed by hand in the initial semester project, comparing the number of gate instances and "equivalent gate" counts. Comment on any "unexpected" or unusual results in the synthesized circuit from what you expected.

4. From a delay report, determine the longest path delay in the circuit, use this information to add a target clock period constraint and an "optimize_timing" command to your synthesis script, and compare the results to see if any improvement was made. Given the clock period constraint, what was the worst timing "slack", and through which modules does this path go?

B. Repeat the 4 steps of part A for the recently-designed divider circuit. However, during synthesis, maintain the design hierarchy and then determine the total number of instances and the total number of flip-flops for each "module" of the circuit. Comment on whether these counts are what you expected. In step 4, we would expect to see some improvement of the worst case path in the circuit.

For parts A and B, send via EMAIL the synthesized netlists from step 1, simulation listings from step 2, and a short report summarizing your comparison of the simulation results and the information in steps 3 and 4. ***(Do not print hard copies of all this information.)***