

ELEC 5250/6250 – Homework Project 2

Now that you have designed a gate-level structural model of a modulo-6 counter by hand, we want to (1) verify its correctness through simulation, (2) develop a behavioral model of the counter, which is where we would normally begin the design process, and (3) compare your hand-designed gate-level model with one that might be synthesized from the behavioral model by the Leonardo or Synopsys automatic synthesis tools. So, in this project you are to write **two** VHDL models.

Model 1.

Design a VHDL **behavioral** model of the modulo-6 counter from Homework Project 1. The model should have a single entity and architecture, and should therefore not instantiate any lower-level components. The inputs/outputs and behavior are to be identical to those of the hand-designed circuit. Use IEEE Standard 1164 data types “std_logic” and “std_logic_vector” instead of types “bit” and “bit_vector” throughout your model. Since this is a behavioral model, you may also use integers, if you wish.

Model 2.

Design a VHDL **structural** (netlist) model of your modulo-6 counter from Homework Project 1. This model will have the same entity as Model 1, but the architecture should contain only instantiations of logic gate components (gates, flip-flops, etc.), and have no “behavioral statements”. The gates should match those from your paper design (with any corrections as necessary), and must be selected from the ADK (ASIC Design Kit) library. The available cells in the library are defined in two VHDL files (linked to the course web site). File *adk.vhd* contains the actual models of all gates in the library, and file *adk_comp.vhd* defines a package named “adk_components” that contains component declarations of these gates. You may browse the latter (*adk_comp.vhd*) to determine the available gates. When we get ready for simulation, these two files are to be compiled into a library named “adk”. The components declaration package will then need to be made available via a “use” statement in your structural model as follows:

```
library adk;  
use adk.adk_components.all;
```

Homework Deliverables

For Thursday, submit printouts of the two VHDL models. We will simulate them for the next class. You should use comments throughout your design to help the instructor understand your logic.