

ELEC 5250_6250 Project 10

Due: 11 am, Friday, November 11, 2011

Part 1.

Create a SPICE model of a 2-input NAND gate, and simulate the operation of the gate in ADiT.

1. A NAND gate comprises 4 transistors. Look at the pre-layout netlist of your previous circuit saved from Design Architect-IC (the one used in the LVS check) for examples.
2. Include the SPICE models for the tsmc025 technology from \$ADK/technology/ic/models
3. Run the simulation three times, applying all four possible input vectors in each simulation.
 - a. The first simulation should use voltage sources on the two inputs.
 - b. The second simulation should use SETBUS/PLOTBUS/SIGBUS/CHECKBUS commands to apply the four input vectors and check the outputs.
 - c. The third simulation should use a test vector file to apply inputs and check outputs.
4. In one of the simulations, measure the delays (TPHL, TPLH) between each input and the output.

Part 2.

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.

ELEC 6250 Students: Do this assignment with the divider circuit.

Do post-layout simulation of the circuit layout from the previous project, using ADiT, checking both functionality and timing.

1. Verify correct results from your circuit for a sequence of inputs. Use one of the ADiT simulation methods that provides automatic checking of outputs.
2. Measure one worst-case circuit path of each of the following types, as determined in your previous timing analysis, and compare the ADiT results to the values found in the previous timing analysis.
 - a. One worst-case flip-flop to flip-flop delay (used to find max clock frequency)
 - b. One worst-case flip-flop to output delay (clock to output)
 - c. One worst-case input to flip-flop delay (used to find input setup time)

Again, for this assignment, a project report is to be submitted electronically as a Word document. For each simulation, insert into the report whatever you feel best demonstrates the information of interest.