

Introduction to ASIC Design

Smith Text – Chapter 1

Application-Specific IC (ASIC)

Designed for a specific application

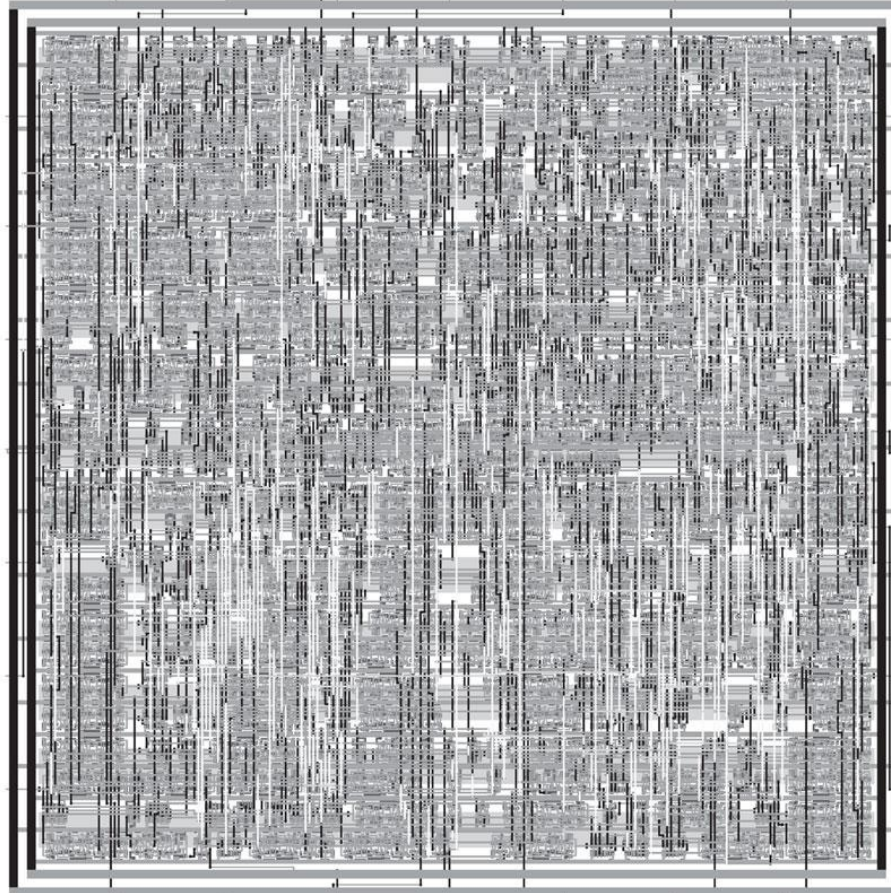


FIG 1.64 Synthesized MIPS processor

Source: N. Weste, "CMOS VLSI Design"

Worldwide semiconductor market

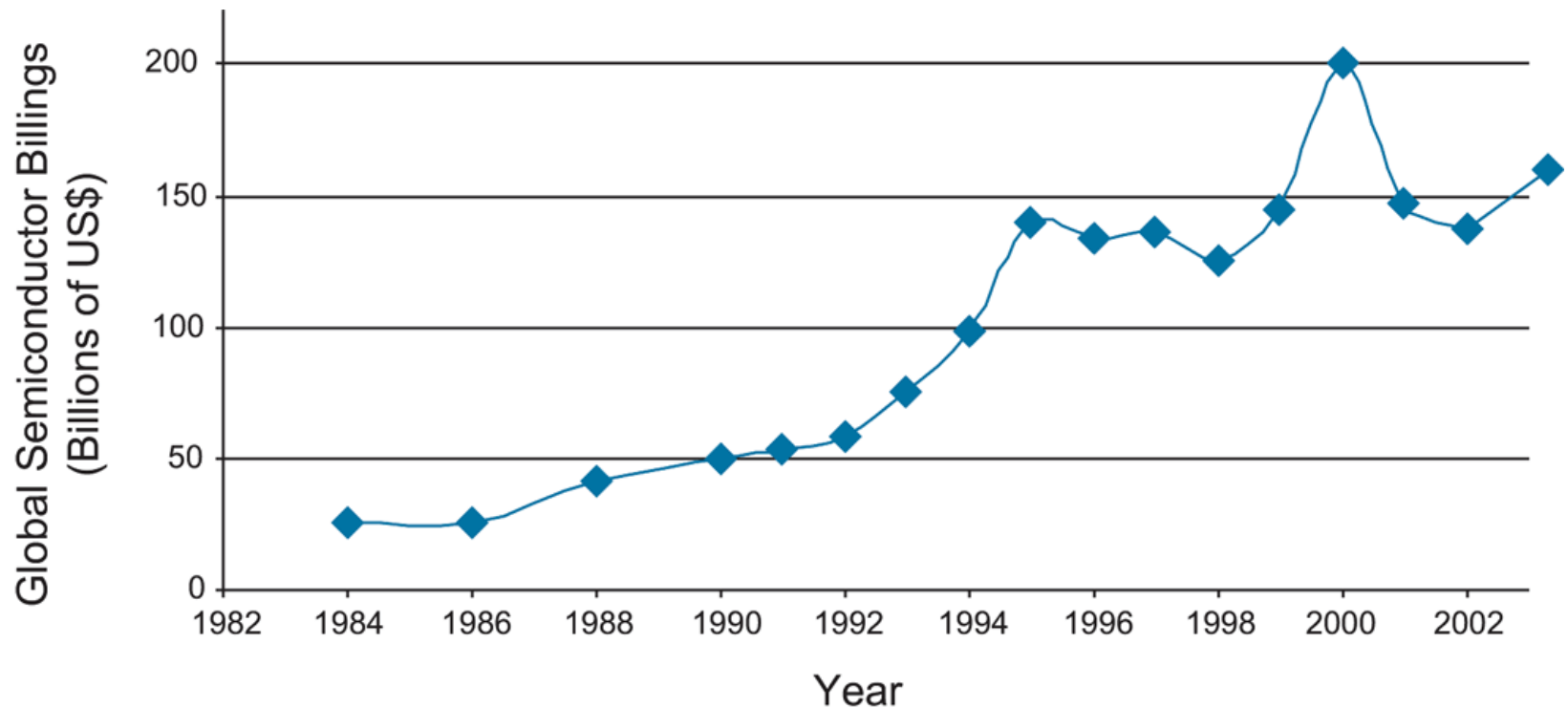


FIG 1.1 Size of worldwide semiconductor market

Source: Semiconductor Industry Association.

Source: N. Weste, "CMOS VLSI Design"

Progress of State of the Art

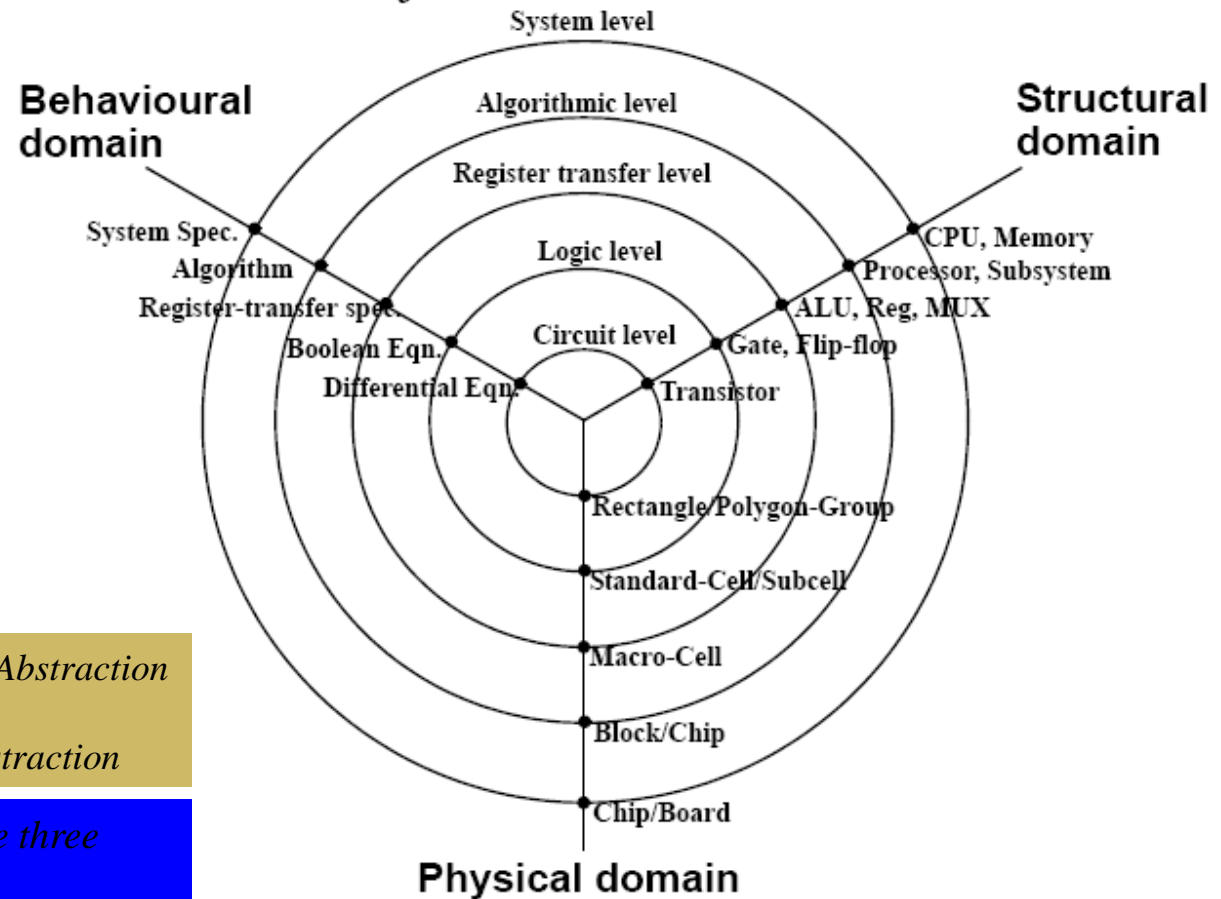
Year	Integration Level	# devices	Function
1938-46	Electromagnetic relays	1	
1943-54	Vacuum tubes	1	
1947-50	Transistor invented	1	
1950-61	Discrete components	1	
1961-66	SSI	10's	Flip-flop
1966-71	MSI	100's	Counter
1971-80	LSI	1,000's	uP
1980-85	VLSI	100,000's	uC
1985-90	ULSI*	1M	uC*
1990	GSI**	10M	SoC
2008	Intel Six-Core Xeon 7400	1.9G	CPU

Hierarchical Abstraction Levels in ASIC Design

- System (CPUs, I/O, memory)
- Behavior/algorithm (HDL)
- Register transfer
- Logic Gate (net list)
- Circuit (transistor)
- Mask/layout (physical design)

The Taxonomy of VLSI Design Space

Gajski Kuhn Y Chart.



*Concentric Circles Represent Abstraction Levels
Larger Circles → Greater Abstraction*

The three axes represents the three domains

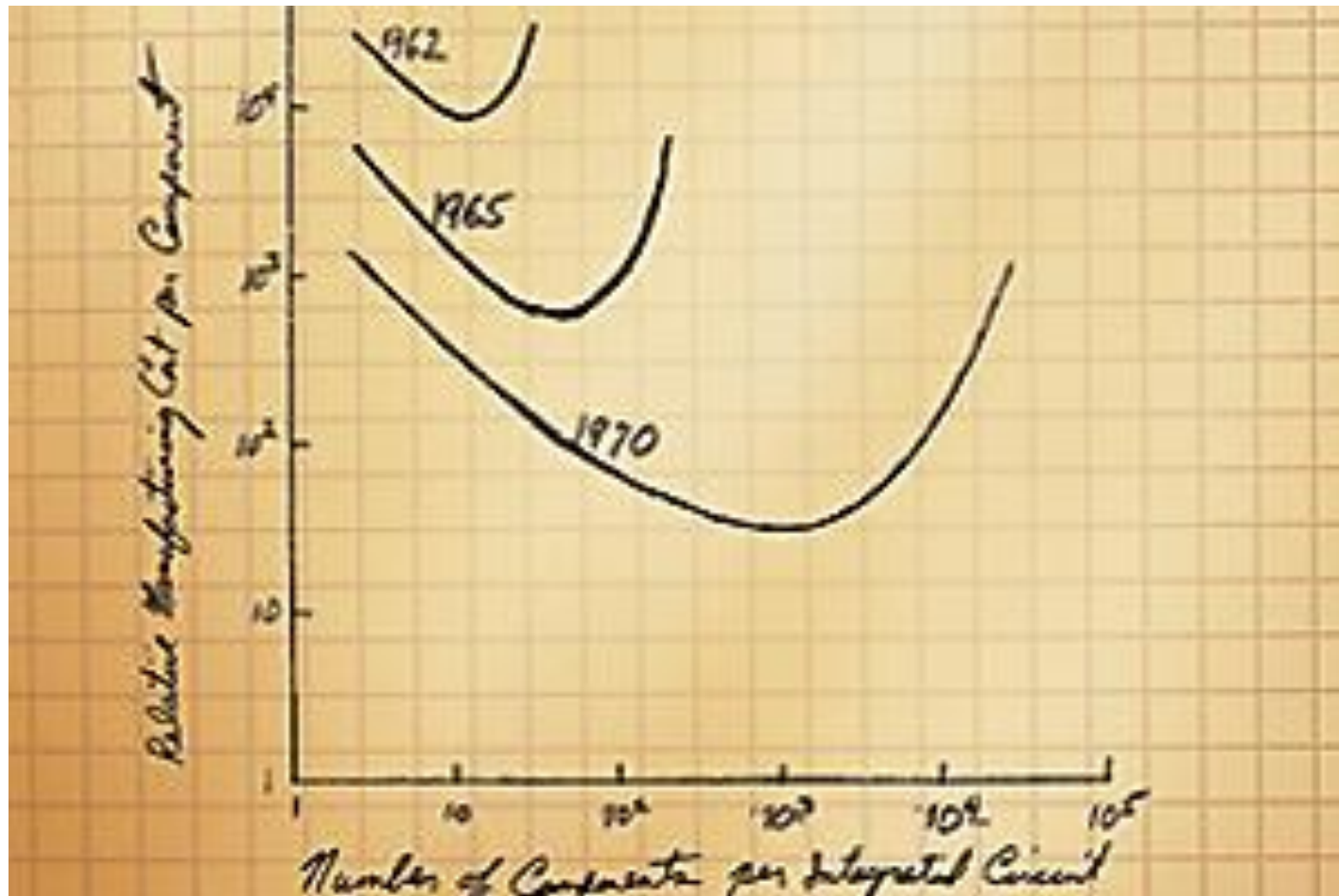
Moore's Law

- Gordon Moore (1965):

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer.”

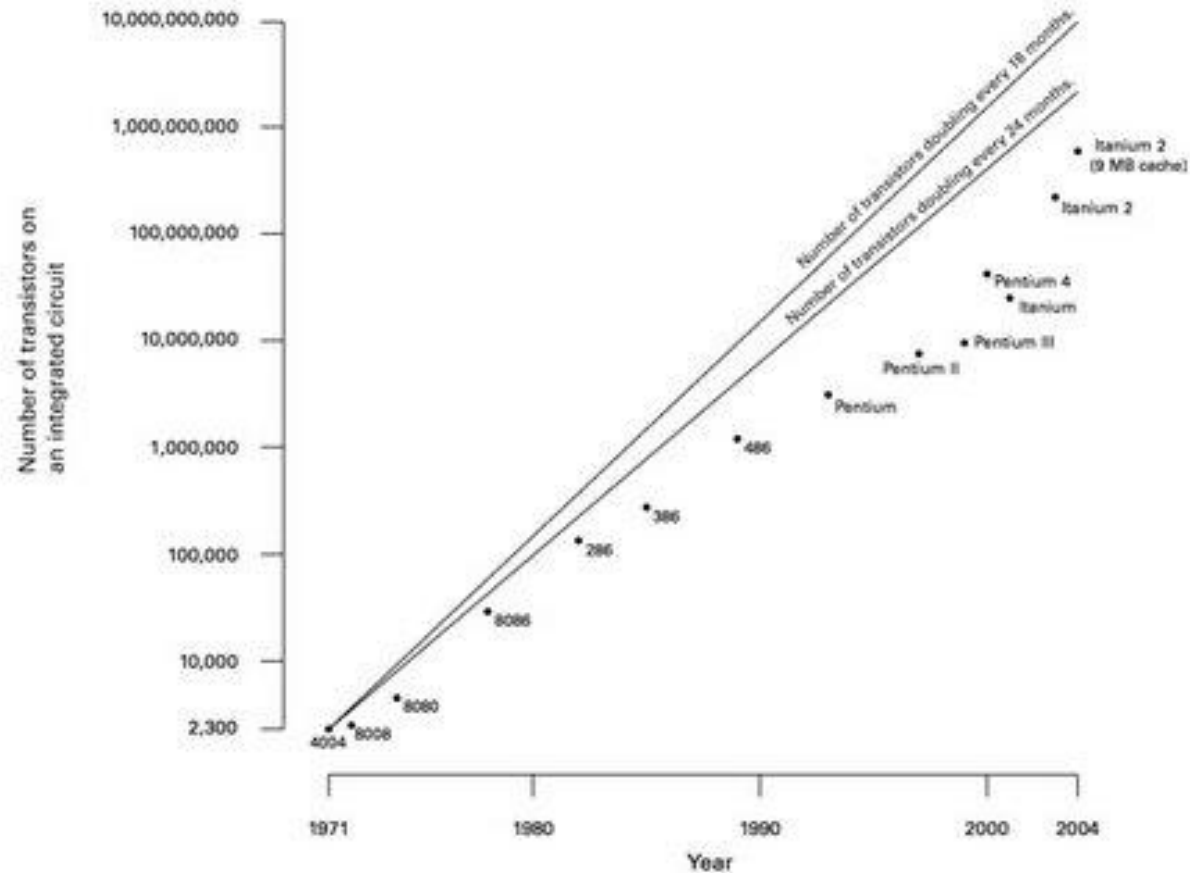
- Now doubling about every 18 months

Moore's Law – Original Graph



Moore's Law Updated

Moore's Law



ASIC clock frequencies

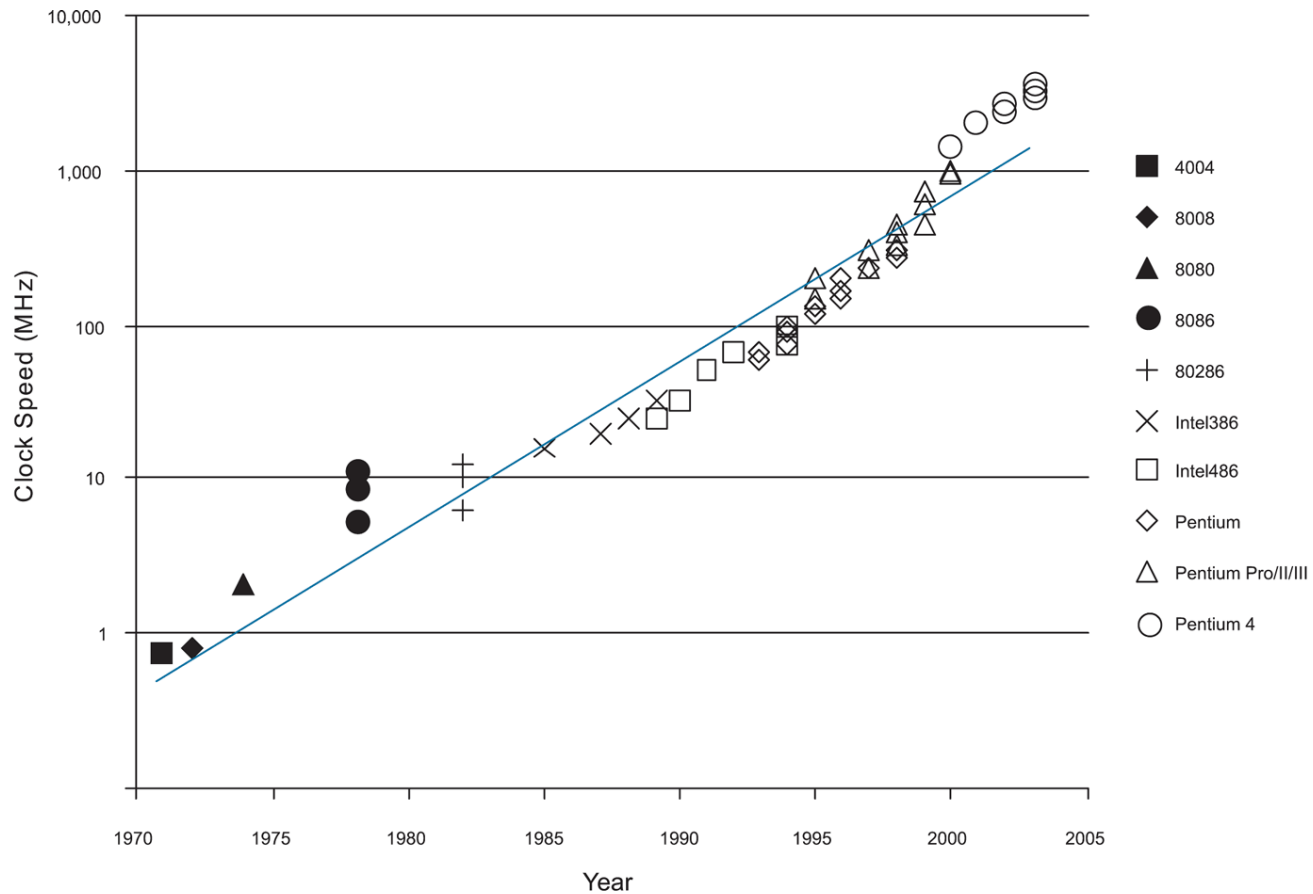


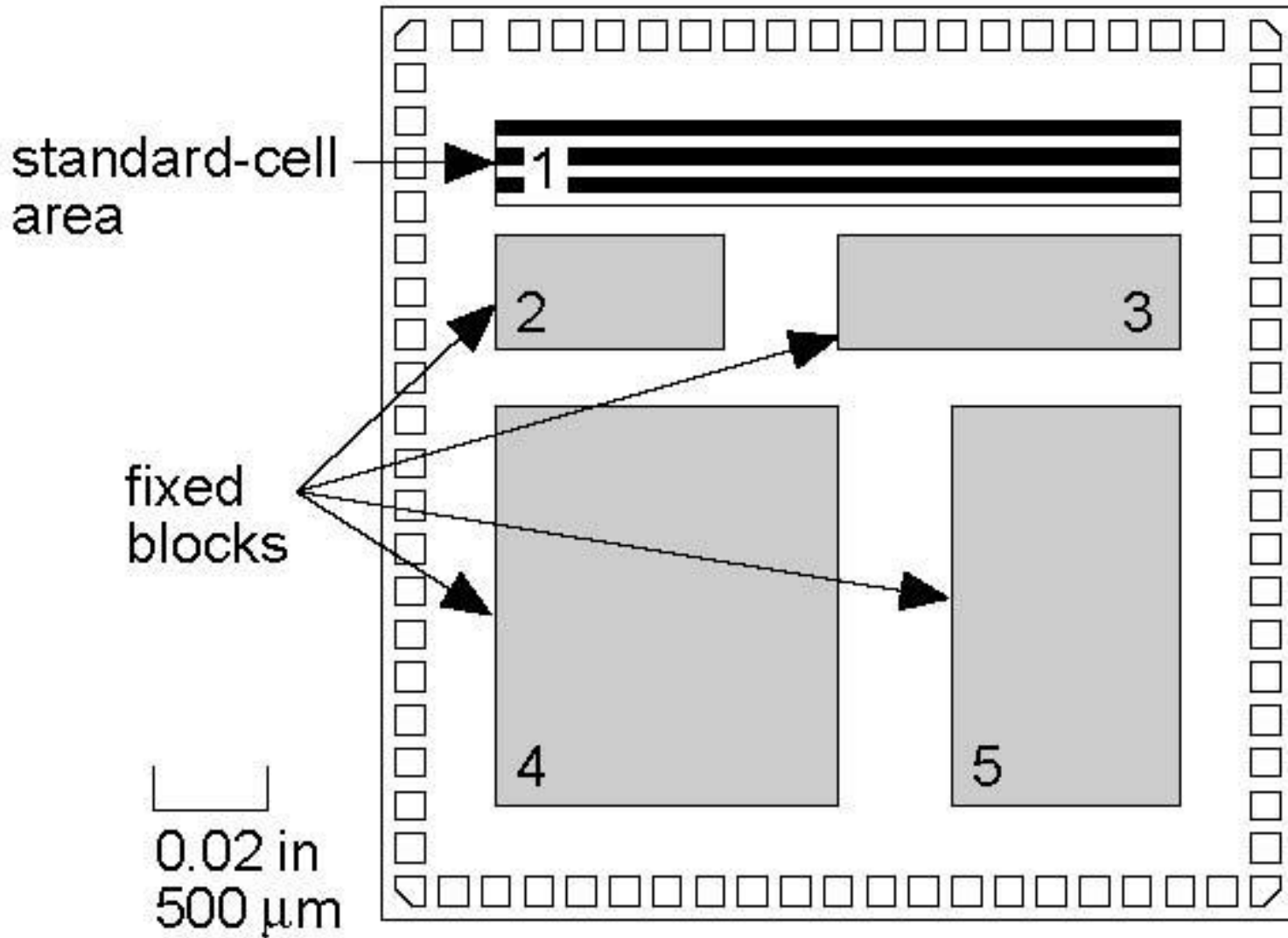
FIG 1.5 Clock frequencies of Intel microprocessors

Source: N. Weste, "CMOS VLSI Design"

ASIC Technologies

- Full custom IC design
- Standard cell based IC
- Mask-programmable gate array
- Field-programmable gate array (FPGA)
- Complex programmable logic device (CPLD)
- Platform/structured ASIC
- Software-programmable device
- Commercial off the shelf (COTS) device

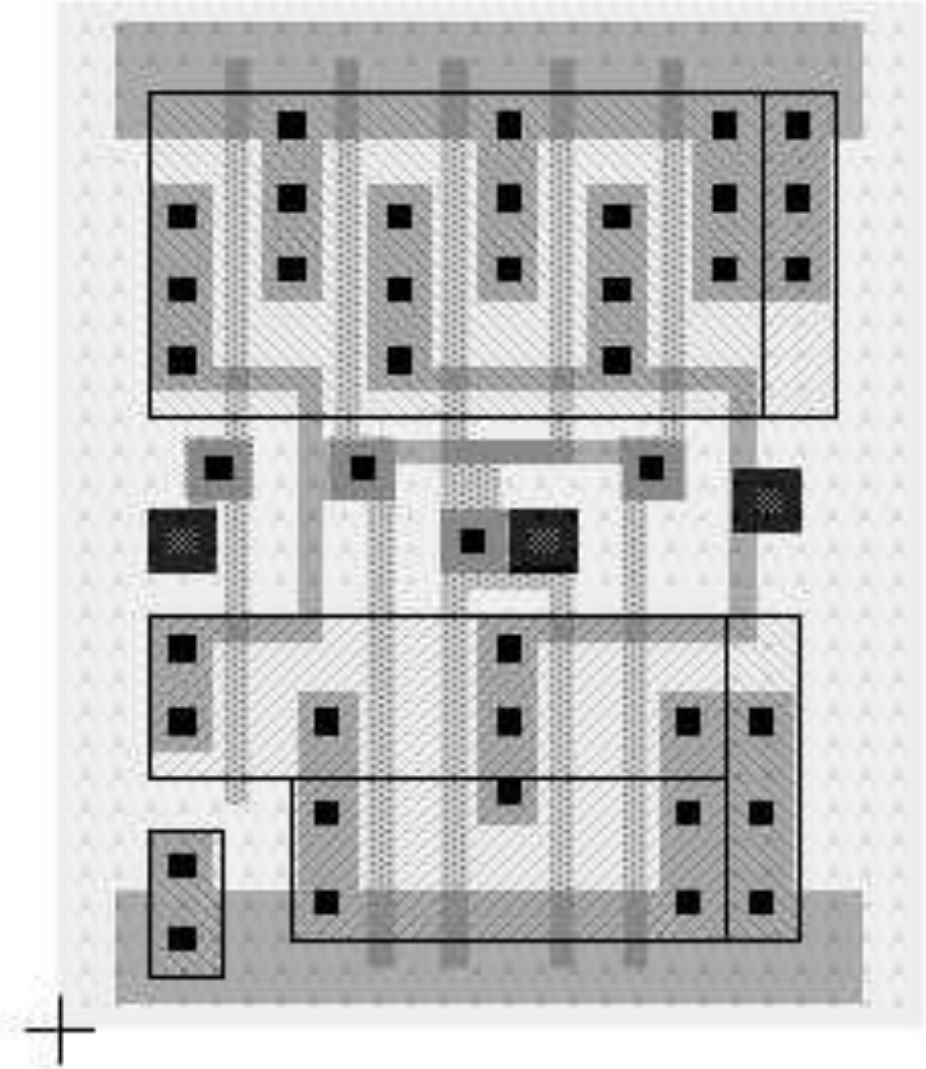
Cell-Based IC



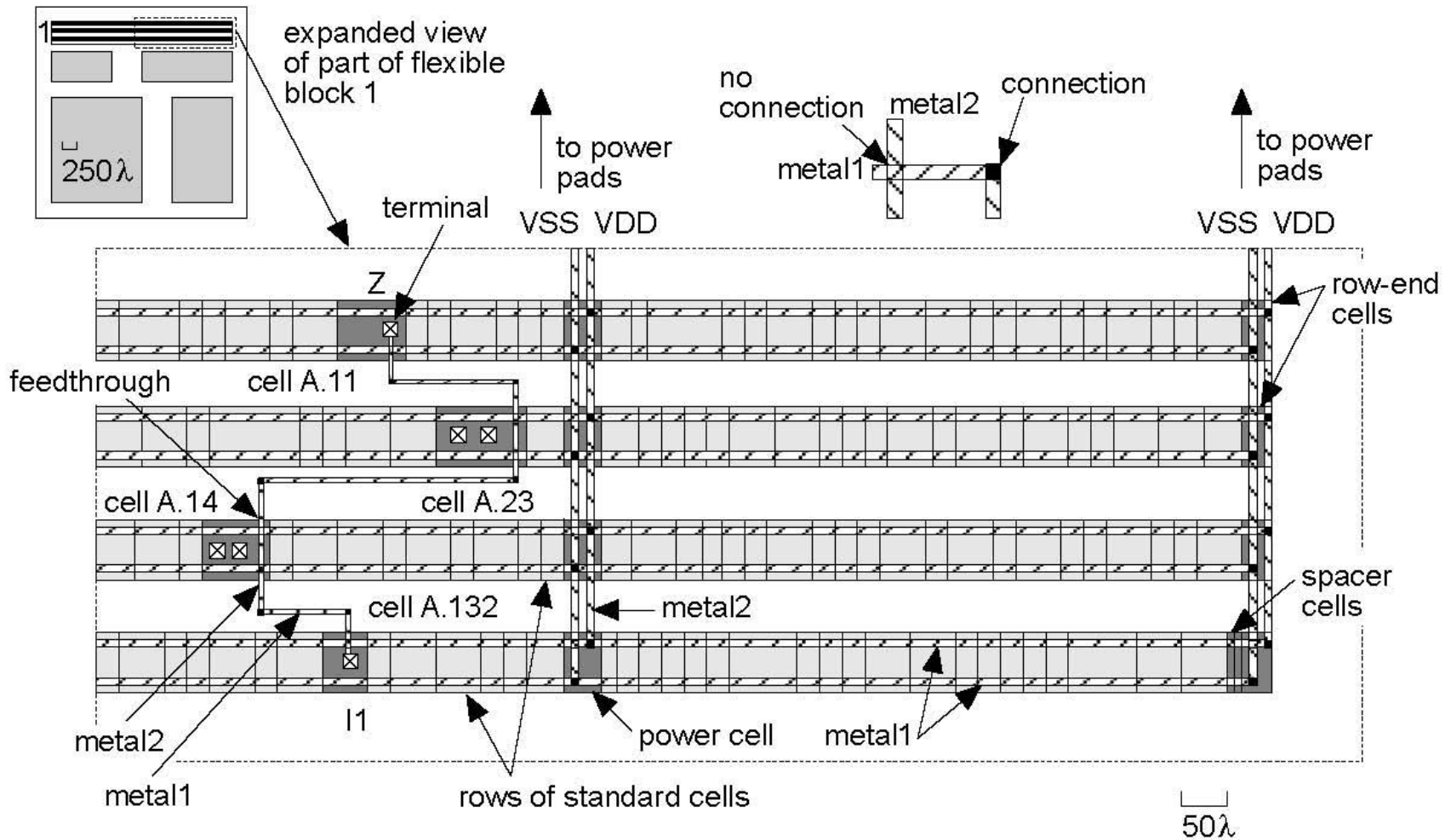
Standard Cell-Based ASIC

- Build design with predesigned “cells”
- Each cell characterized
- Customize placement and interconnect
- 8-week lead time (must fabricate all layers)
- Place cells into fixed-height rows

Standard Cell



Cell-Based Block

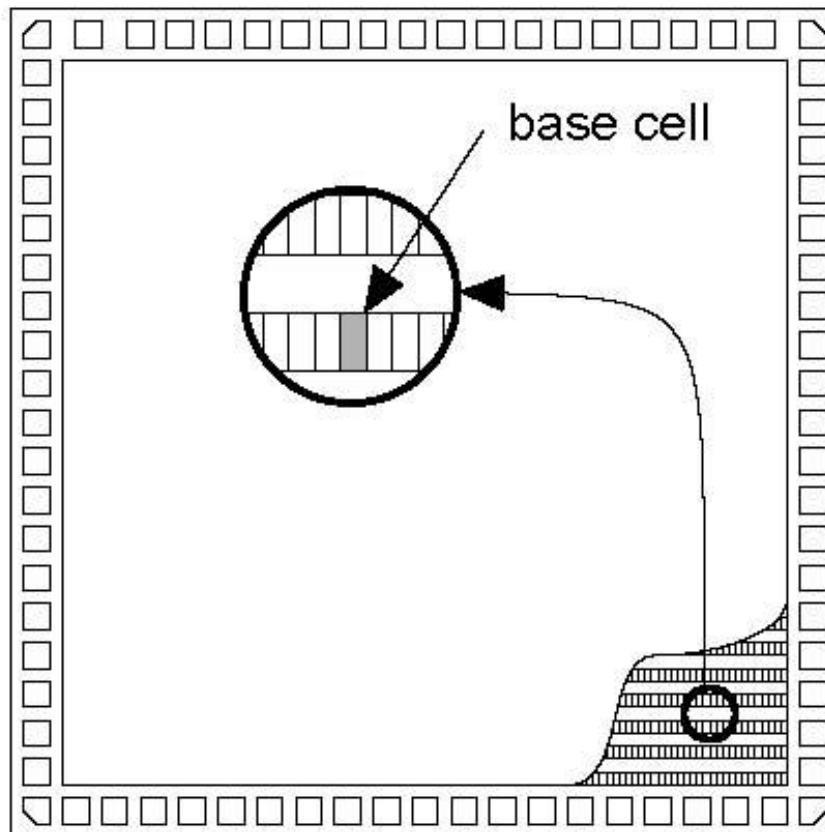


Masked Gate Array

- Map design onto gates in the array
 - Gates designed & characterized
- Customize placement and interconnect
- Lead time = few days to 2 weeks
- Cell library usually contains “macros”
 - Patterns of gates/functions
 - Soft vs. hard macros

Channeled Gate Array

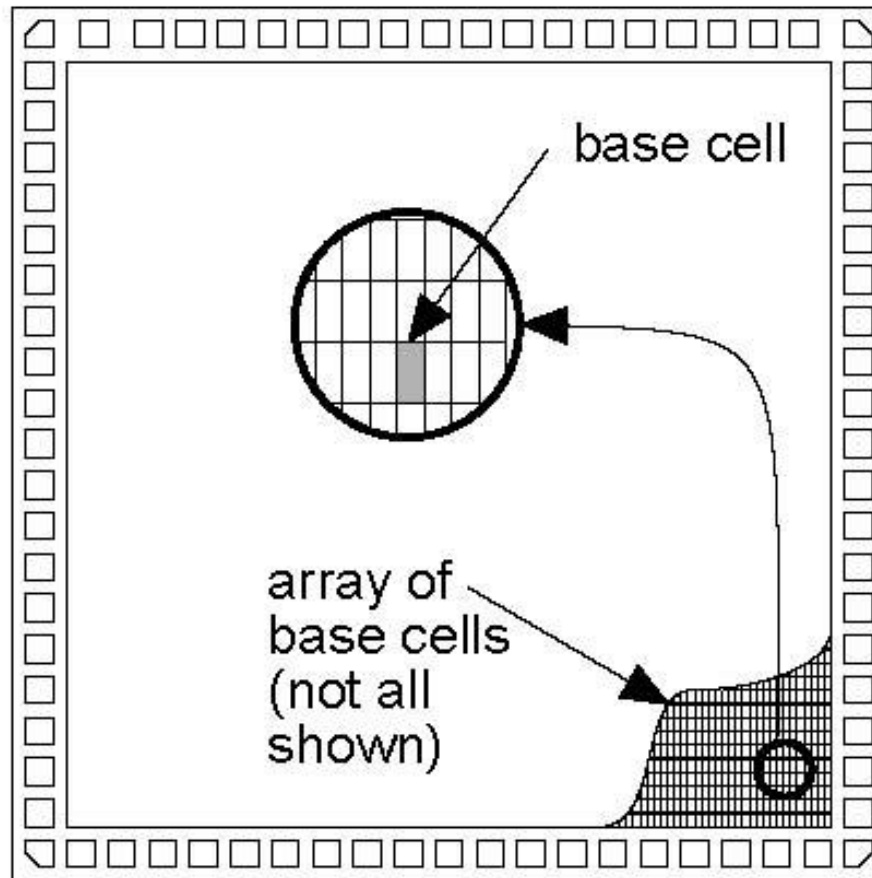
Route in spaces between rows of gates



“Sea of Gates” (Channelless) Array

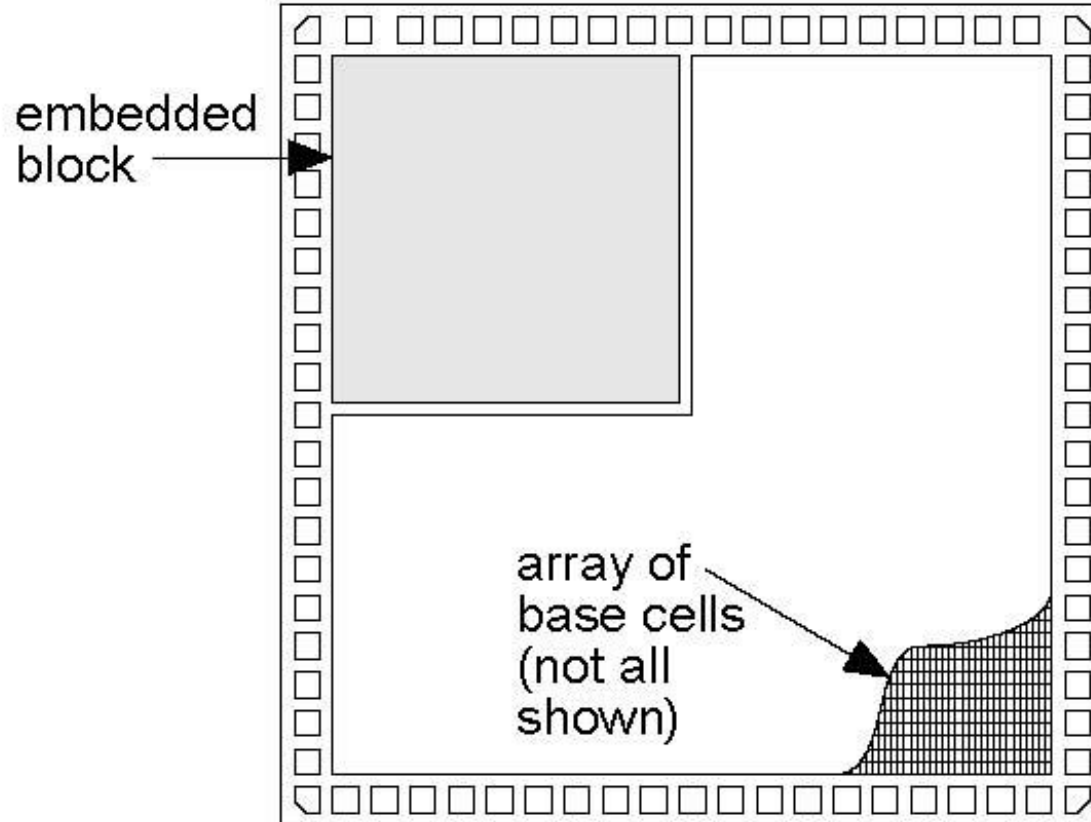
Route over gates

Don't use gates under wires

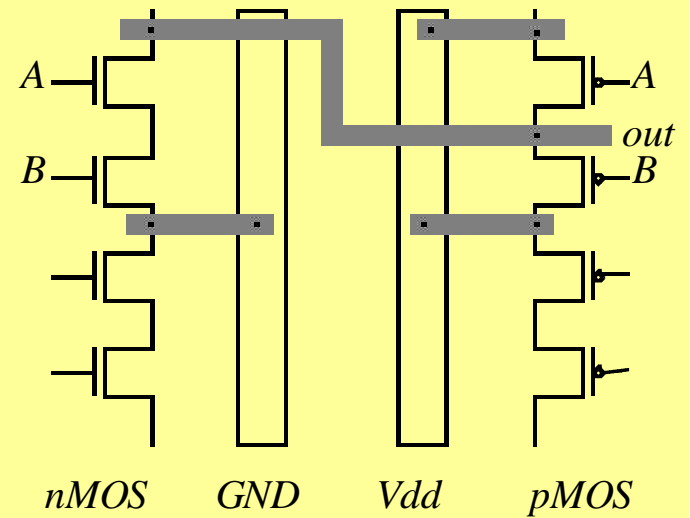
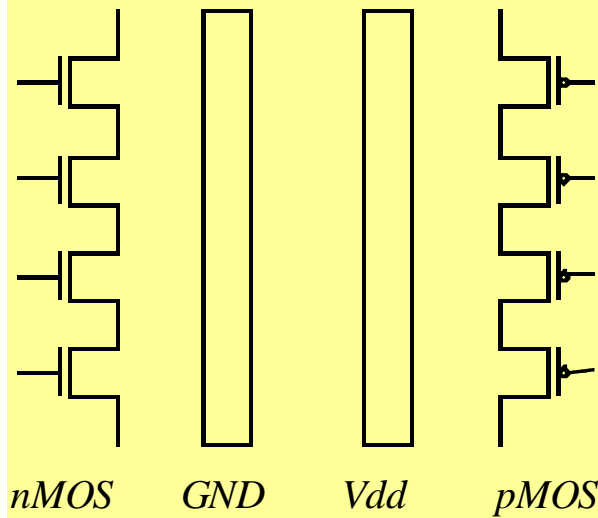


Structured/Embedded Gate Array

Embedded blocks (microprocessor, memory)
Customize interconnect and gate array



MPGAs contd.

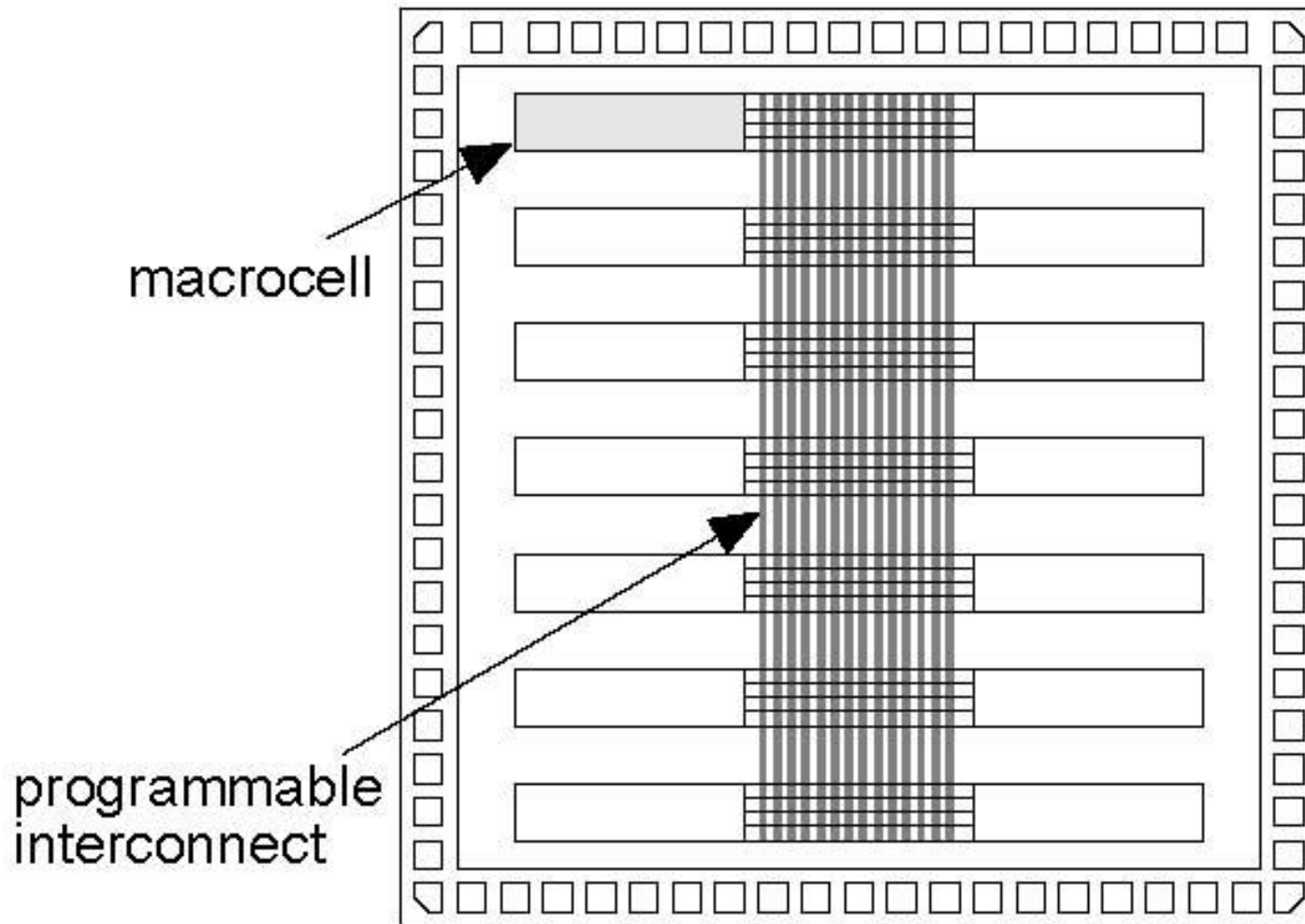


Programmable Logic Devices

- No custom circuitry
- USER programs logic/interconnects
- ROM-EPROM-EEROM-RAM based
- Design turnaround time in hours

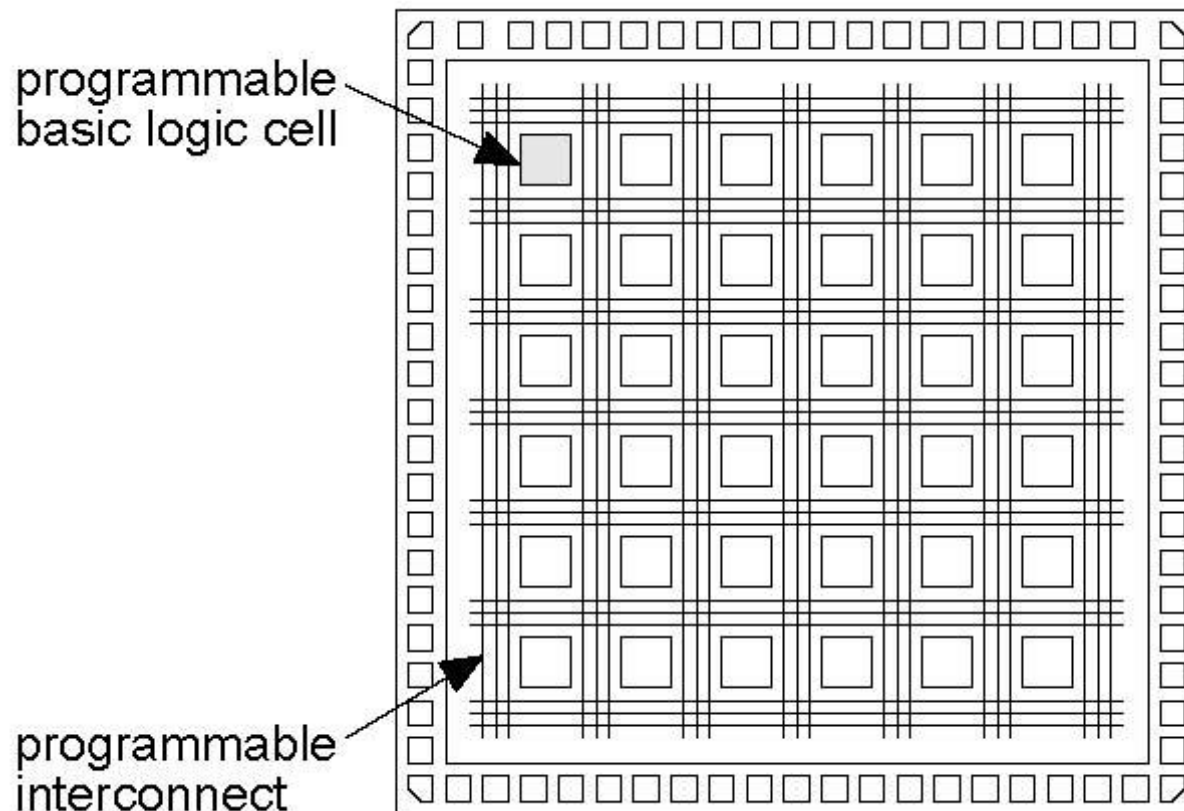
- FPGA: array of gates & interconnects
- PLD: based on AND/OR array

Programmable Logic Device Die



Field-Programmable Gate Array

Program logic cells, I/O pads & interconnects



FPGA Evolution

● FPGA	Transistor count	Date	Manufacturer
● <u>Virtex</u>	~70,000,000	1997	Xilinx
● <u>Virtex-E</u>	~200,000,000	1998	Xilinx
● <u>Virtex-II</u>	~350,000,000	2000	Xilinx
● <u>Virtex-II PRO</u>	~430,000,000	2002	Xilinx
● <u>Virtex-4</u>	1,000,000,000	2004	Xilinx
● <u>Virtex-5</u>	1,100,000,000	2006	Xilinx
● <u>Stratix IV</u>	2,500,000,000	2008	Altera

VLSI Implementations

	Custom	Standard cell	Gate array	FPGA
Density	Highest	Medium	Low	Lowest
Performance	Highest	Medium	Low	Lowest
Design time	Long	Medium	Short	Shortest
Chip Dev cost	High	Medium	Low	Lowest
Testability	Difficult	Less difficult	Easy	Easy
High Volume?	High	Medium	Low	Lowest

Comparing Implementation Styles

