Introduction to ASIC Design

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Refer to Michael J. S. Smith

*Application-Specific Integrated Circuits*
Application-Specific IC (ASIC)
Designed for a specific application

Source: N. Weste, “CMOS VLSI Design”
## Progress of State of the Art

<table>
<thead>
<tr>
<th>Year</th>
<th>Integration Level</th>
<th># devices</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1938-46</td>
<td>Electromagnetic relays</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1943-54</td>
<td>Vacuum tubes</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1947-50</td>
<td>Transistor invented</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1950-61</td>
<td>Discrete components</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1961-66</td>
<td>SSI</td>
<td>10’s</td>
<td>Flip-flop</td>
</tr>
<tr>
<td>1966-71</td>
<td>MSI</td>
<td>100’s</td>
<td>Counter</td>
</tr>
<tr>
<td>1971-80</td>
<td>LSI</td>
<td>1,000’s</td>
<td>uP</td>
</tr>
<tr>
<td>1980-85</td>
<td>VLSI</td>
<td>100,000’s</td>
<td>uC</td>
</tr>
<tr>
<td>1985-90</td>
<td>ULSI*</td>
<td>1M</td>
<td>uC*</td>
</tr>
<tr>
<td>1990</td>
<td>GSI**</td>
<td>10M</td>
<td>SoC</td>
</tr>
<tr>
<td>2011</td>
<td>Intel Ten-Core Xeon</td>
<td>2.6G</td>
<td>CPU</td>
</tr>
</tbody>
</table>
Hierarchical Abstraction Levels in ASIC Design

- System (CPUs, I/O, memory)
- Behavior/algorithm (HDL)
- Register transfer
- Logic Gate (net list)
- Circuit (transistor)
- Mask/layout (physical design)
The taxonomy of VLSI design space

Concentric Circles Represent Abstraction Levels
Larger Circles → Greater Abstraction

The three axes represent the three domains
Moore’s Law

- Gordon Moore (1965):
  “The complexity for minimum component costs has increased at a rate of roughly a factor of two per year … Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer.”

- Now doubling about every 18 months
Moore’s Law – Original Graph
Moore’s Law Updated
ASIC clock frequencies

FIG 1.5 Clock frequencies of Intel microprocessors

Source: N. Weste, “CMOS VLSI Design”
ASIC Technologies

- Full custom IC design
- Standard cell based IC
- Mask-programmable gate array
- Field-programmable gate array (FPGA)
- Complex programmable logic device (CPLD)
- Platform/structured ASIC
- Software-programmable device
- Commercial off the shelf (COTS) device
Cell-Based IC

standard-cell area

fixed blocks

0.02 in
500 μm
Standard Cell-Based ASIC

- Build design with predesigned “cells”
- Each cell characterized
- Customize placement and interconnect
- 8-week lead time (must fabricate all layers)
- Place cells into fixed-height rows
Standard Cell
Cell-Based Block

expanded view of part of flexible block 1

terminal

to power pads

to power pads

connection

no connection

metal1

metal2

metal1

metal2

VSS VDD

VSS VDD

feedthrough

cell A.11

cell A.14

cell A.23

cell A.132

I1

power cell

rows of standard cells

row-end cells

spacer cells

250λ
Masked Gate Array

- Map design onto gates in the array
  - Gates designed & characterized
- Customize placement and interconnect
- Lead time = few days to 2 weeks
- Cell library usually contains “macros”
  - Patterns of gates/functions
  - Soft vs. hard macros
Channeled Gate Array

Route in spaces between rows of gates

base cell
“Sea of Gates” (Channelless) Array

Route over gates
Don’t use gates under wires
Structured/Embedded Gate Array

Embedded blocks (microprocessor, memory)
Customize interconnect and gate array
MPGAs contd.
Programmable Logic Devices

- No custom circuitry
- USER programs logic/interconnects
- ROM-EPROM-EEROM-RAM based
- Design turnaround time in hours

- FPGA: array of gates & interconnects
- PLD: based on AND/OR array
Programmable Logic Device Die
Field-Programmable Gate Array

Program logic cells, I/O pads & interconnects
## FPGA Evolution

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Transistor count</th>
<th>Date</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex</td>
<td>~70,000,000</td>
<td>1997</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Virtex-E</td>
<td>~200,000,000</td>
<td>1998</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Virtex-II</td>
<td>~350,000,000</td>
<td>2000</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Virtex-II PRO</td>
<td>~430,000,000</td>
<td>2002</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Virtex-4</td>
<td>1,000,000,000</td>
<td>2004</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Virtex-5</td>
<td>1,100,000,000</td>
<td>2006</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Stratix IV</td>
<td>2,500,000,000</td>
<td>2008</td>
<td>Altera</td>
</tr>
<tr>
<td>Virtex-7</td>
<td>6,800,000,000</td>
<td>2012</td>
<td>Xilinx</td>
</tr>
</tbody>
</table>
“Structured ASIC”

● Contains pre-configured IP cores
  - CPUs, memory, serial I/O, etc

● Contains blocks of programmable “gate array” structures
  ● Map netlist onto gate array
  ● Fab company creates masks for top metal layers only

● Market position between FPGA and standard cell based ASIC
Faraday - Profile of 1P7M Structured ASIC (www.faraday-tech.com)
Structured ASIC Approach
(NEC Electronics America)

Metal layers customized for the design

(Electronic Design Supplement – July 20, 2006)
LSI Logic “CoreWare” IP Solution (www.RapidChip.com)

Designing with pre-integrated systems of IP
(Electronic Design Supplement – Sep. 6, 2004)
LSI Logic “CoreWare” IP Solution
(www.RapidChip.com)

(Electronic Design Supplement – Sep. 6, 2004)
Faraday TEMPLATE platform ASIC

www.faraday-tech.com

Figure 4: A TEMPLATE master-slice
Faraday platform ASIC examples
www.faraday-tech.com

Figure 5: (a) A DisplayComposer Chip
(b) A NetComposer Chip
## Faraday TEMPLATE structured ASICs

[www.faraday-tech.com](http://www.faraday-tech.com)

<table>
<thead>
<tr>
<th>MasterSlice</th>
<th>FT2000</th>
<th>FT3000</th>
<th>FT4000</th>
<th>FT5000</th>
<th>FT6000</th>
<th>FT7000</th>
<th>FT8000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Usable ASIC Gates</td>
<td>256K</td>
<td>1024K</td>
<td>1024K</td>
<td>2236K</td>
<td>2048K</td>
<td>4352K</td>
<td>6400K</td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>512K</td>
<td>1024K</td>
<td>768K</td>
<td>1536K</td>
<td>1664K</td>
<td>2560K</td>
<td>4224K</td>
</tr>
<tr>
<td>Number of PLL</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>8</td>
<td>12</td>
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<tr>
<td>Number of DLL</td>
<td>-</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
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<td>32bit CPU</td>
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<tr>
<td>USB OTG</td>
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<td>1</td>
<td>1</td>
<td>2</td>
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<td>2</td>
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<tr>
<td>E'net 10/100</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
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<td>OSC/POR/VDT</td>
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<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<tr>
<td>System clock Speed</td>
<td>500MHz+</td>
<td>500MHz+</td>
<td>500MHz+</td>
<td>500MHz+</td>
<td>500MHz+</td>
<td>500MHz+</td>
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<tr>
<td>Max. IO available</td>
<td>208</td>
<td>292</td>
<td>292</td>
<td>388</td>
<td>388</td>
<td>484</td>
<td>580</td>
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<td>Package</td>
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<td>QFP128</td>
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<td>*</td>
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<tr>
<td>QFP208</td>
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<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<tr>
<td>BGA256</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<td>BGA292</td>
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<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<tr>
<td>BGA352</td>
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<td>*</td>
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<td>*</td>
<td>*</td>
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<td>BGA388</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>BGA484</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<tr>
<td>BGA580</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

**Table 2: Template Family**
Nvidia Tegra 2 System on Chip (SoC)

Tablet Applications:
- Asus Eee Pad
- Motorola Xoom
- Samsung Galaxy
- Acer Iconia Tab
# VLSI Implementations

<table>
<thead>
<tr>
<th></th>
<th>Custom</th>
<th>Standard cell</th>
<th>Gate array</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>Highest</td>
<td>Medium</td>
<td>Low</td>
<td>Lowest</td>
</tr>
<tr>
<td>Performance</td>
<td>Highest</td>
<td>Medium</td>
<td>Low</td>
<td>Lowest</td>
</tr>
<tr>
<td>Design time</td>
<td>Long</td>
<td>Medium</td>
<td>Short</td>
<td>Shortest</td>
</tr>
<tr>
<td>Chip Dev cost</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
<td>Lowest</td>
</tr>
<tr>
<td>Testability</td>
<td>Difficult</td>
<td>Less difficult</td>
<td>Easy</td>
<td>Easy</td>
</tr>
<tr>
<td>High Volume?</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
<td>Lowest</td>
</tr>
</tbody>
</table>
Comparing Implementation Styles

- **System Design**
  - **Layout**
    - 2-50 wks
  - **Masks & Prototyping**
    - 8-10 wks
  - **Test program processing**
    - 8-10 wks

- **Auto routing**
  - 1-2 wks
  - 8-10 wks
  - 8-10 wks

- **Std. Cell**
  - **Gate Array**
    - 1-2 wks
    - 1-2 wks
    - 2-3 wks

- **Field Programmable Gate Array.**
  - 1-2 wks

Interface to foundary house.

- **Full Custom**
- **Std. Cell**
- **Gate Array**
- **Field Programmable Gate Array.**