Bulletin Description: ELEC 5250. COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS (3) LEC. 3. Pr., ELEC 2220 or COMP 3350. Computer-automated design of digital logic circuits, using discrete gates, programmable logic devices, and standard cells, hardware description languages, circuit simulation for design verification and analysis, fault diagnosis and testing.

ELEC 6250. COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS (3) LEC. 3. Computer-automated design of digital logic circuits, using discrete gates, programmable logic devices, and standard cells, hardware description languages, circuit simulation for design verification and analysis, fault diagnosis and testing.

Course Web Page: http://www.eng.auburn.edu/~nelson/courses/elec5250_6250

References:
Mentor Graphics manuals and tutorials (College of Engineering Network)


EDACafe: http://www.edacafe.com/
Chiptalk.org: http://www.chiptalk.org
Mentor Graphics: http://www.mentor.com

Instructor: Victor P. Nelson, Professor, ECE
nelsovp@auburn.edu
Office: 326 Broun Hall, (334) 844-1849

References: Links to CAD tool tutorials provided on course web page.

Course Objectives:
1. To be able to use computer-aided design tools for development of complex digital logic circuits
2. To be able to model, simulate, verify, analyze, and synthesize with hardware description languages
3. To be able to design and prototype with standard cell technology and programmable logic
4. To be able to design tests for digital logic circuits, and design for testability

Prerequisites by topic:
1. Digital logic design and analysis or switching theory
2. Computer system organization and design

Lecture Topics: Class schedule (75 minute classes)
1. ASIC design options and physical implementation options (1 class)
2. Hierarchical design concepts and CAD flow for digital ASICS (1 class)
3. Hardware description languages (1 class)
4. VHDL entities, architectures, and processes (2 classes)
5. VHDL modeling for combinational and sequential circuits (3 classes)
6. Logic synthesis from VHDL models (2 classes)
7. Design simulation for verification and analysis (3 classes)
8. Programmable logic: PLAs, PLDs, CPLDs and FPGAs (1 classes)
9. Design with standard cells (1 classes)
10. Placement and routing of standard-cell designs (2 classes)
11. Post-layout verification and simulation (3 classes)
12. Chip floor planning, placement and routing (2 classes)
13. Fault modeling and fault simulation (1 classes)
14. Design for testability (1 classes)
15. CAD tools for testing       (2 classes)  
16. Midterm exam        (1 class)  

Method for evaluating student performance:  

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<tr>
<th>Category</th>
<th>ELEC 5250</th>
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<tr>
<td>Midterm exam</td>
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<td>Final exam</td>
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<tr>
<td>Design projects</td>
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ELEC 6250 Projects:  
The final project for ELEC 6250 will require research of system design methods outside of what is 
presented in the lectures, and incorporation of those methods into the system design project.  

Design Projects (Students in ELEC 5250 and 6250 will be assigned different projects):  
Following a series of “introductory” projects, a specification-oriented design project will be an integral part of 
the course which will include design, modeling, simulation, and synthesis of VHDL into standard cells and, 
time permitting, a field programmable gate array. The design projects will include development of test 
vectors and fault simulation analysis of the test vectors and design.  
Every student is expected to do his/her own project. Discussion of various aspects of the project with 
fellow students is acceptable, provided that designs are neither collaborative nor copied.  

Computer Usage/Laboratory Projects:  
The course projects will be various elements of ASIC design, each of which will utilizing electronic design 
automation (EDA) tools from Mentor Graphics Corporation and other sources, which run on Linux servers in the 
College of Engineering network. Details about the projects and tools are available on the course web page.  

Justification for Graduate Credit in ELEC 6250: The material in this course is beyond the scope of what is 
typically presented in undergraduate electrical and computer engineering programs.  
Class attendance: Attendance is strongly encouraged, but will not be recorded or factored into the course grade.  
Policy on unannounced quizzes: There will be no unannounced “pop” quizzes.  
Accommodations: Students who need accommodations are asked to arrange a meeting during office hours the first 
week of classes, or as soon as possible if accommodations are needed immediately. If you have a conflict with 
the instructor’s office hours, an alternate time can be arranged. To set up this meeting, please contact the 
instructor by E-mail. Bring a copy of your Accommodation Memo and an Instructor Verification Form to the 
meeting. If you do not have an Accommodation Memo but need accommodations, make an appointment with 
The Program for Students with Disabilities, 1244 Haley Center, 844-2096 (V/TT).  

Academic Honesty Policy: All portions of the Auburn University student academic honesty code (Title XII) found 
in the Tiger Cub will apply to this class. All academic honesty violations or alleged violations of the SGA Code 
of Laws will be reported to the Office of the Provost, which will then refer the case to the Academic Honesty 
Committee.  

Primary student outcomes related to the course ELEC 5250:  
Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.  
Outcome 2. Ability to apply in-depth knowledge in one or more disciplines  
Outcome 3. Ability to design an electrical component or system to meet desired needs.  
Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.  

Prepared by: V. P. Nelson Date: August 19, 2014