Since this project serves as the final exam, any form of collaboration with others in the class is prohibited. This is to be an individual effort to demonstrate your knowledge of the subject. Any duplication of designs or results will be considered a violation of the Academic Honesty Code.

You are to modify your previously-designed divider circuit netlist to incorporate “full-scan” design, and then redo the block layout and related analyses. While it is up to you to provide evidence that each step of the design process has been completed properly, as a minimum, you must provide the following information:

1. Comparison of the area of the physical circuit block layout for the original design (non-scan) vs the full-scan design, i.e. determine the area penalty incurred by using scan design.

2. Comparison of the minimum clock period (related to the critical path) for the non-scan vs. the full-scan design, i.e. determine the performance penalty incurred by using scan design.

Create a report (to be submitted electronically) describing each of the design steps used to produce the above information.

For each design step in this process:

- Briefly describe what was done in that step.
- Describe how you verified the results of that step.
- Provide sufficient evidence in your report to demonstrate the correctness of that step to the reader.

A list or description of required evidence was intentionally not provided here. You are expected to be able to determine what information should be generated and examined to verify each design step.

If you feel that your divider circuit cannot be completed to do the required analyses, you may do the above with the modulo-6 counter instead, in which case the maximum grade would be ‘B’ for the final exam.