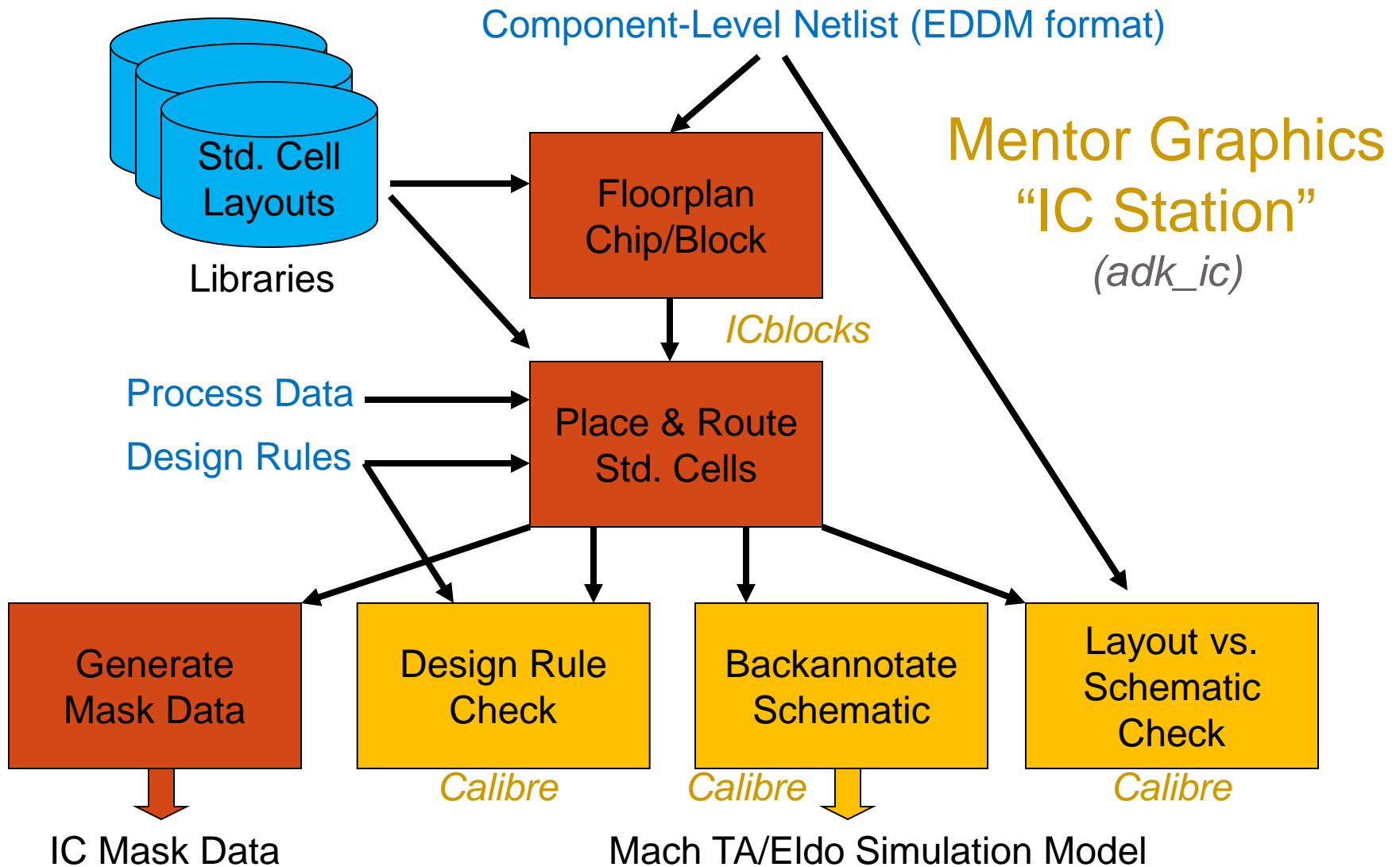


ASIC Physical Design Post-Layout Verification

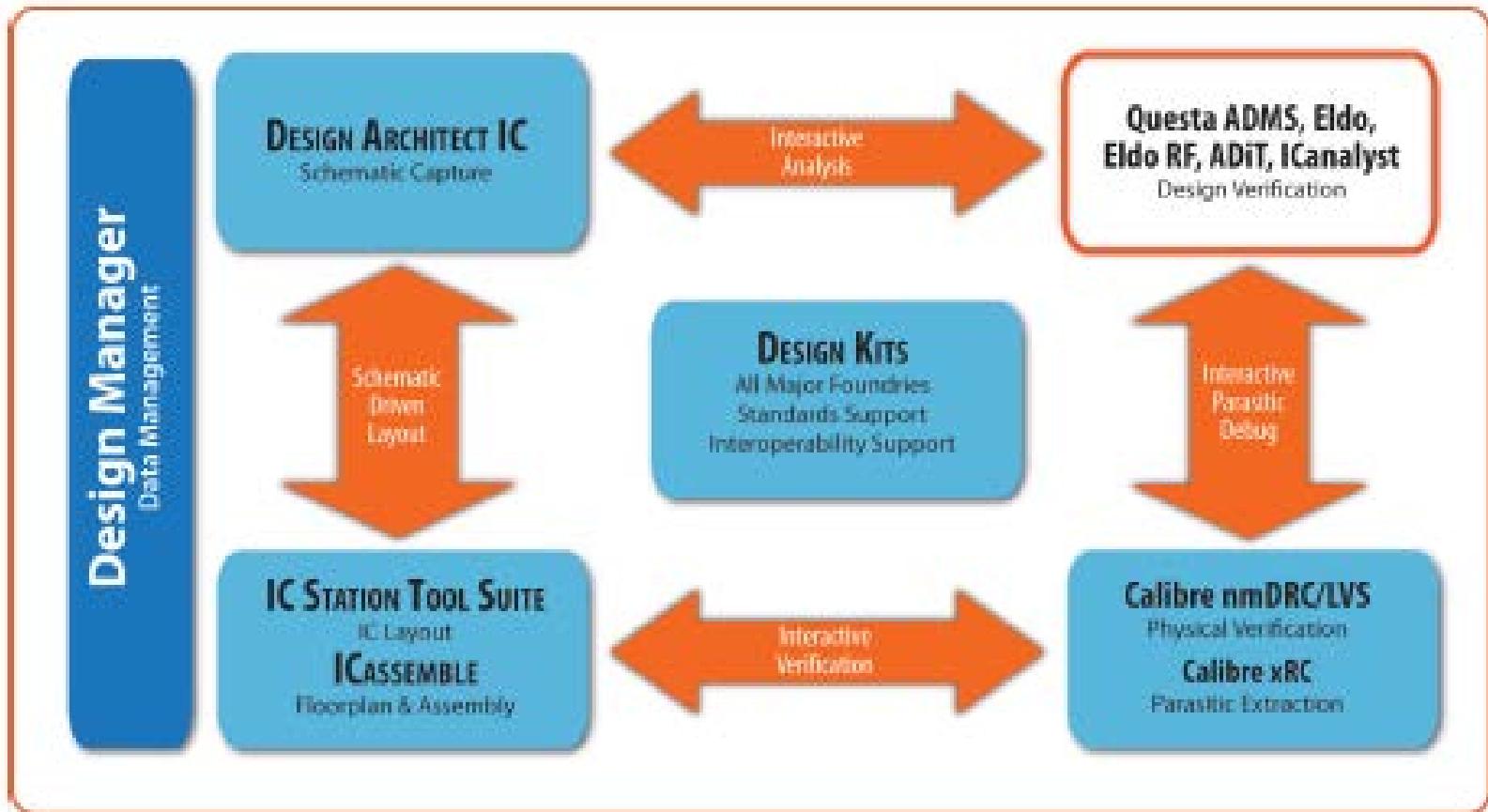
Course Web Page Reference:
[Designing Standard Cells ASICs
with the ASIC Design Kit \(ADK\)
and Mentor Graphics Tools](#)

ASIC Physical Design (Standard Cell)

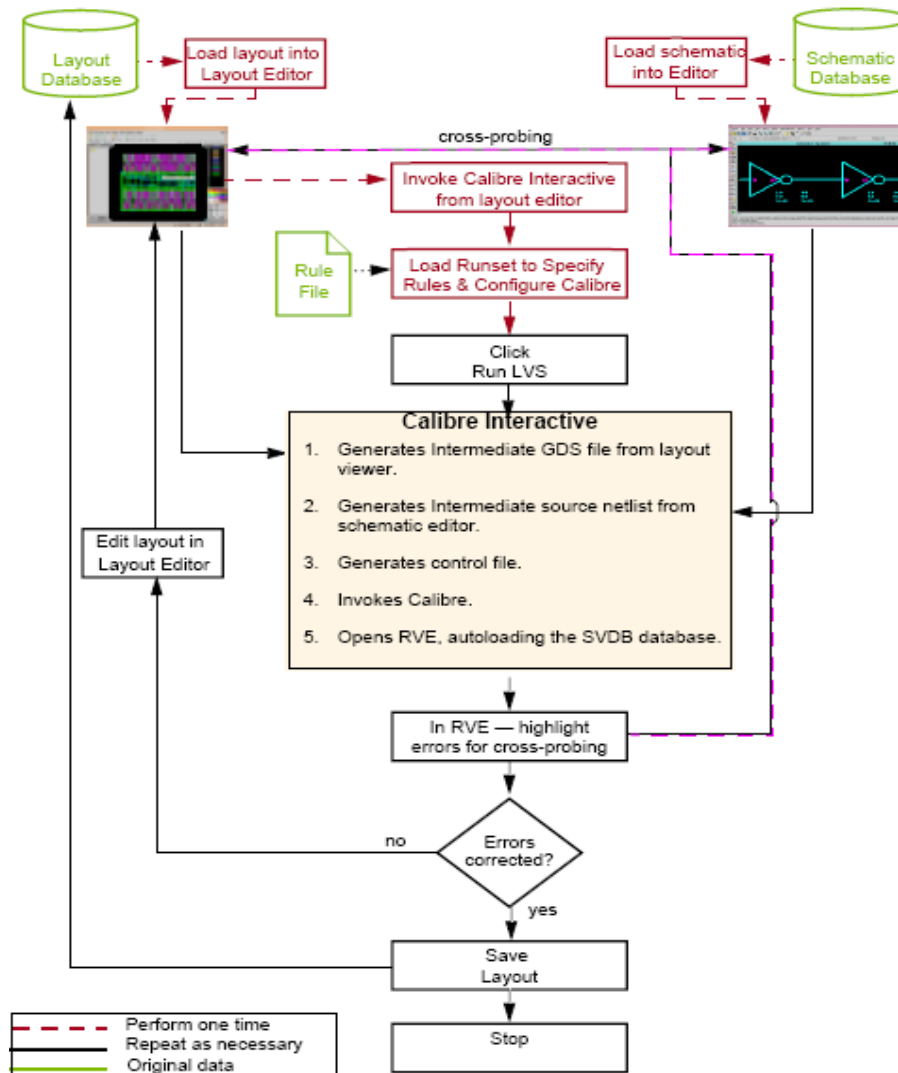
(can also do full custom layout)



Mentor Graphics Analog/Mixed-Signal IC Design Flow



Calibre Layout-vs-Schematic (LVS) Check

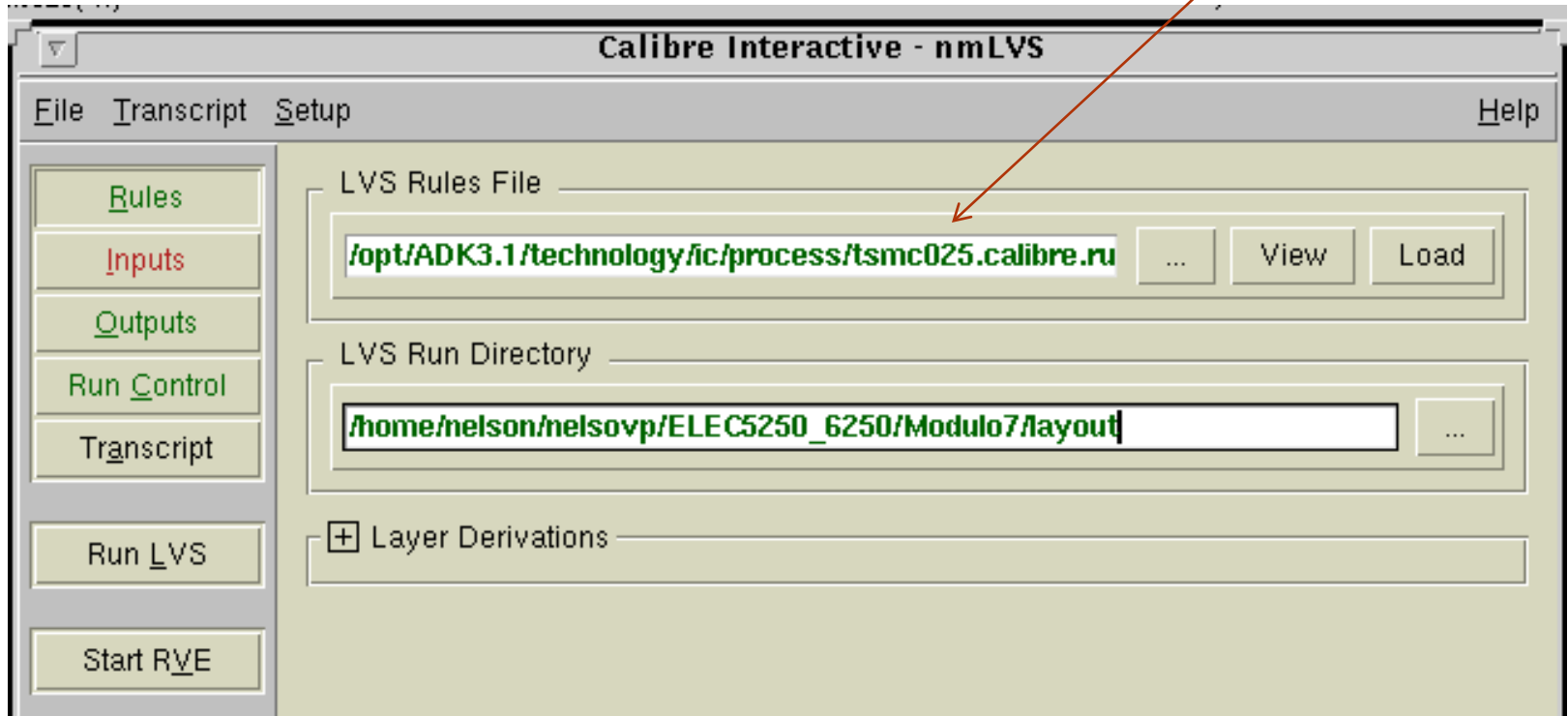


Layout vs schematic check (Calibre Interactive LVS)

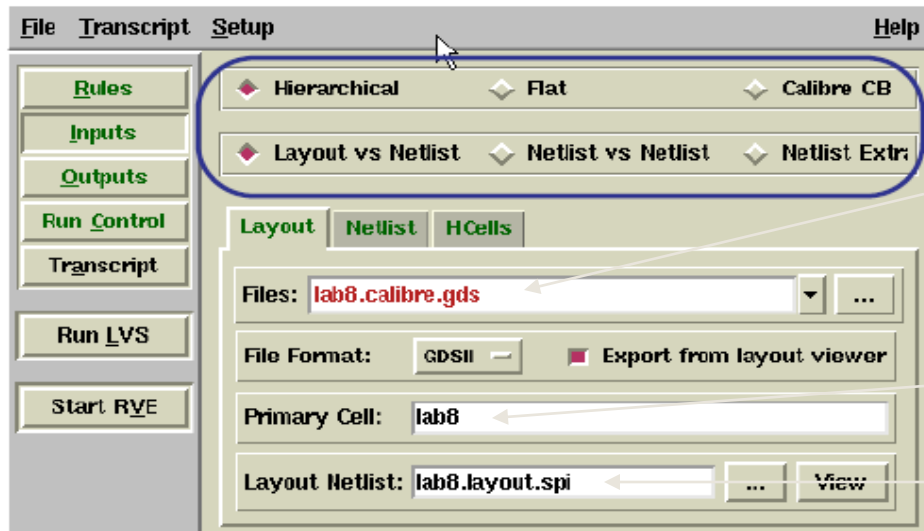
- Compares extracted transistor-level netlist vs. netlist saved in DA-IC
- From ICstation menu: *Calibre > Run LVS*
 - In popup, Calibre location: *\$MGC_CALIBRE_TREE*
 - Rules: *\$ADK/technology/ic/process/tsmc035.calibre.rules*
 - Inputs/Layout: *will be generated by Calibre*
 - Inputs/Netlist: *count4.src.net* (created in DA-IC)
 - Top-level cell: *count4* (schematic name)
 - Inputs/H-cells (hierarchical cells): *\$ADK/technology/adk.hcell*
 - Extracted file: *count4.lay.net*

Load rules file

tsmc035



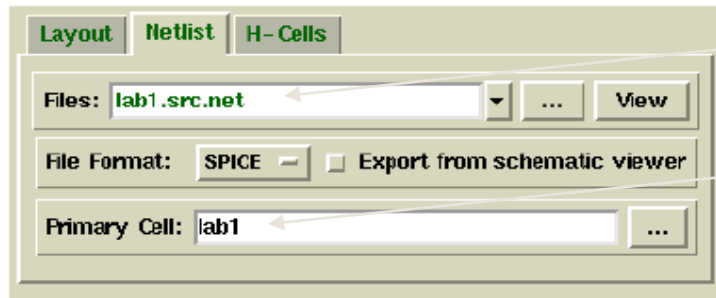
Calibre inputs



Layout to be extracted by Calibre (GDSII format)

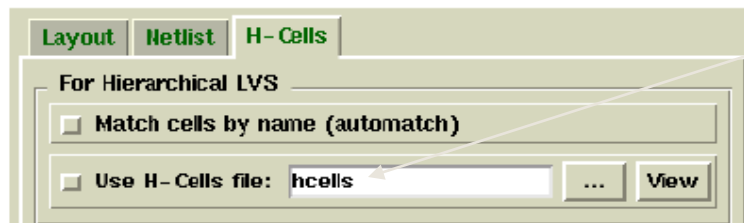
Layout top cell name

Extracted layout netlist



Source netlist created in DA-IC

Schematic name



Hierarchical cells file:

\$ADK/technology/adk.hcell

Calibre RVE to probe LVS results

Calibre - LVS RVE : svdb (lab8)

File View Layout Source Setup Help

Input Files
Rules File
Source Netlist

Output Files
Layout Netlist
Extraction Report
LVS Report

LVS Results: Designs Don't Match
a1220 / s1220 - 1 Discrepancy
Incorrect Nets - 1 Discrepancy
Discrepancy #1
a1230 / s1230
a1240 / s1240
a1310 / s1310
a1620 / s1620
a1720 / s1720

Expand the results tree to display individual discrepancies.

Click a discrepancy to display information.

a1220 / s1220: Discrepancy #1 - Incorrect Nets

LAYOUT NAME	ne	SOURCE NAME
Net		

Query Cell: lab8

Cells

- lab0
- a1220
- s1230
- a1240
- s1310
- s1620
- s1720
- s2311
- s3500

Double-click a net or instance name to highlight in a layout viewer.

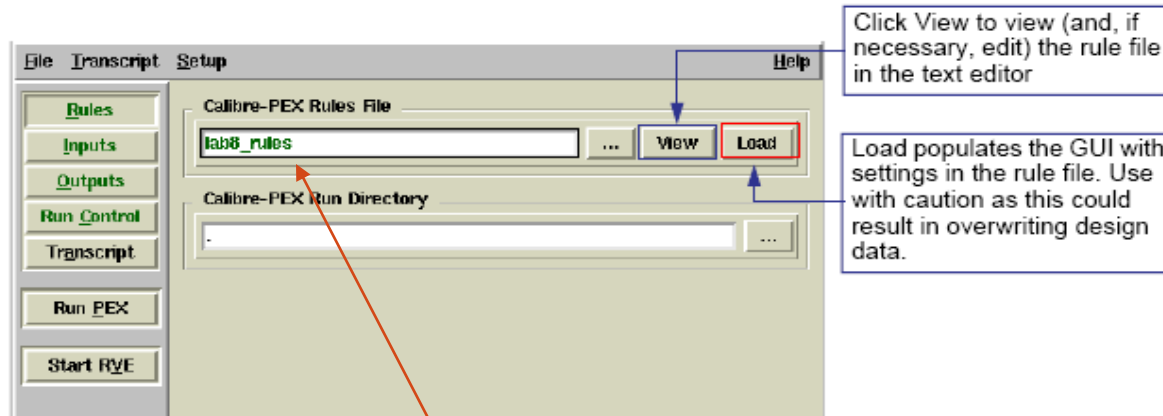
Post-layout functional/timing verification (Calibre PEX)

- Purpose: timing analysis & functional verification of the final design
 - analyze netlist extracted from layout
 - includes resistance, parasitic capacitance & coupling capacitance
 - perform netlist & parameter extraction with *Calibre PEX*
 - perform simulation in *ADiT, Eldo, Pspice, HSPICE, etc.*

Parameter extraction with Calibre PEX

- Extracts SPICE netlist, including parasitic RC
 - *Transistor-level*, gate-level, or hierarchical extraction
- In IC Station, with the layout cell open:
 - In the menu bar: *Calibre>Run PEX*
 - Input options: *similar to Calibre LVS*
 - Extraction options (Outputs tab):
 - choose *“Transistor level”*
 - choose one of:
 - *C: lumped C + coupling cap’s*
 - *RC: distributed RC*
 - *RCC: distributed RC + coupling cap’s*
 - Click *“Run PEX”*
 - Output file: *count4.pex.netlist*

Calibre PEX inputs



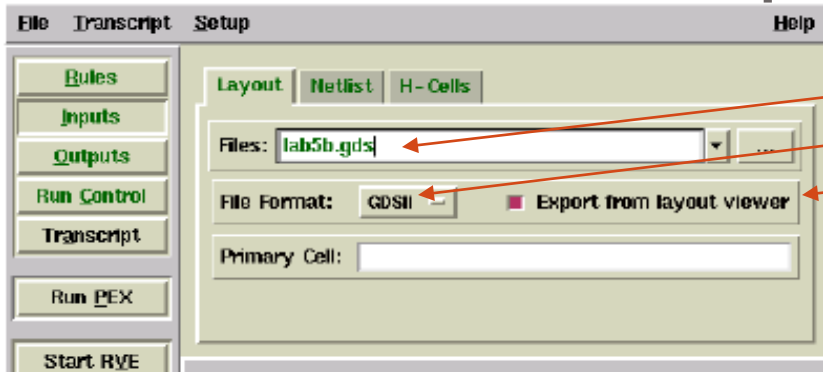
Click View to view (and, if necessary, edit) the rule file in the text editor

Load populates the GUI with settings in the rule file. Use with caution as this could result in overwriting design data.

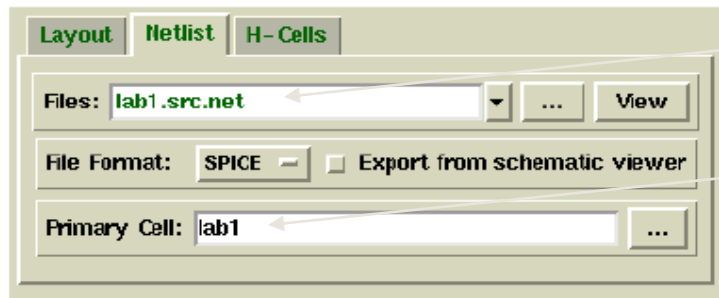
Specify rules file:

`$ADK/technology/ic/process/tsmc035.calibre.rules`

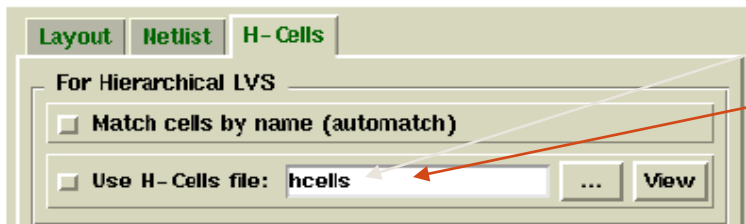
Calibre PEX inputs



- Name of layout file (count4.gds)
- GDSII file format
- Check to generate new layout file
- Name of top cell (count4)

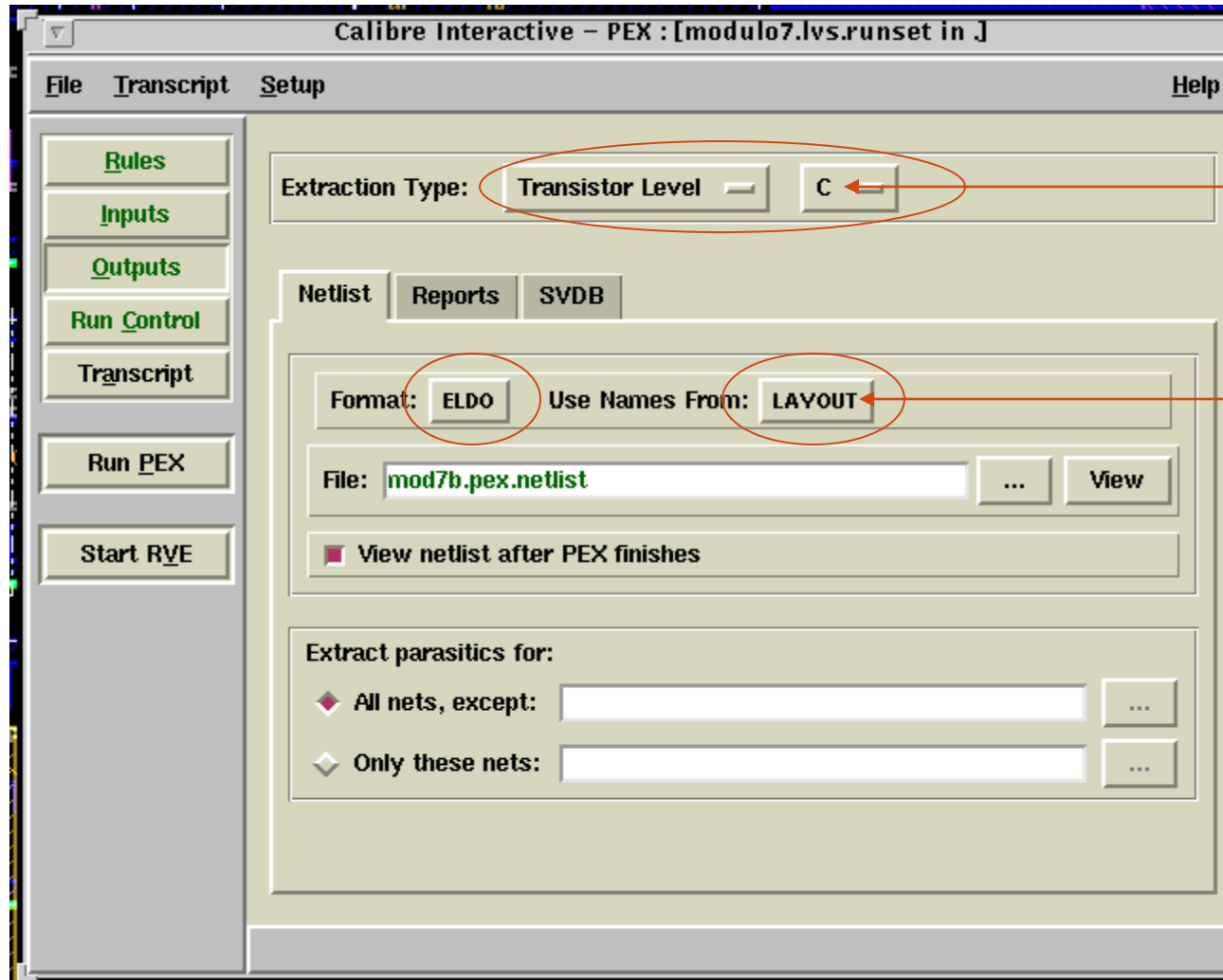


- Source(SPICE) netlist created in DA-IC
- Top-level cell name in SPICE netlist



- Hierarchical cells file:
\$ADK/technology/adk.hcell

Calibre PEX netlist output



Lumped capacitance

Use net names from LAYOUT