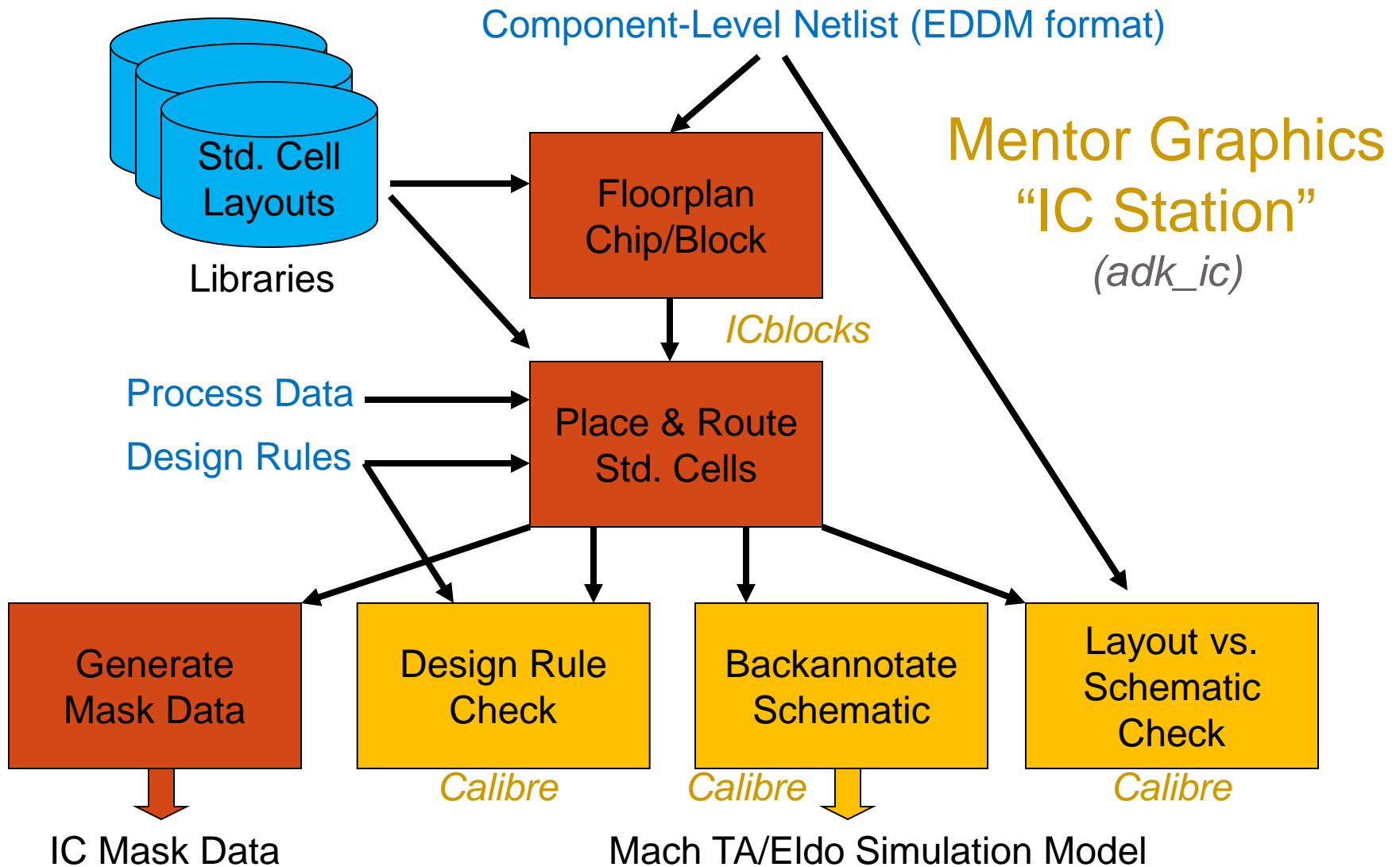


# ASIC Physical Design Standard-Cell Design Flow

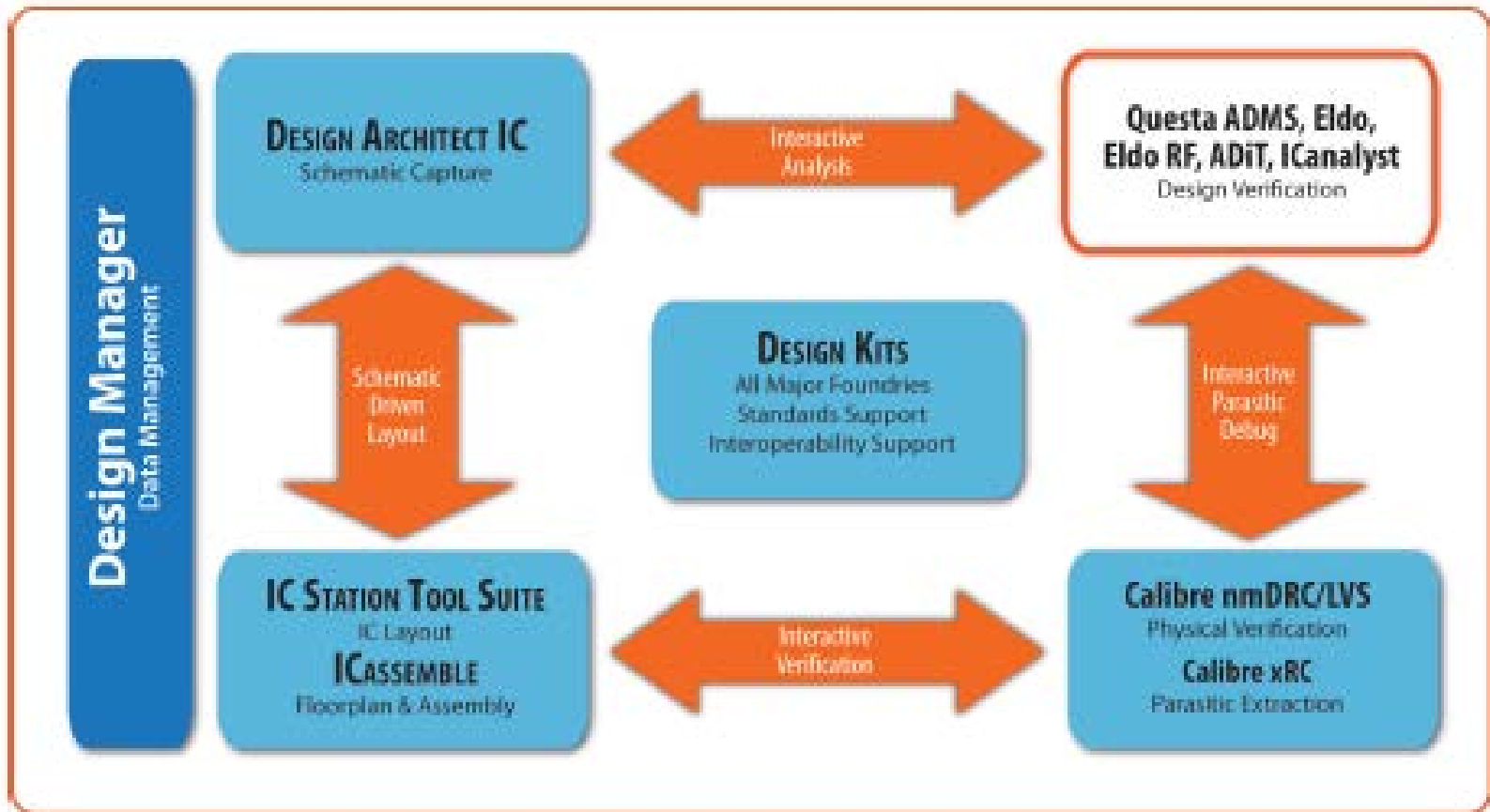
Course Web Page Reference: [Designing Standard Cells ASICs with the ASIC Design Kit \(ADK\) and Mentor Graphics Tools](#)

# ASIC Physical Design (Standard Cell)

(can also do full custom layout)



# Mentor Graphics Analog/Mixed-Signal IC Design Flow



# ASIC CAD tools available in ECE

- Modeling and Simulation
  - Questa ADMS = Questa+Modelsim+Eldo+ADiT (Mentor Graphics)
  - Verilog-XL, NC\_Verilog, Spectre (Cadence)
- Design Synthesis (digital)
  - Leonardo Spectrum (Mentor Graphics)
  - Design Compiler (Synopsys), RTL Compiler (Cadence)
- Design for Test and Automatic Test Pattern Generation
  - Tessent DFT Advisor, Fastscan, SoCScan (Mentor Graphics)
- Schematic Capture & Design Integration
  - Design Architect-IC (Mentor Graphics)
  - Design Framework II (DFII) - Composer (Cadence)
- Physical Layout
  - IC Station (Mentor Graphics)
  - SOC Encounter, Virtuoso (Cadence)
- Design Verification
  - Calibre DRC, LVS, PEX (Mentor Graphics)
  - Diva, Assura (Cadence)

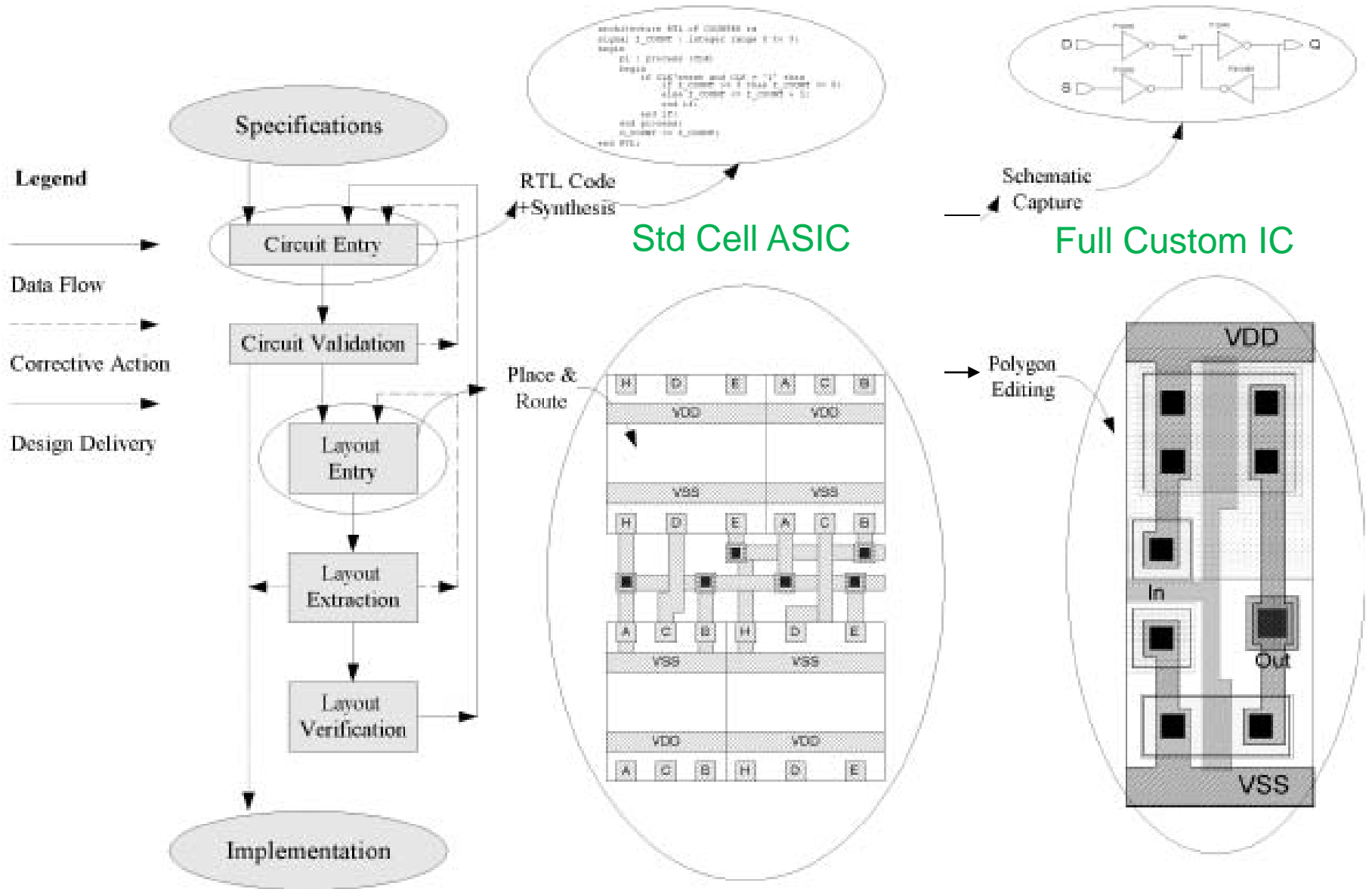
# Mentor Graphics ASIC Design Kit (ADK)

We also have ADK's for Cadence tools for several technologies

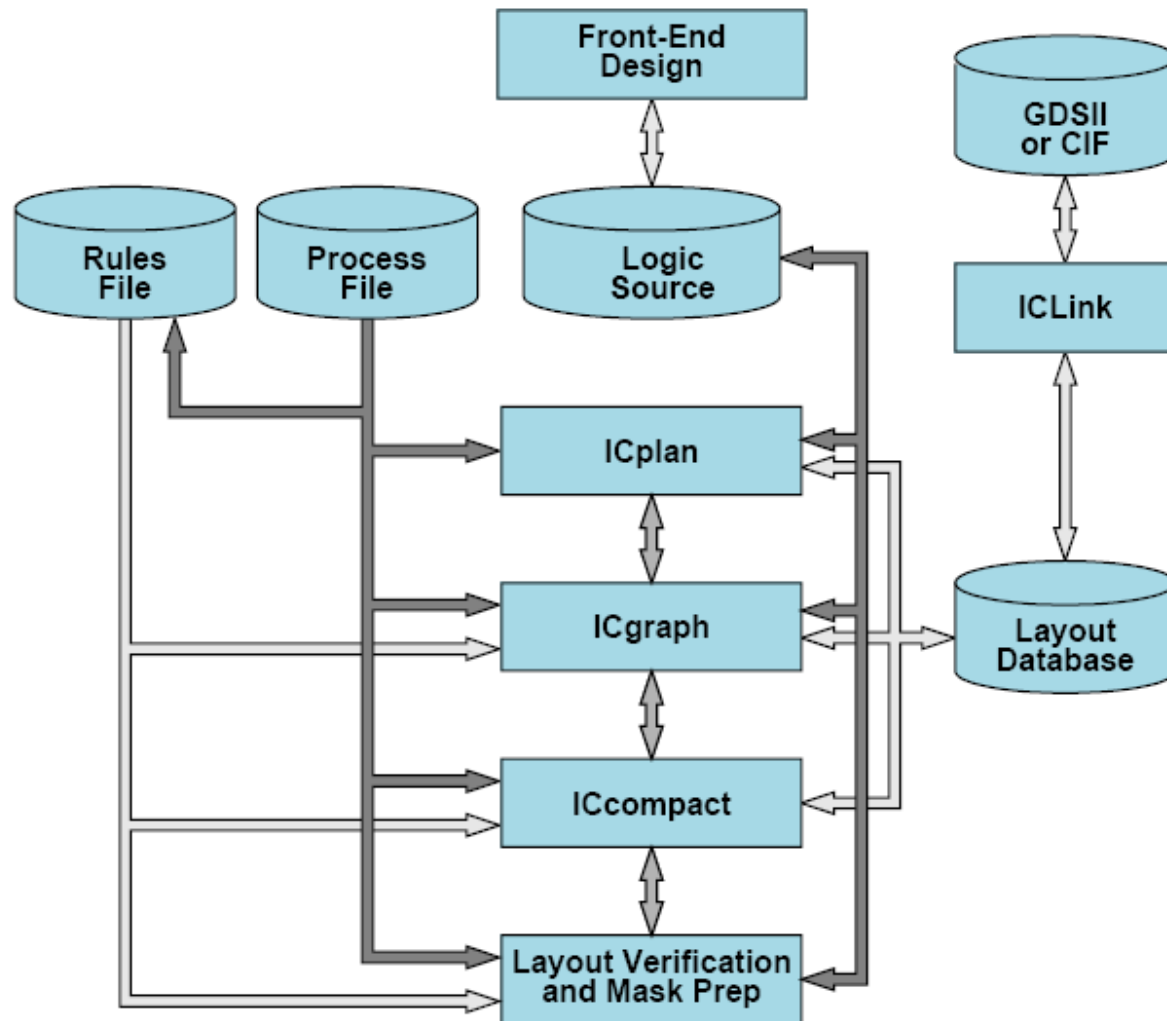
- Technology files & standard cell libraries
  - AMI: ami12, ami05 (1.2, 0.5  $\mu\text{m}$ )
  - TSMC: tsmc035, tsmc025, tsmc018 (0.35, 0.25\*\*, 0.18  $\mu\text{m}$ ) \*\*also have VT Cadence lib
  - *Current MOSIS Instructional: IBM 180nm CMOS (7RF), ON Semi 0.5um CMOS*
  - *Current MOSIS Unfunded Research: IBM 130nm CMOS (8RF), 130nm SiGE BiCMOS(8HP)*
- IC flow & DFT tool support files:
  - Simulation models
    - VHDL/Verilog/Mixed-Signal models (*Modelsim SE/ Questa ADMS*)
    - Analog (SPICE) models (*Eldo, ADiT*)
    - \*Post-layout timing (*Mach TA*) \* *obsolete: Mach TA replaced by ADiT*
    - \*Digital schematic (*Quicksim II, Quicksim Pro*) \* *obsolete: HDL or Eldo now used*
  - Standard cell synthesis libraries (*LeonardoSpectrum*)
  - Design for test & ATPG libraries (*DFT Advisor, Fastscan*)
  - Schematic capture (*Design Architect-IC*)
  - IC physical design (standard cell & custom)
    - Standard cell models, symbols, layouts (*IC Station*)
    - Design rule check, layout vs schematic, parameter extraction (*Calibre*)

# Automated ASIC Design Flow

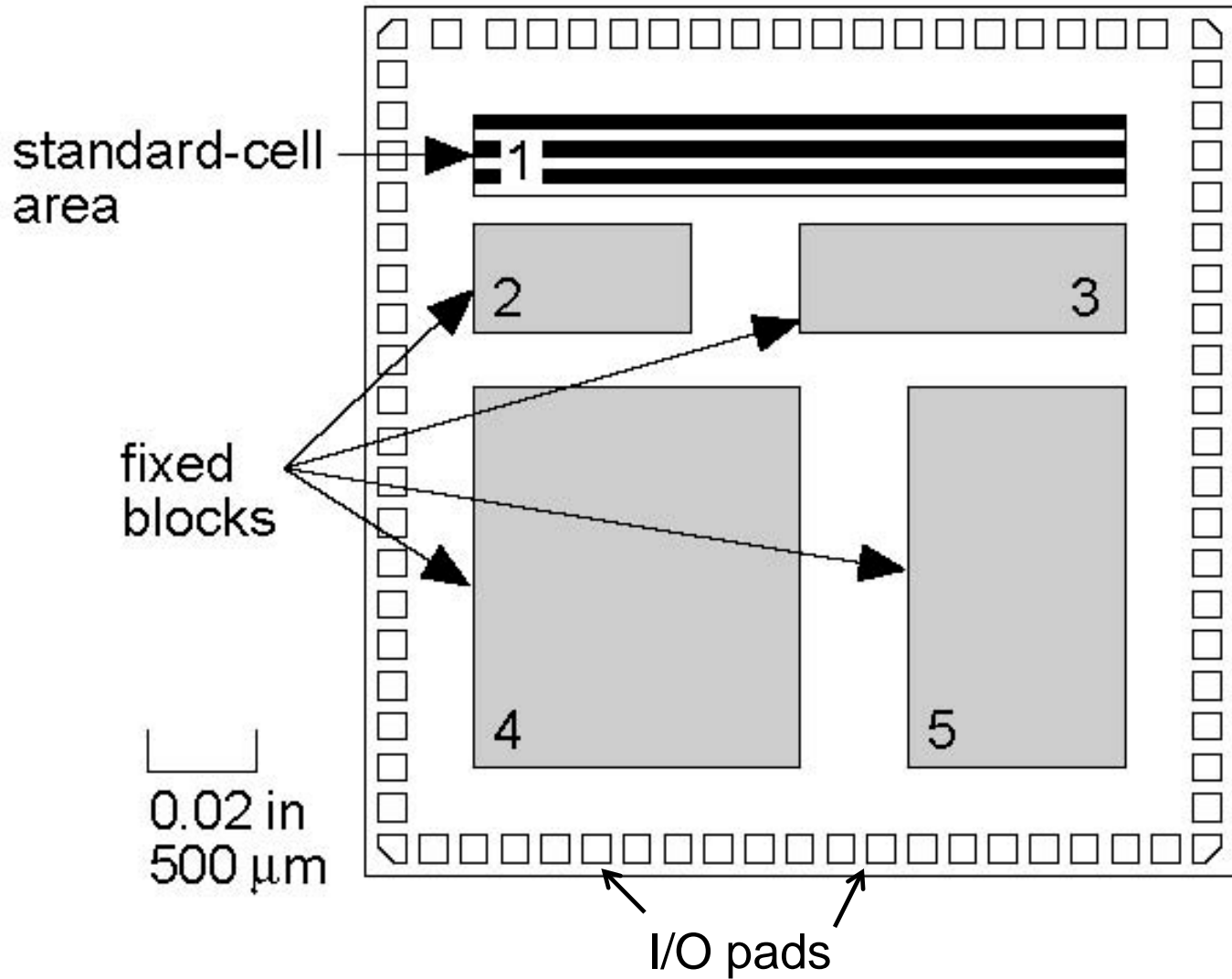
Source: CMOS IC Layout, Dan Clein



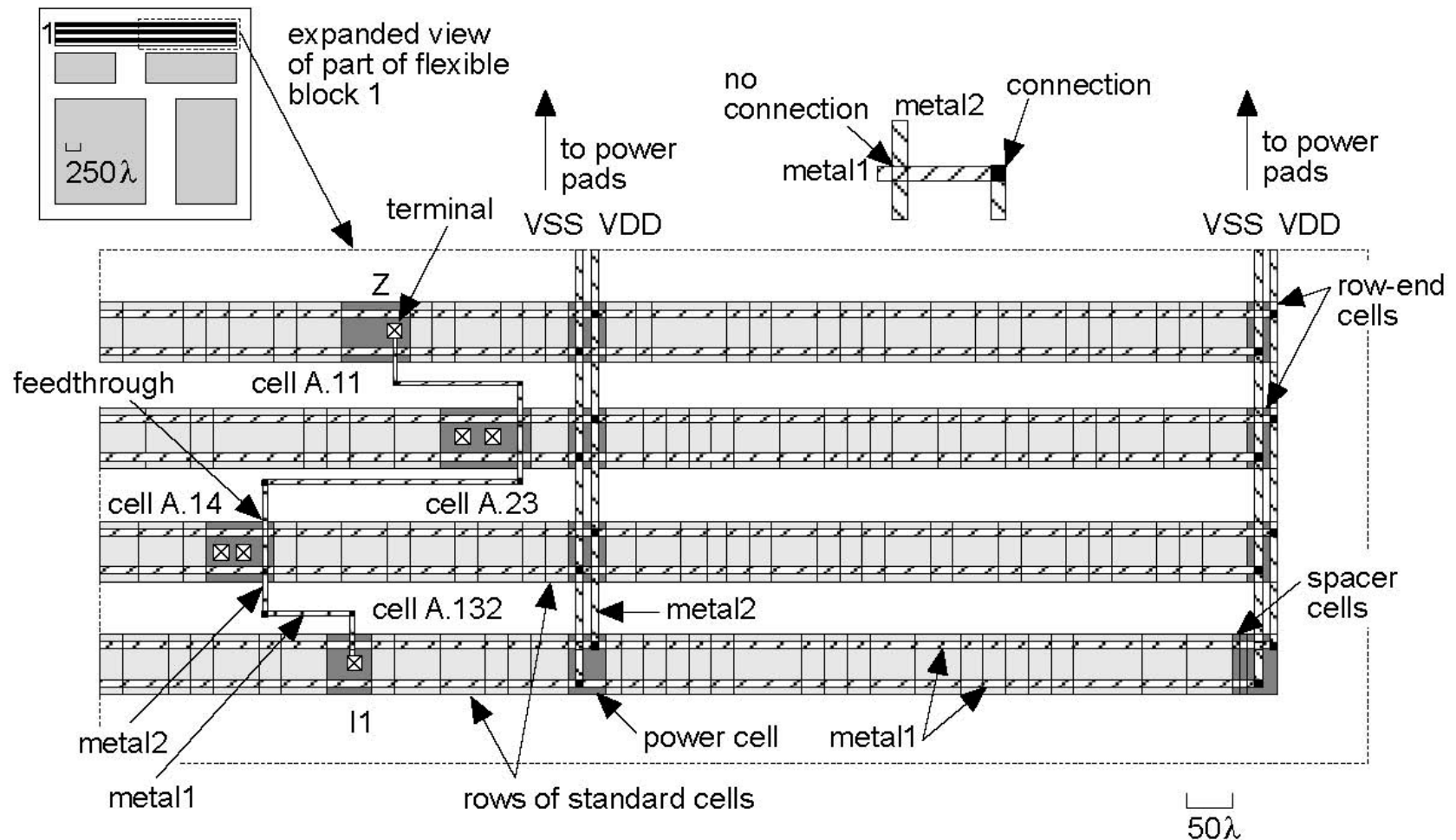
# IC Station full-custom design flow



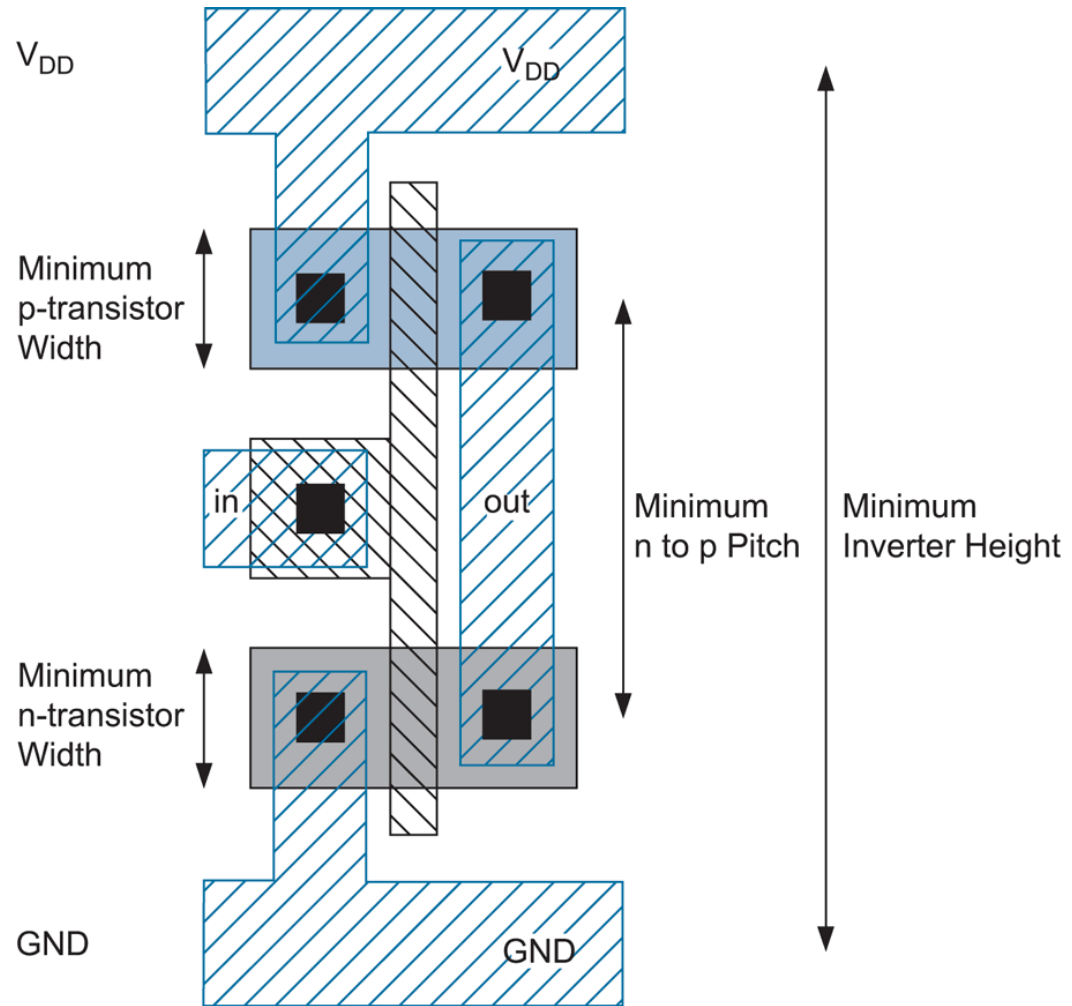
# Cell-Based IC



# Cell-Based Block

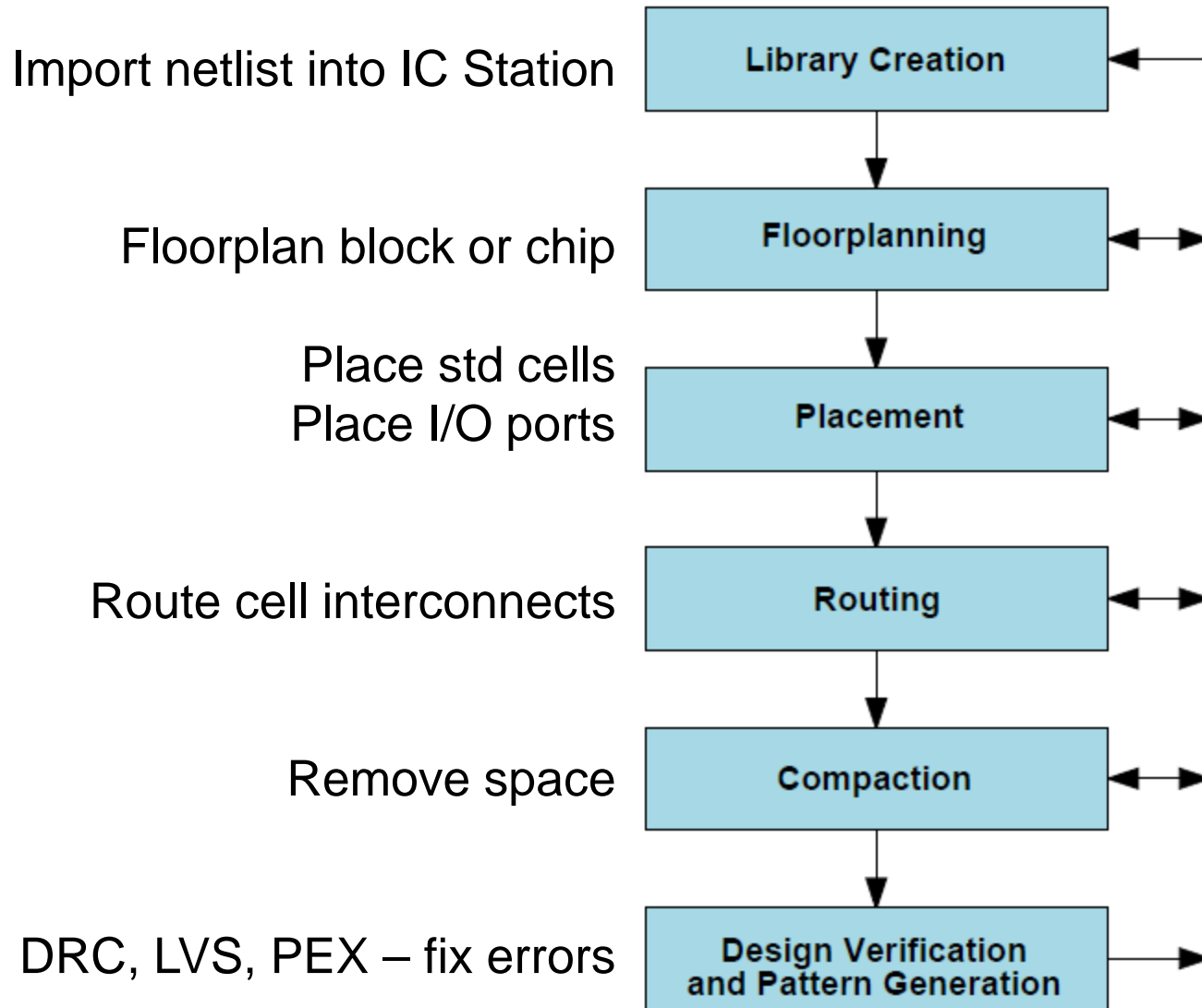


# Basic standard Cell layout



**FIG 3.30** Minimum inverter height

# Automated Layout Design Flow in IC Station



# Preparation for Layout

1. Use Design Architect-IC to convert Verilog netlist to Mentor Graphics EDDM netlist format
  - Invoke Design Architect-IC (*adk\_daic*)
  - On menu bar, select *File > Import Verilog*
    - Netlist file: *count4.v* (*the Verilog netlist*)
    - Output directory: *count4* (for the EDDM netlist)
    - Mapping file *\$ADK/technology/adk\_map.vmp*
2. Open the generated schematic for viewing
  - Click *Schematic* in DA-IC palette
  - Select schematic in directory named above (*see next slide*)
  - Click *Update LVS* in the schematic palette to create a netlist to be used later by “Calibre”
3. Create design viewpoints for ICstation tools
  - *adk\_dve count4 -t tsmc035* (V.P's: layout, lvs, sdl, tsmc035)

Can also create gate/transistor schematics directly in DA-IC using components from the ADK library

# DA-IC generated schematic

The screenshot displays the Design Architect-IC v2004.3\_1.1 software interface. The main window shows a schematic diagram for a 4-bit counter, titled "Schematic#2 count4 sheet1". The schematic is composed of several logic gates and flip-flops. On the left, there are three input signals: "clear", "clock", and "enable". The circuit includes four D-type flip-flops, each with a "R" (Reset) input, a "CLK" (Clock) input, and a "D" (Data) input. The flip-flops are connected to a network of logic gates, including AND gates (labeled "i x 31", "i x 110", "i x 100", "i x 101", "i x 102", "i x 103", "i x 104", "i x 105", "i x 106", "i x 107", "i x 108", "i x 109", "i x 110", "i x 111", "i x 112", "i x 113", "i x 114", "i x 115", "i x 116", "i x 117", "i x 118", "i x 119", "i x 120", "i x 121", "i x 122", "i x 123", "i x 124", "i x 125", "i x 126", "i x 127", "i x 128", "i x 129", "i x 130", "i x 131", "i x 132", "i x 133", "i x 134", "i x 135", "i x 136", "i x 137", "i x 138", "i x 139", "i x 140", "i x 141", "i x 142", "i x 143", "i x 144", "i x 145", "i x 146", "i x 147", "i x 148", "i x 149", "i x 150", "i x 151", "i x 152", "i x 153", "i x 154", "i x 155", "i x 156", "i x 157", "i x 158", "i x 159", "i x 160", "i x 161", "i x 162", "i x 163", "i x 164", "i x 165", "i x 166", "i x 167", "i x 168", "i x 169", "i x 170", "i x 171", "i x 172", "i x 173", "i x 174", "i x 175", "i x 176", "i x 177", "i x 178", "i x 179", "i x 180", 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"i x 1000".

The right-hand panel contains a "schematic edit" menu with the following options:

- Session
- Library
- ADK IC Library
- Simulation
- Prep for Layout
- Update LVS
- Edit
- Draw
- Text
- Check & Save
- Select
- By Property
- Unselect All
- Edit
- Move
- Copy
- Delete
- Undo
- Flip
- Rotate
- Properties
- Add
- Instance
- Wire
- Bus/Bundle
- Port
- Add Source
- Property
- Name
- Instance
- Net
- Model Registration
- Choose adms.ini File
- Choose Library

At the bottom of the window, there are three notes:

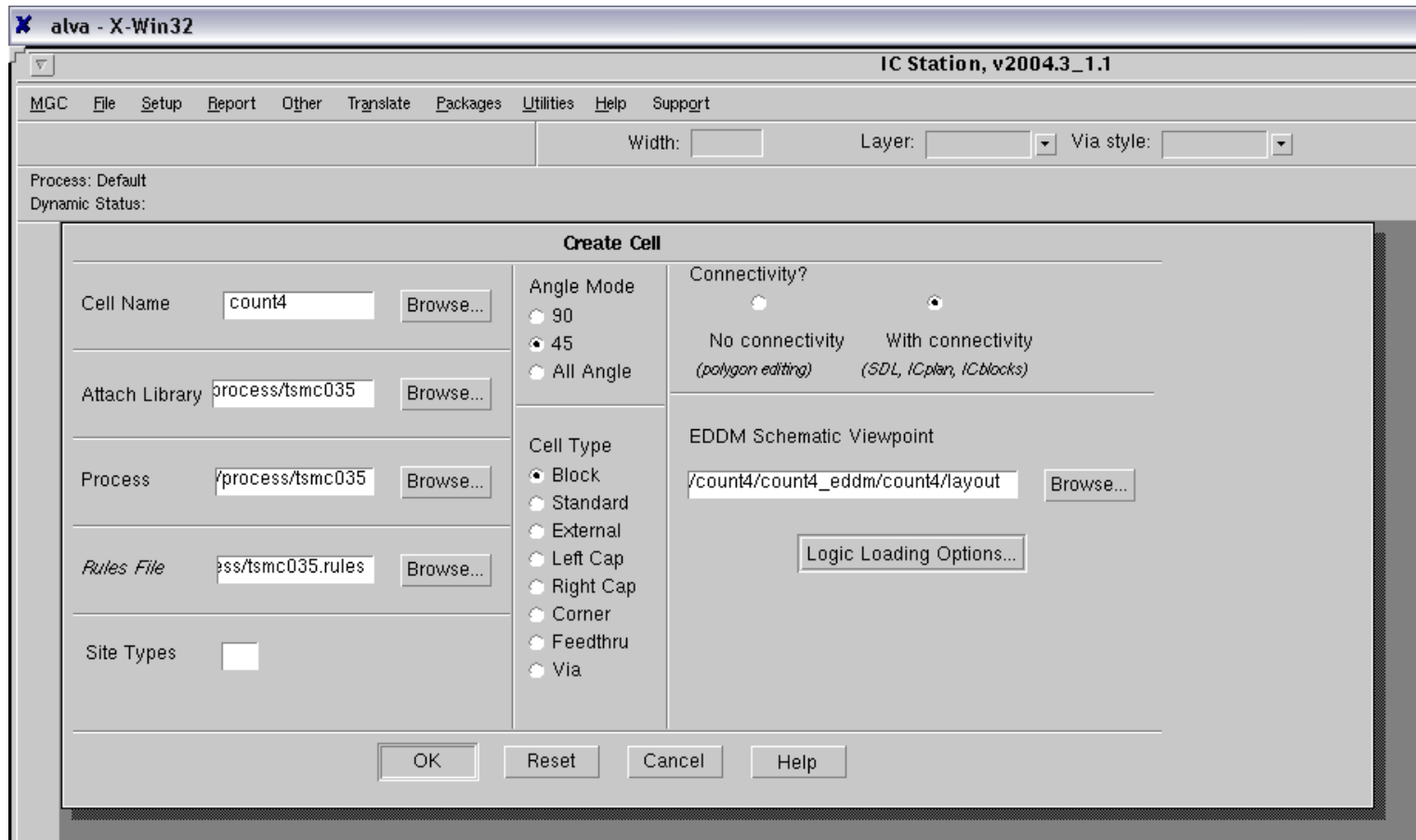
- Note : apptmentor/ICFlow2004.3/tmp/loc\_map\_script\_642370 will support soft names in simulation commands
- Note : Writing LVS netlist, please wait.
- Note : Netlist completed successfully.

The taskbar at the bottom shows the following applications: start, Novell GroupWise - M..., Mentor Presentation, Microsoft PowerPoint ..., alva - X-Win32, and a system clock showing 3:07 PM.

# Create a std-cell based logic block in IC Station

- Invoke: *adk\_ic*
- In IC Station palette, select: *Create Cell*
  - Cell name: *count4*
  - Attach library: *\$ADK/technology/ic/process/tsmc035*
  - Process: *\$ADK/technology/ic/process/tsmc035*
  - Rules file: *\$ADK/technology/ic/process/tsmc035.rules*
  - Angle mode: *45*
  - Cell type: *block*
  - Select *With connectivity*
  - EDDM schematic viewpoint: *count4/layout*
  - Logic loading options: *flat*

# Create Cell dialog box



# Floorplanning (Text chap. 15, 16)

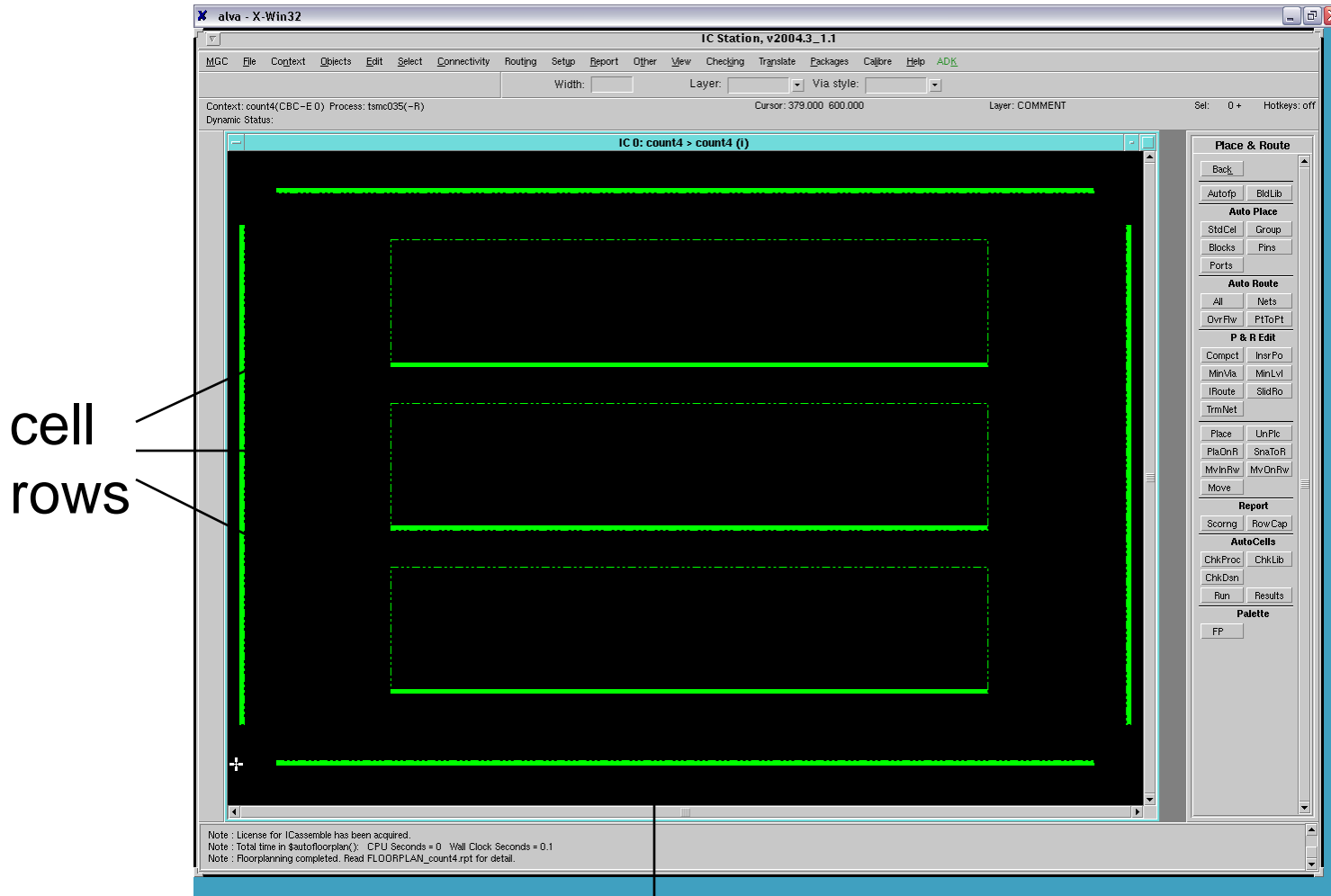
- Floorplanning: arrange major blocks prior to detailed layout to minimize chip area
  - input is a netlist of circuit blocks (hierarchical)
  - estimate layout areas, shapes, etc.
  - do initial placement of blocks (keep highly-connected blocks close)
  - decide location of I/O pads, power, clock

# Autofloorplan options

- Aspect ratio – defines block shape
- Max dimensions
- #Rows – specify or automatic
- Edge gaps – between core & external rows (for pins, etc.)
- Route area ratio – vertical space between rows
- Internal row layout – can “flip bottom”

# Auto-floorplan the block with *ICplan*

*place & route > autofp*

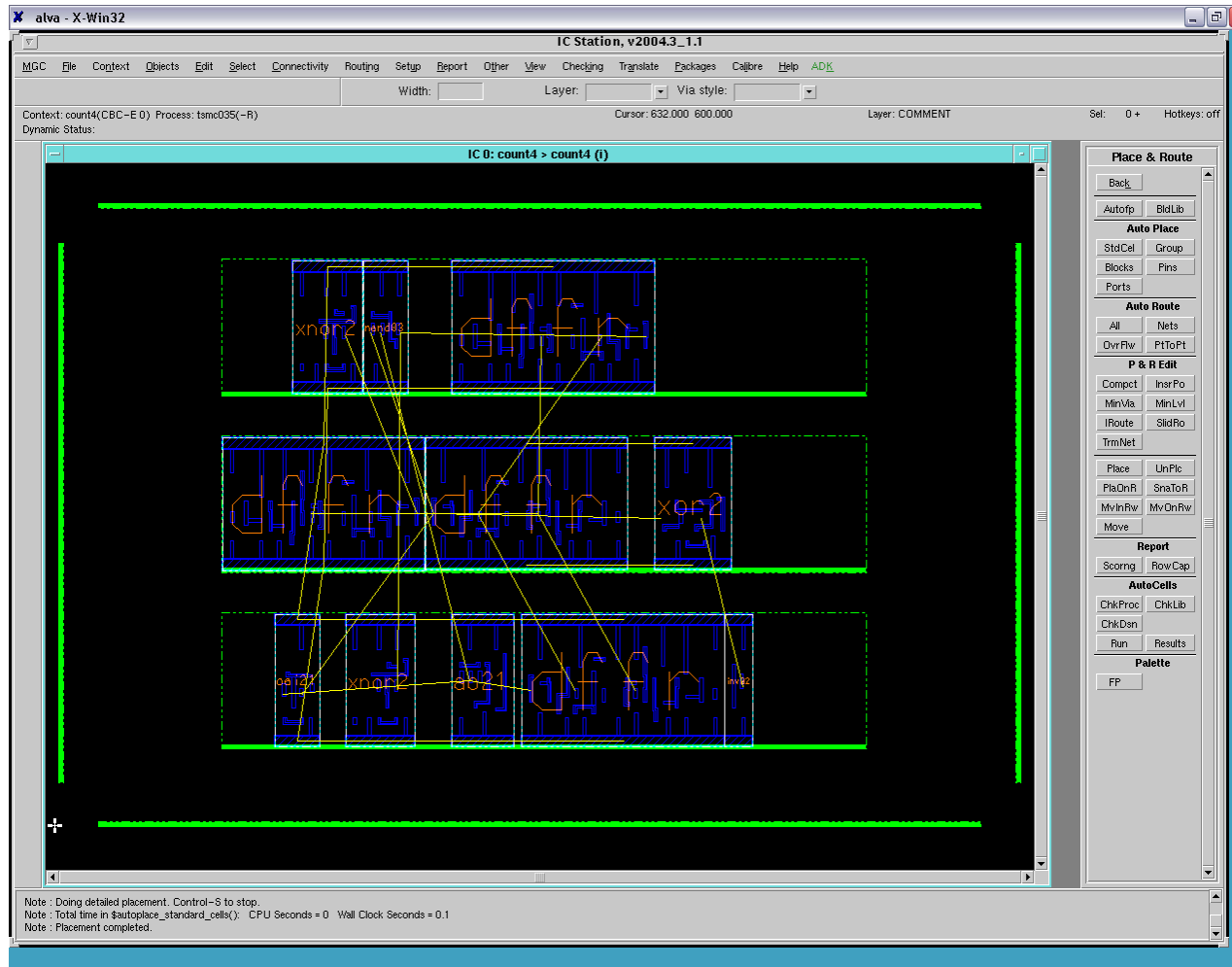


cell  
rows

cell boundary

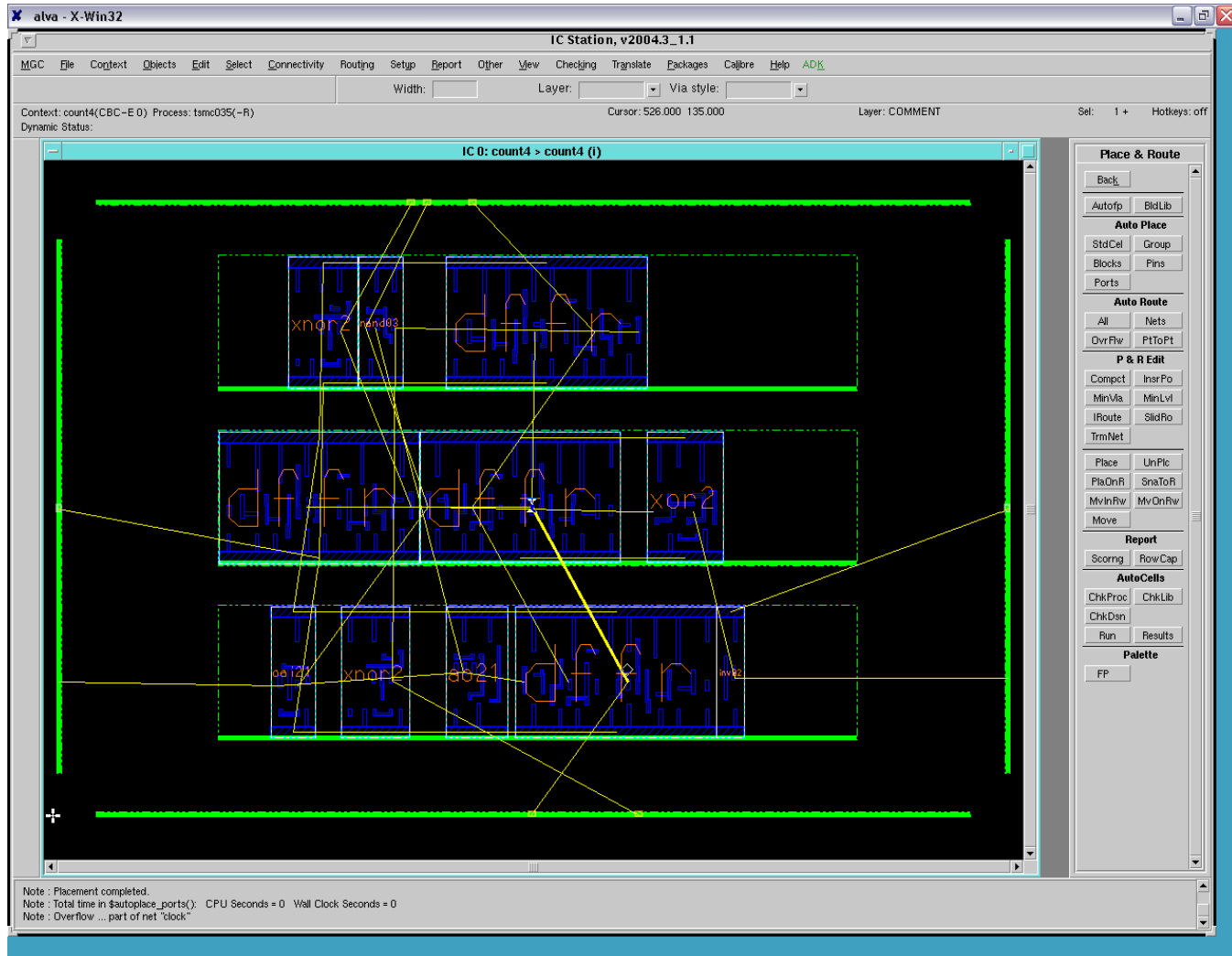
# Auto-place the std cells

## *Autoplac > StdCel*



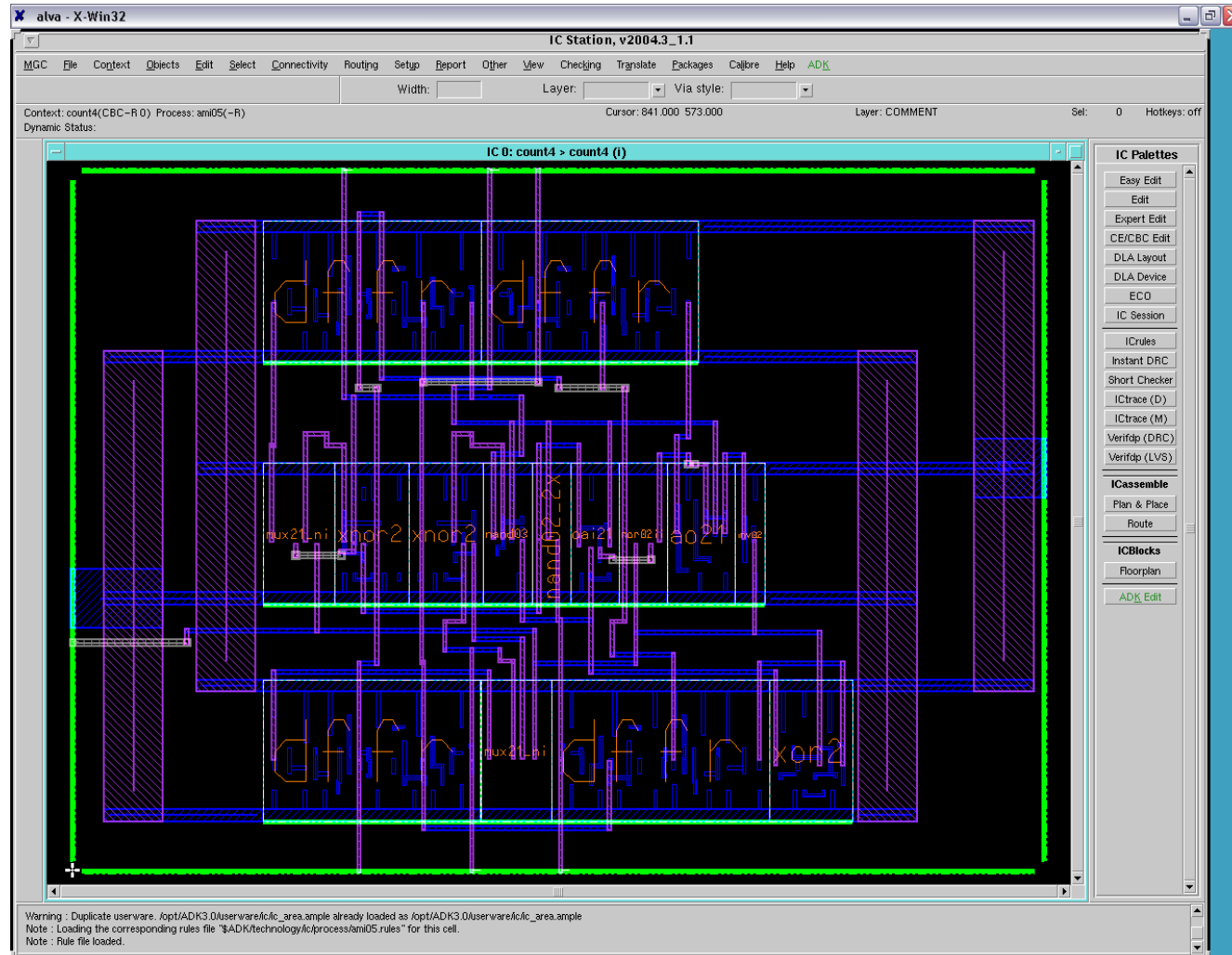
# Auto-place ports (signal connections on cell boundaries)

## *Autoplac > Ports*

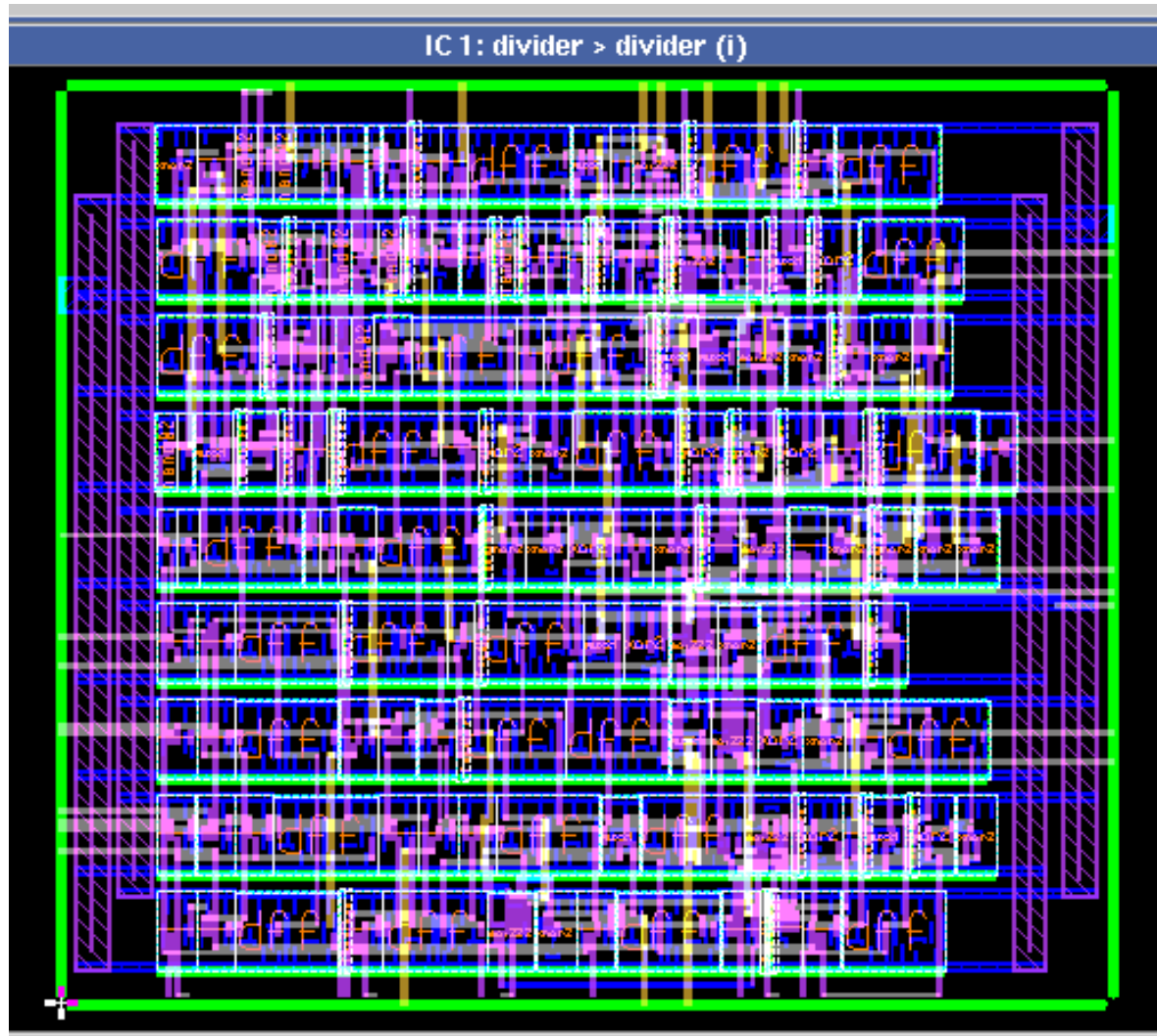


# AutoRoute all nets (hand-route unrouted “overflows”)

Then: *Add > Port Text* to copy port names from schematic – for Calibre



# 16 by 8 divider circuit



# Layout design rule check (DRC)

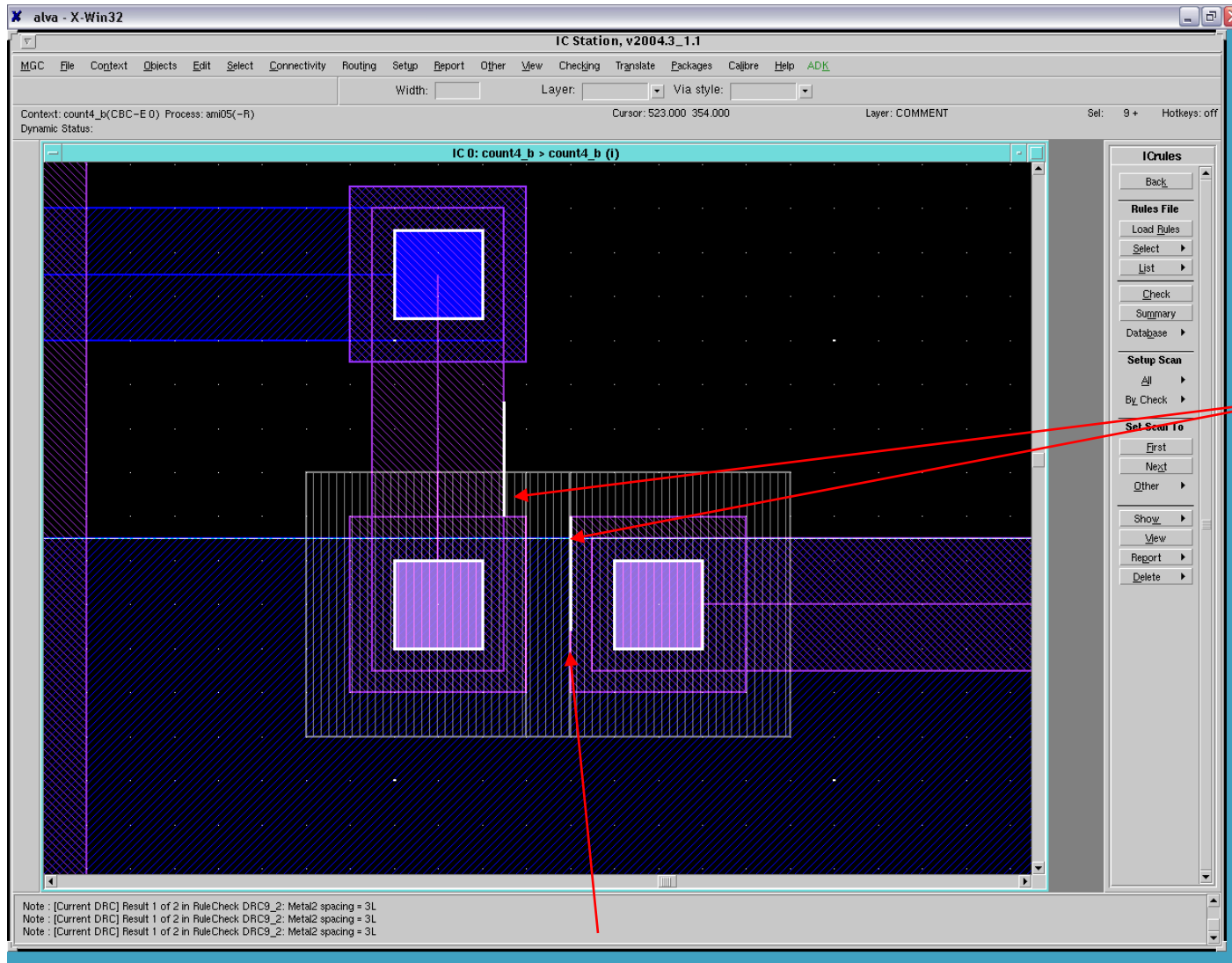
- Technology-specific design rules specify minimum sizes, spacing, etc. of features to ensure reliable fabrication
  - Design rules file specified at startup  
Ex. *tsmc035.rules*
- From main palette, select ICrules
  - Click *Check* and then *OK* in prompt box  
(can optionally select a specific area to check)
  - Rules checked in numeric order

# Common errors detected by DRC

- To fix, click on *First* in palette to highlight first error
  - Error is highlighted in the layout
  - Click *View* to zoom in to the error (see next)
  - Example: DRC9\_2: Metal2 spacing = 3L
  - Fix by drawing a rectangle of metal2 to fill in the gap between contacts that should be connected
- Click *Next* to go to next error, until all are fixed

**NOTE:** The layout must be free of DRC errors if MOSIS is to fabricate the chip; they will run their own DRC.

# Sample error: DRC9\_2 metal2 spacing = 3L



Draw rectangle of metal2 to fill gap

It also called contact-to-contact metal 2 spacing DRC9\_2 error