

# ASIC Physical Design CMOS Processes

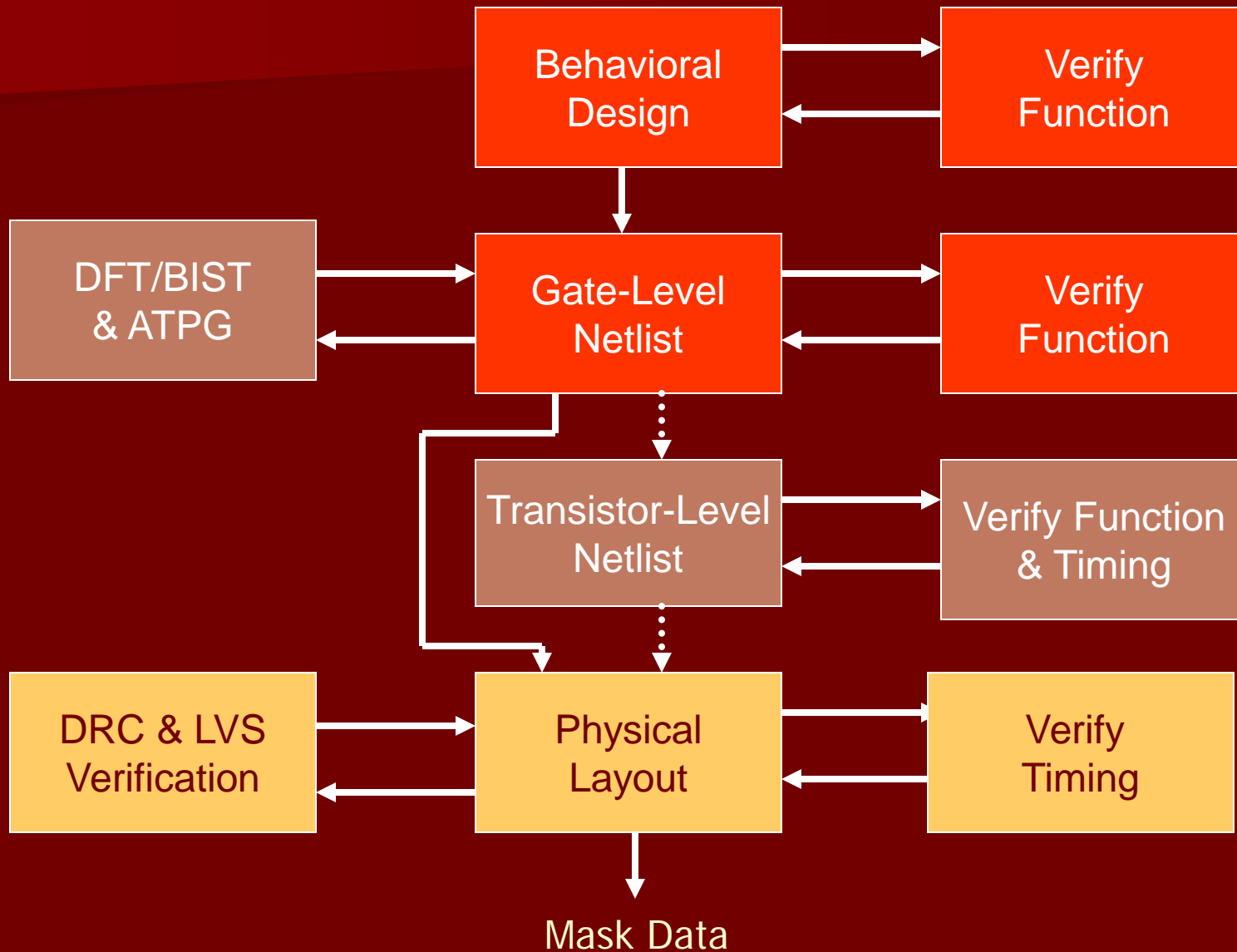
Smith Text: Chapters 2 & 3

Weste – “CMOS VLSI Design”

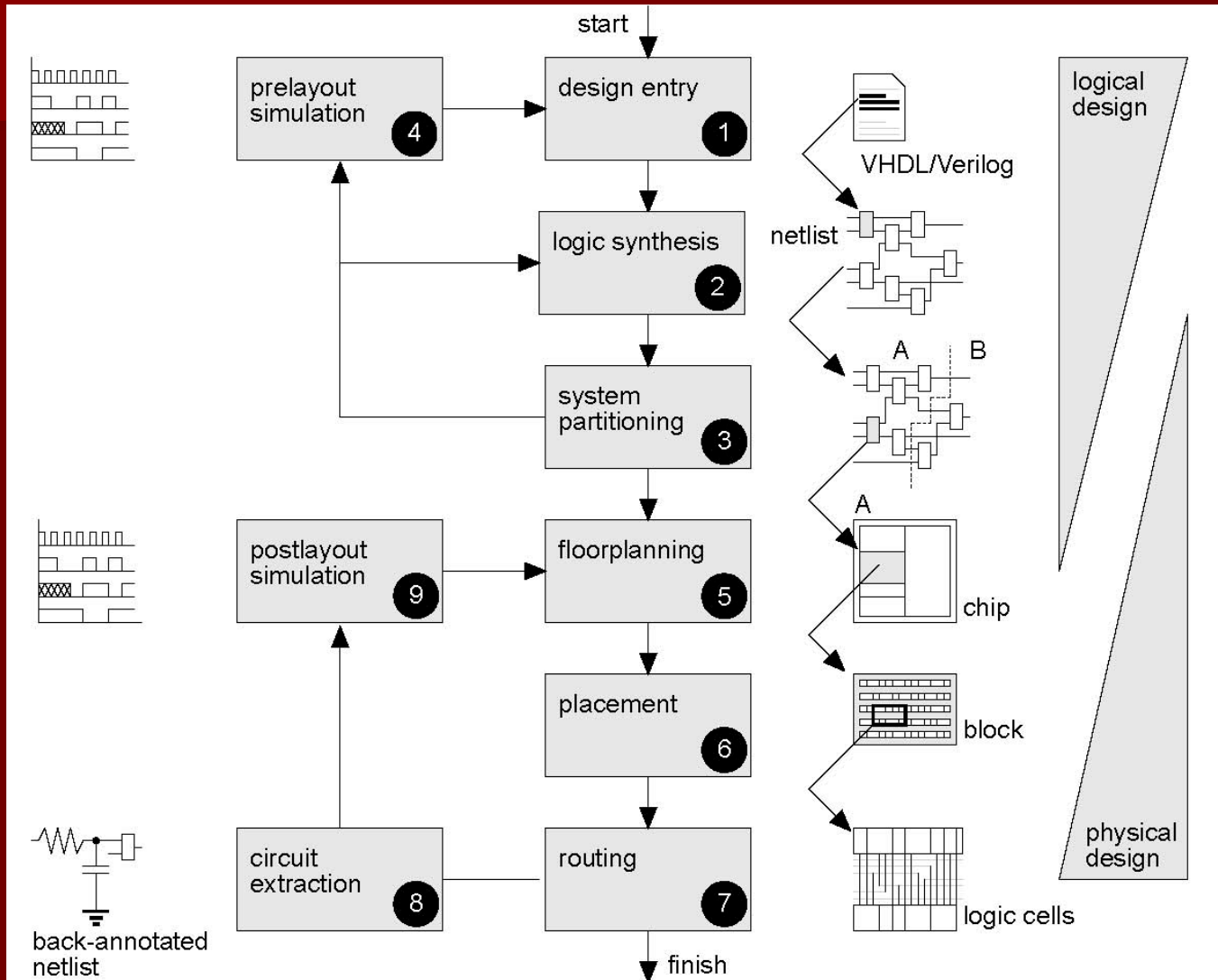
# Physical design process overview

- CMOS transistor structure and fabrication steps
- Standard cell layouts
- Creation, verification & characterization of a standard-cell based logic circuit block
- Creation of a chip from circuit blocks

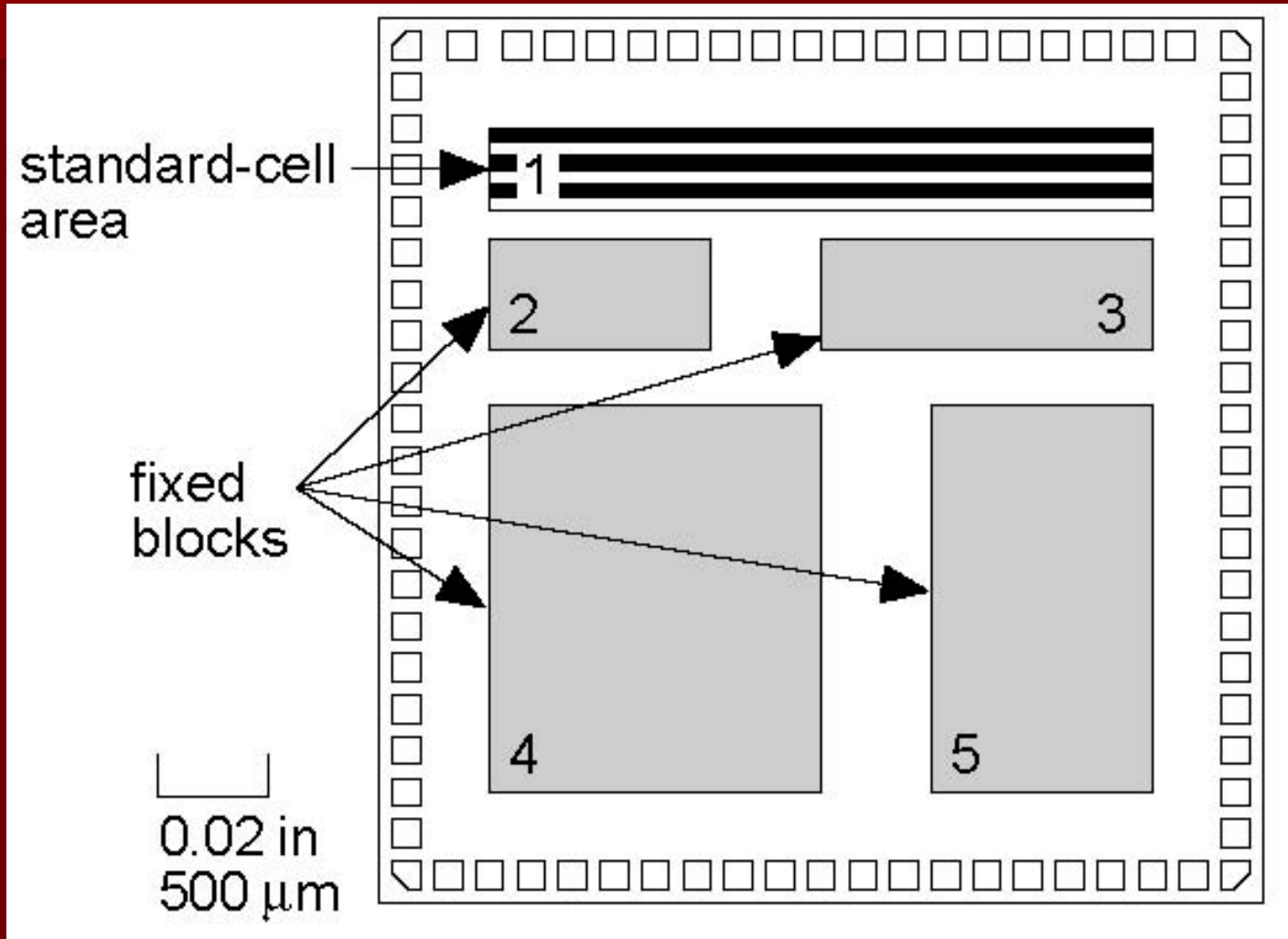
# IC/ASIC Design Flow



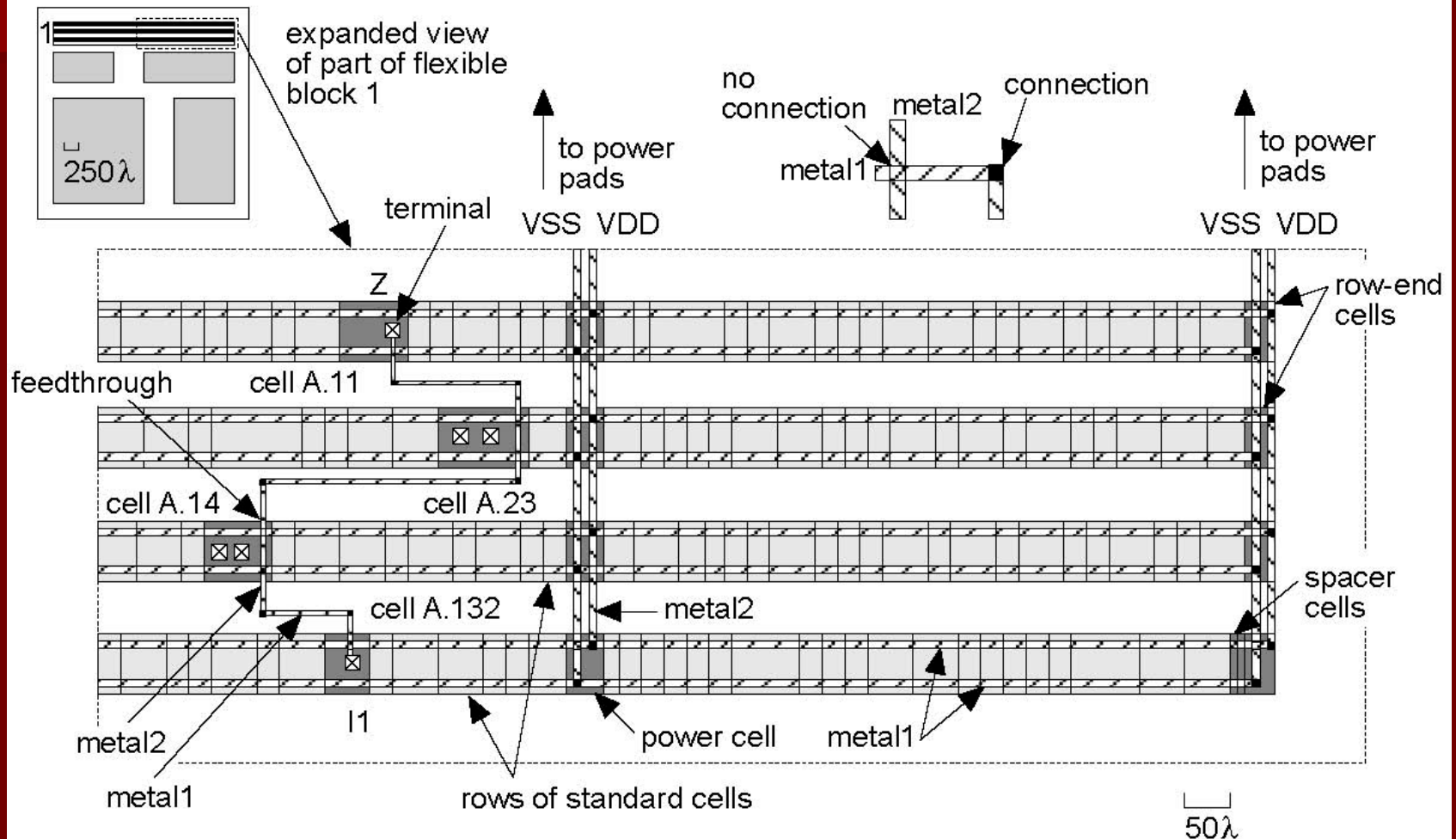
# ASIC Design Flow



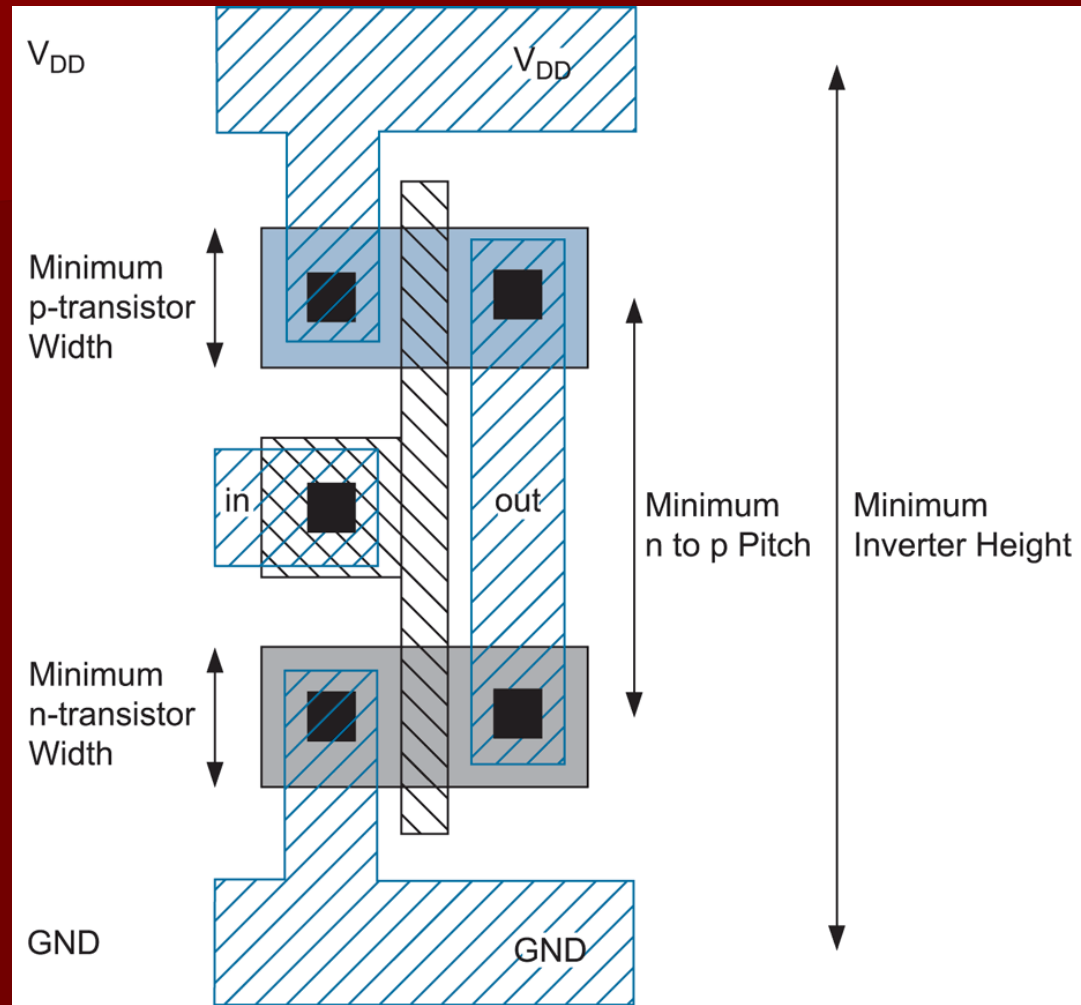
# Cell-Based IC



# Cell-Based Block

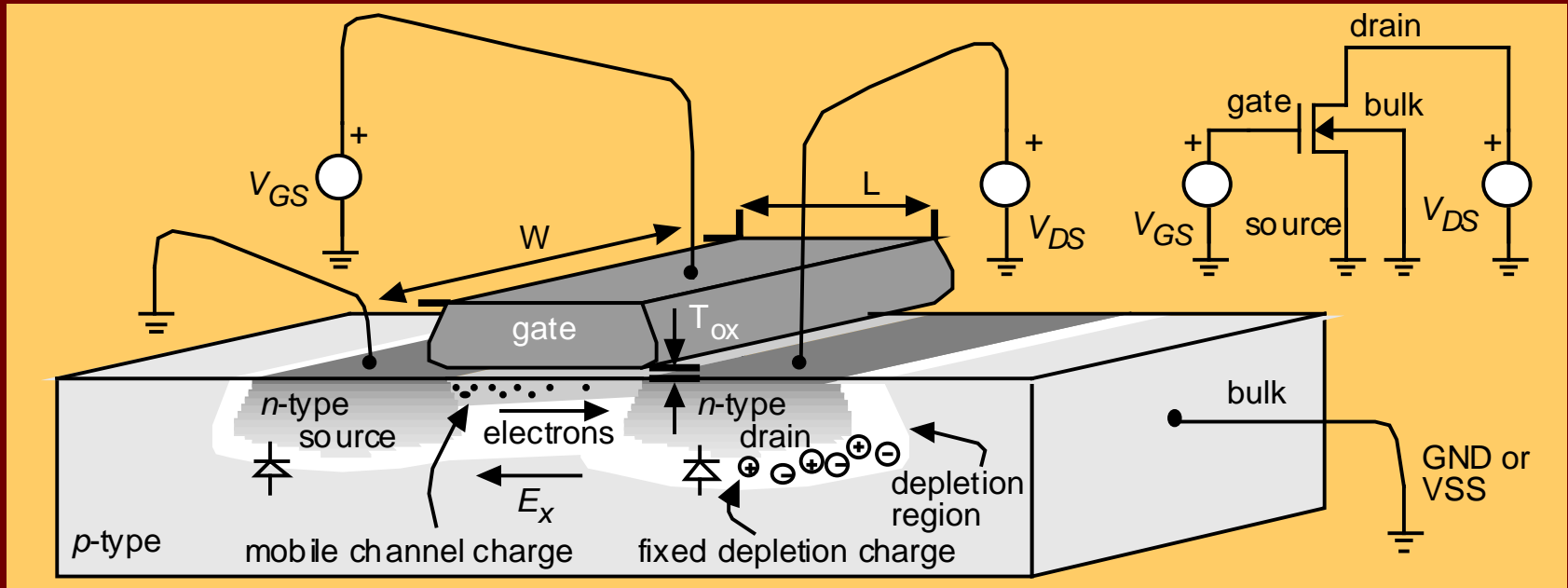


# Basic standard Cell layout

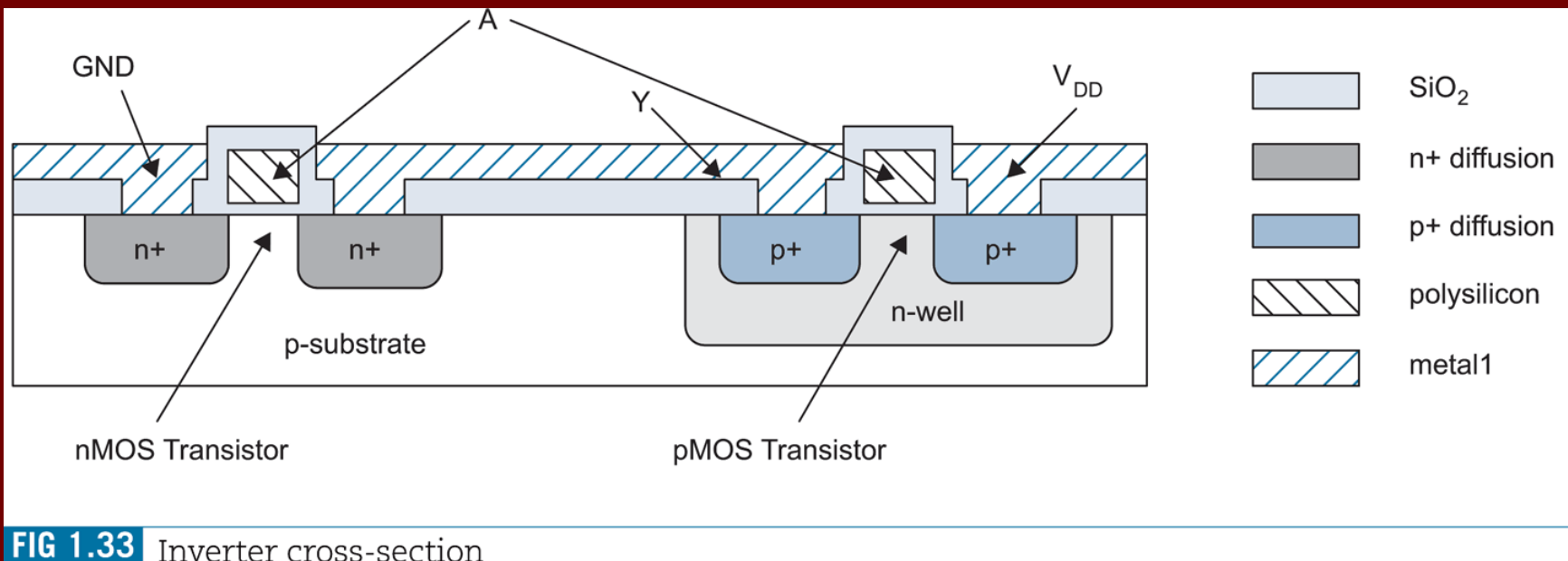


**FIG 3.30** Minimum inverter height

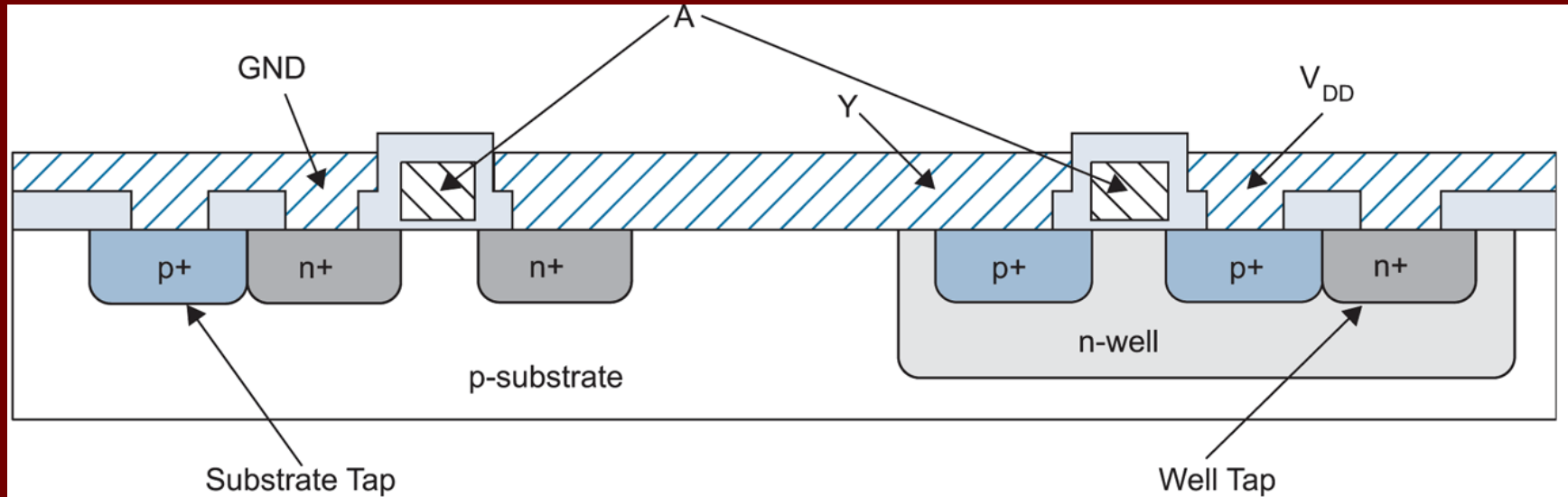
# N-channel MOS transistor



# CMOS Inverter Cross-Section

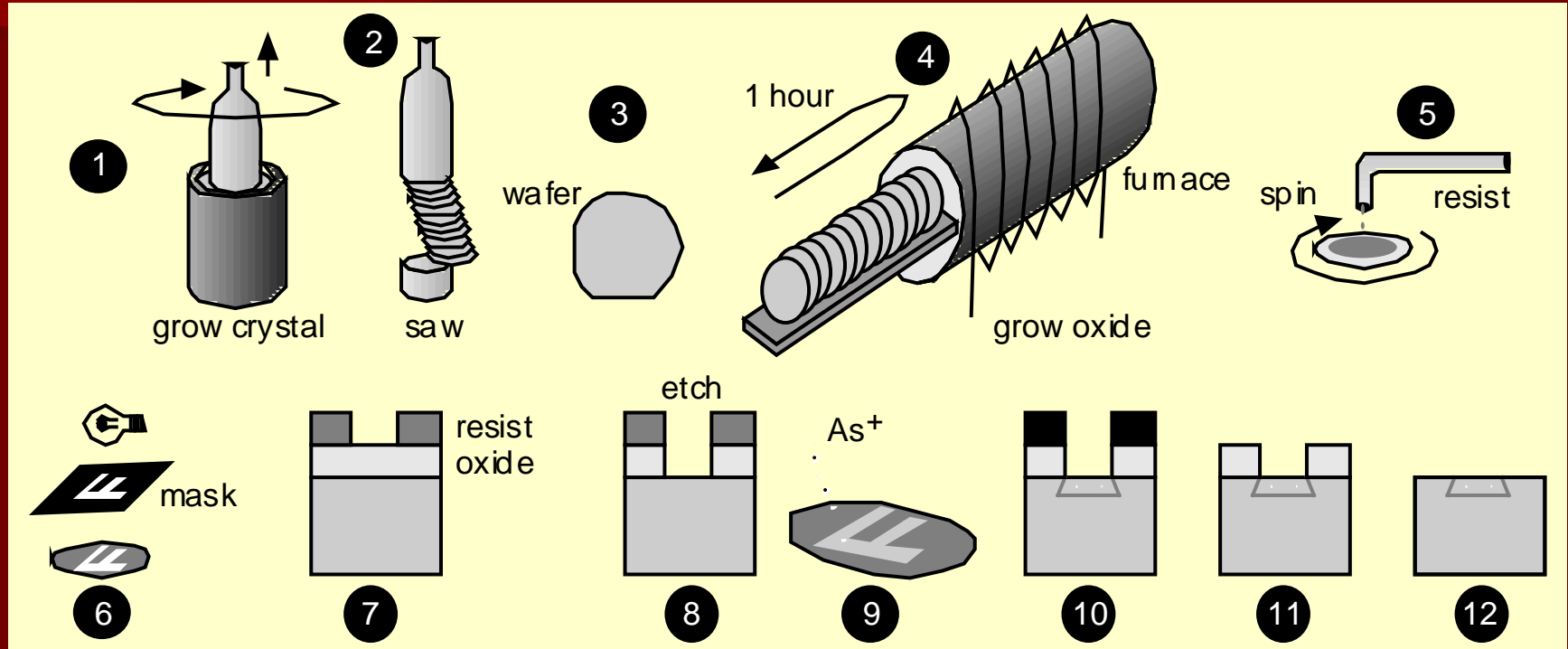


# Inverter cross-section with well and substrate contacts



**FIG 1.34** Inverter cross-section with well and substrate contacts. Color version on inside front cover.

# IC fabrication process



4. Grow oxide  $SiO_2$

5. Apply photoresist

6. UV light exposes resist

7. Remove exposed resist

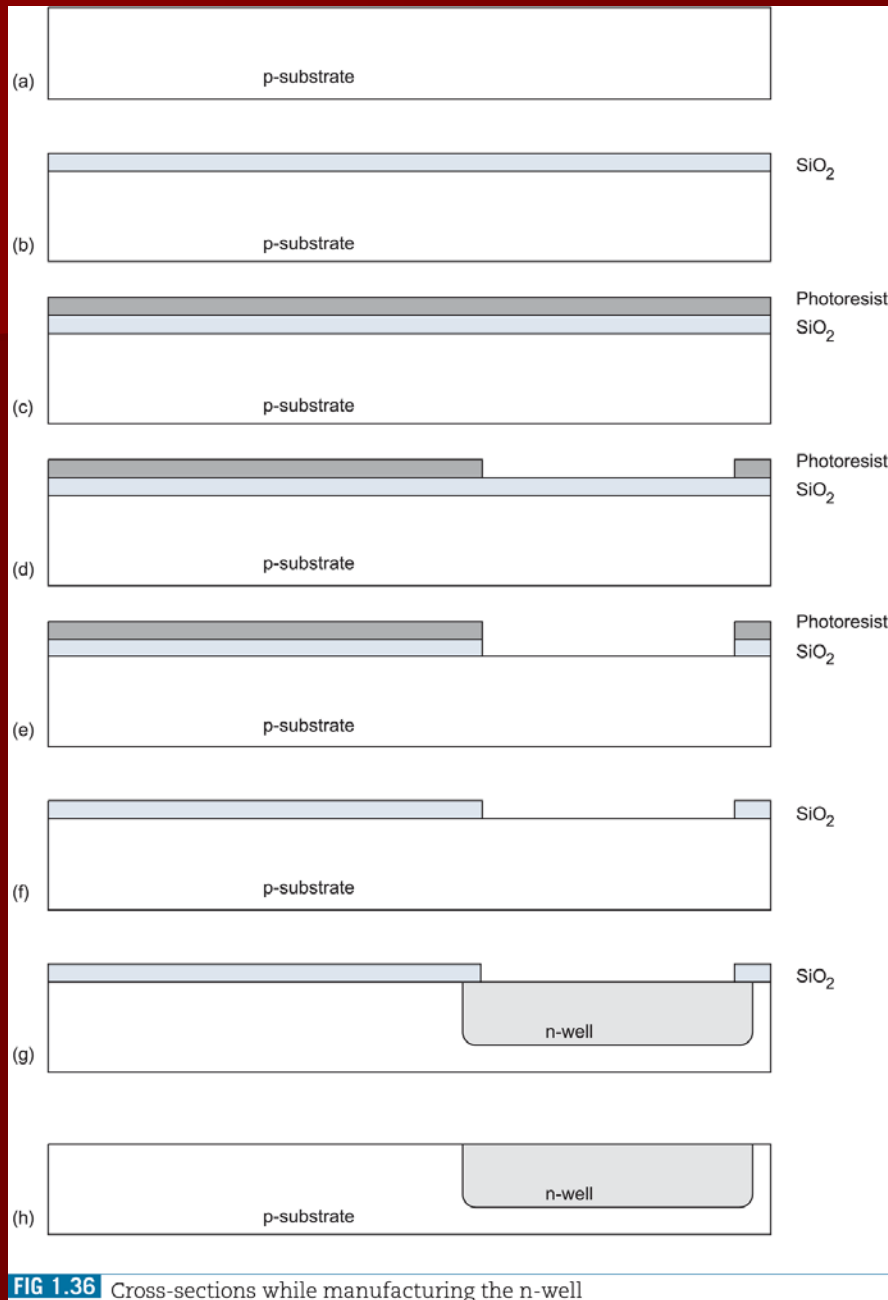
8. Etch exposed oxide

9-10. Implant ions in exposed substrate

11. Strip resist

12. Etch oxide

# CMOS Process steps



P-substrate

SiO<sub>2</sub> layer

Photoresist

Expose and etch

Etch SiO<sub>2</sub>

Remove photoresist

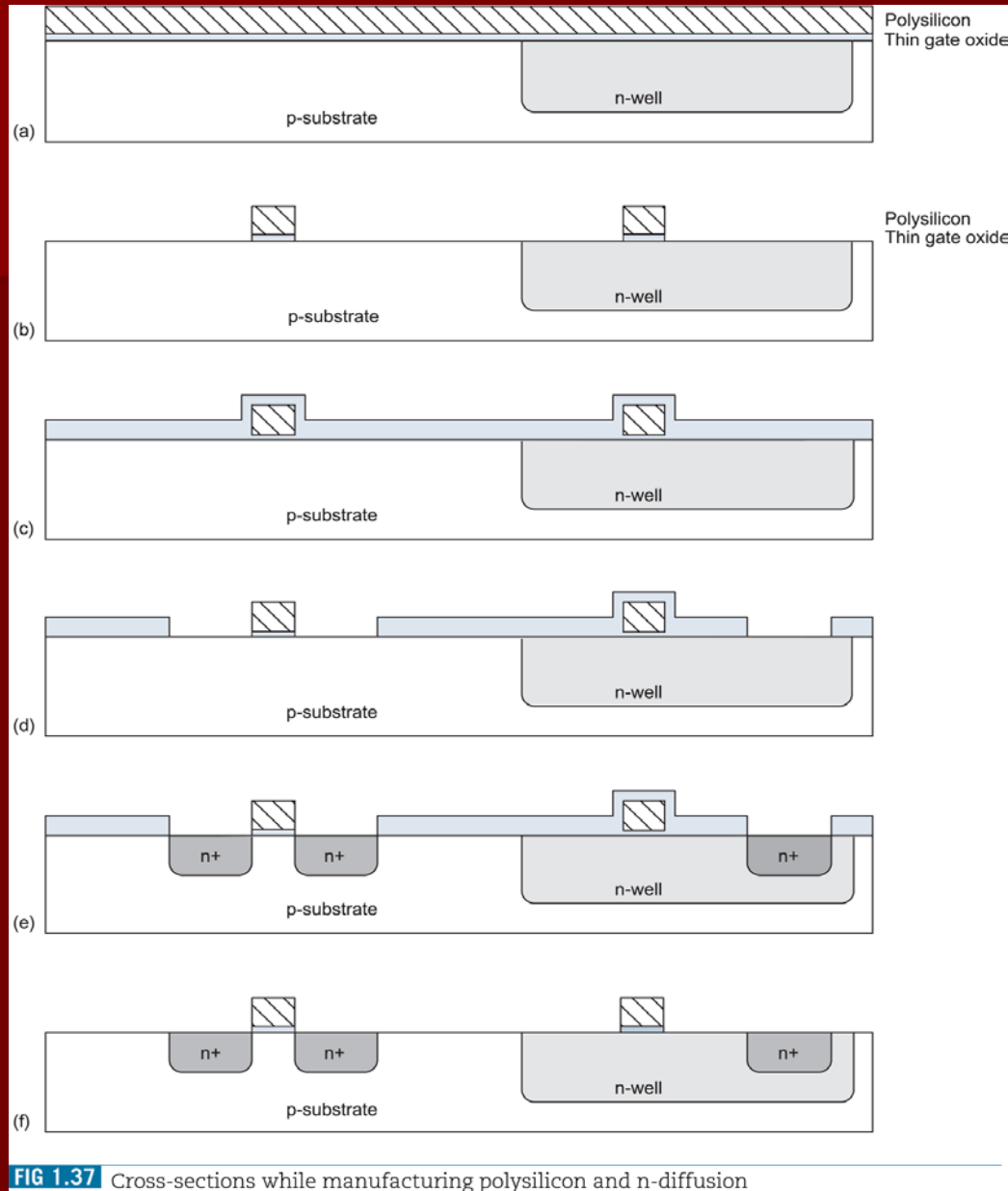
Implant n-well

Remove SiO<sub>2</sub>

FIG 1.36 Cross-sections while manufacturing the n-well

Source: Weste "CMOS VLSI Design"

# CMOS Process steps



Deposit poly

Etch

Deposit SiO<sub>2</sub>

Etch

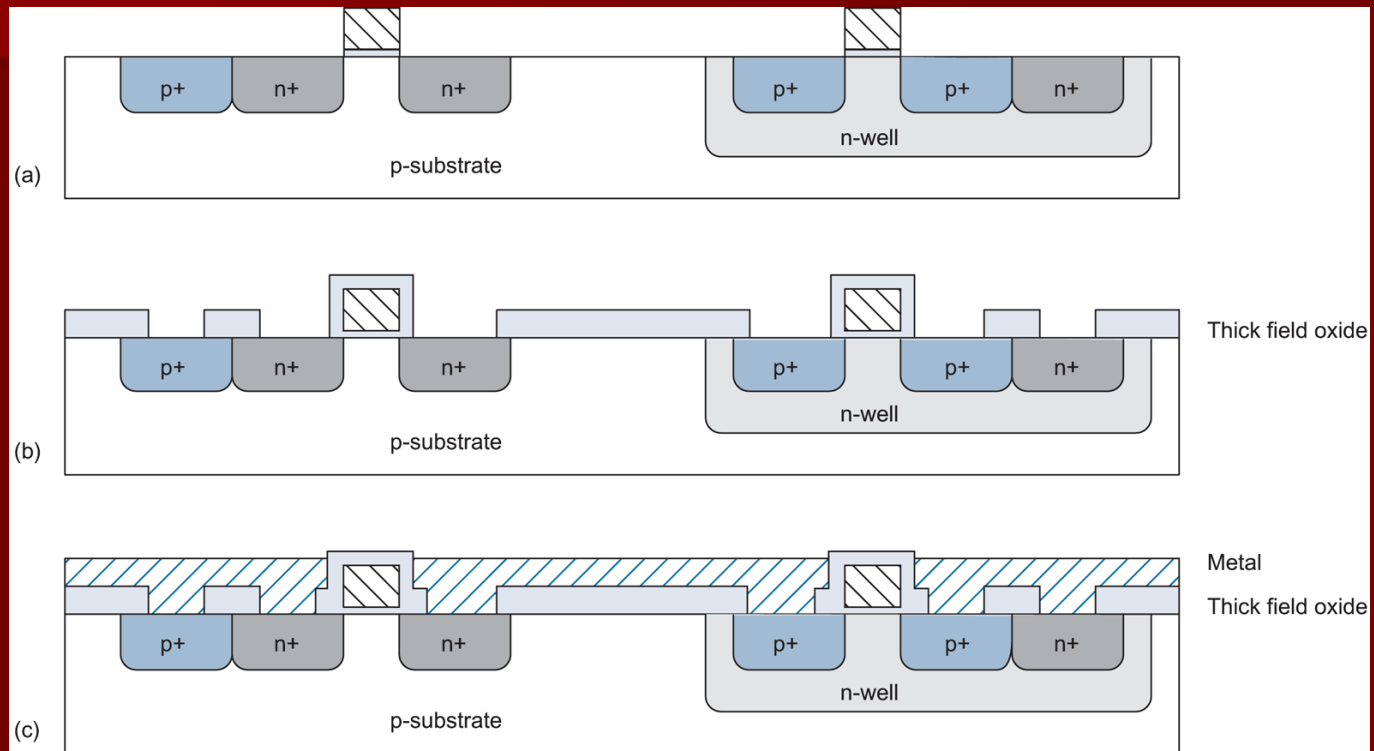
Diffusion

Remove SiO<sub>2</sub>

FIG 1.37 Cross-sections while manufacturing polysilicon and n-diffusion

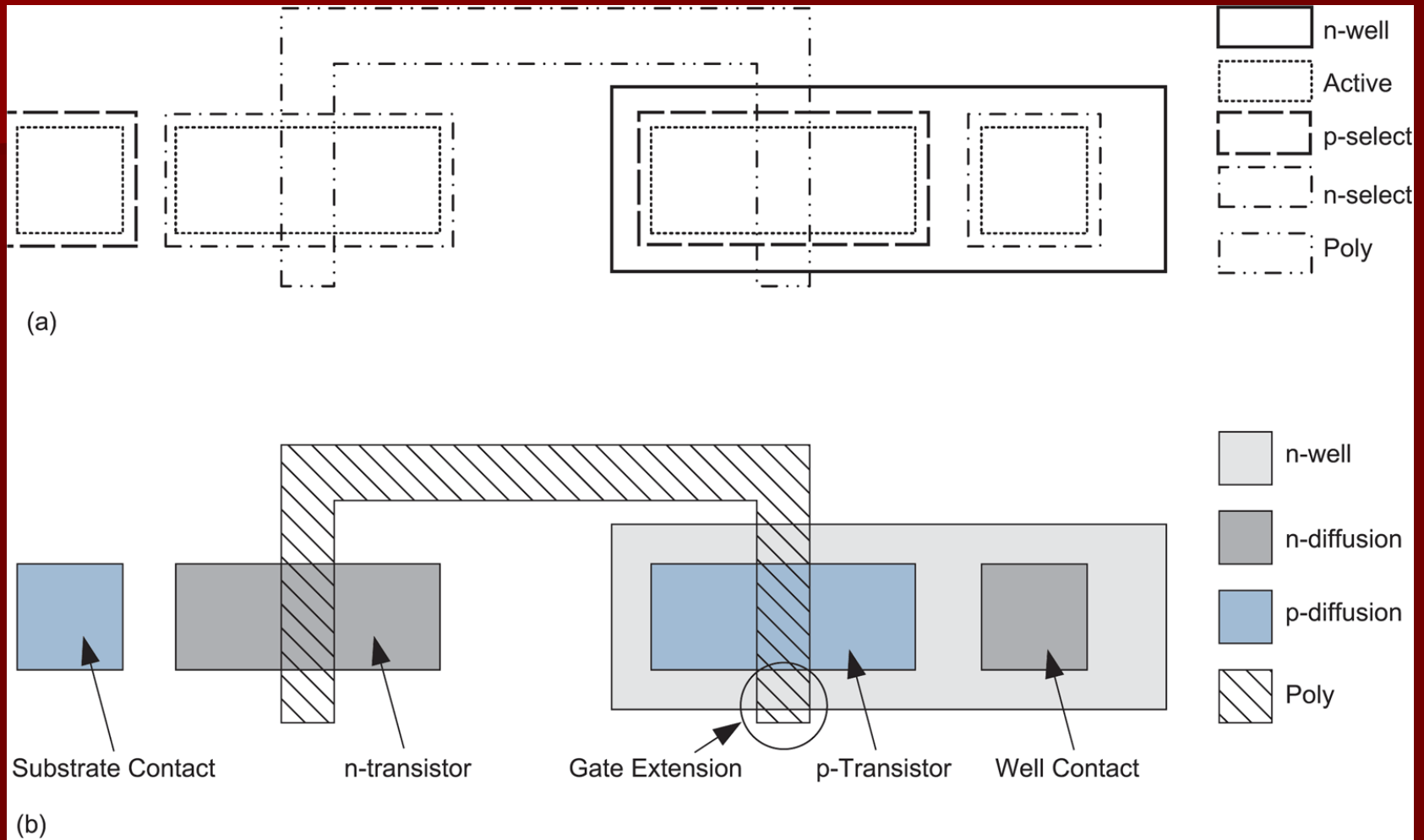
Source: Weste "CMOS VLSI Design"

# CMOS Process steps



**FIG 1.38** Cross-sections while manufacturing p-diffusion, contacts, and metal

# CMOS n-well process transistor



**FIG 3.9** CMOS n-well process transistor and well/substrate contact construction

# Inverter mask set

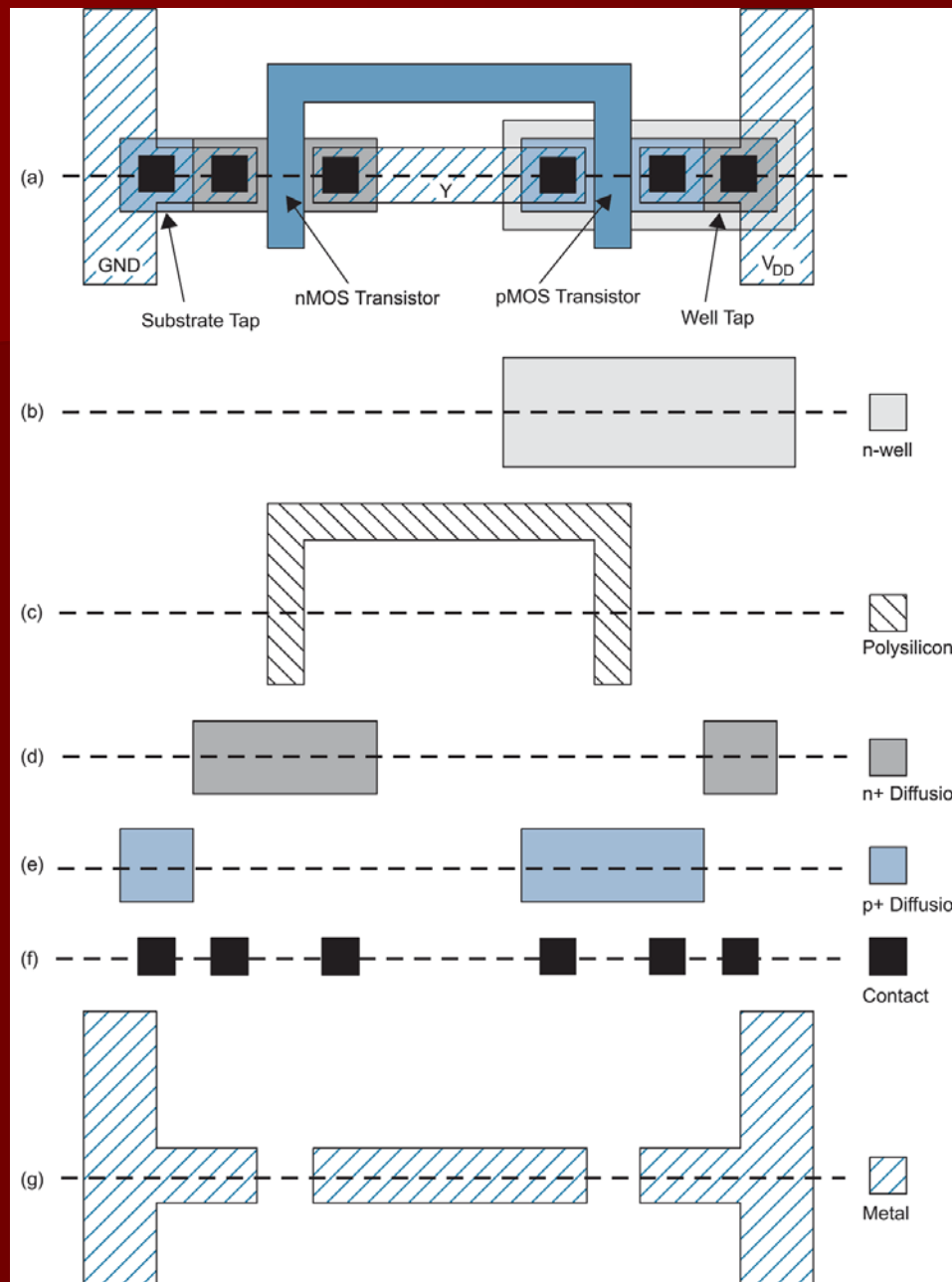
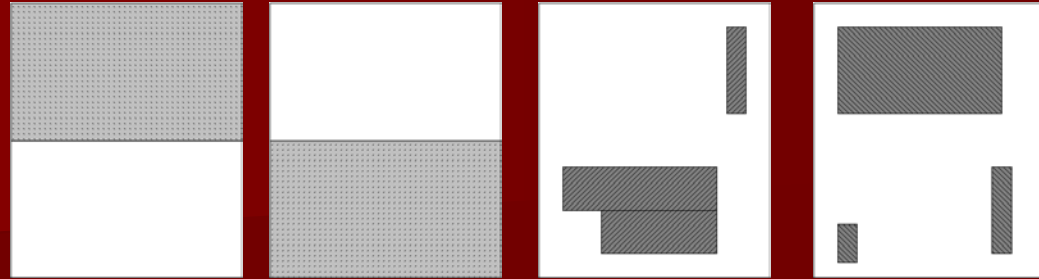
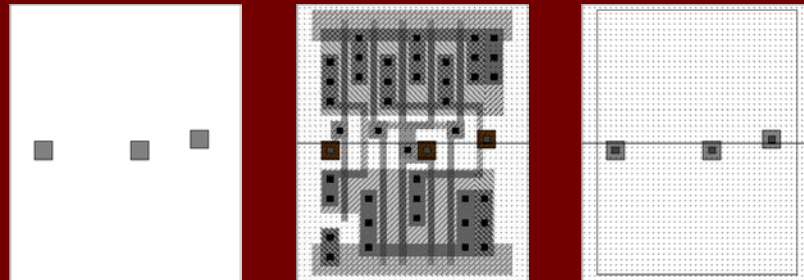
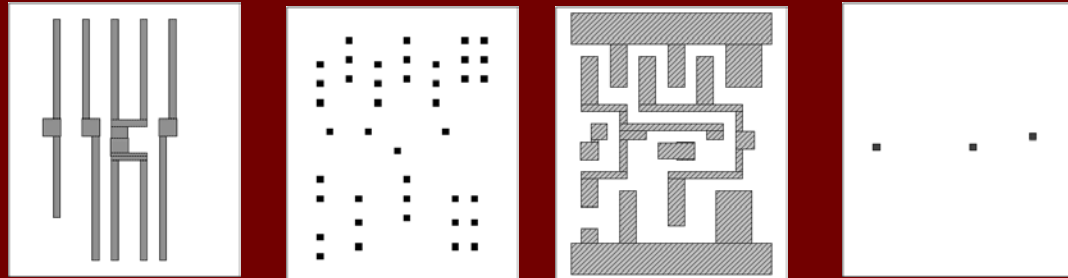


FIG 1.35 Inverter mask set. Color version on inside front cover.

# Standard Cell Mask Set



Submit mask  
info to fab.



Source: Smith, Figure 2.7

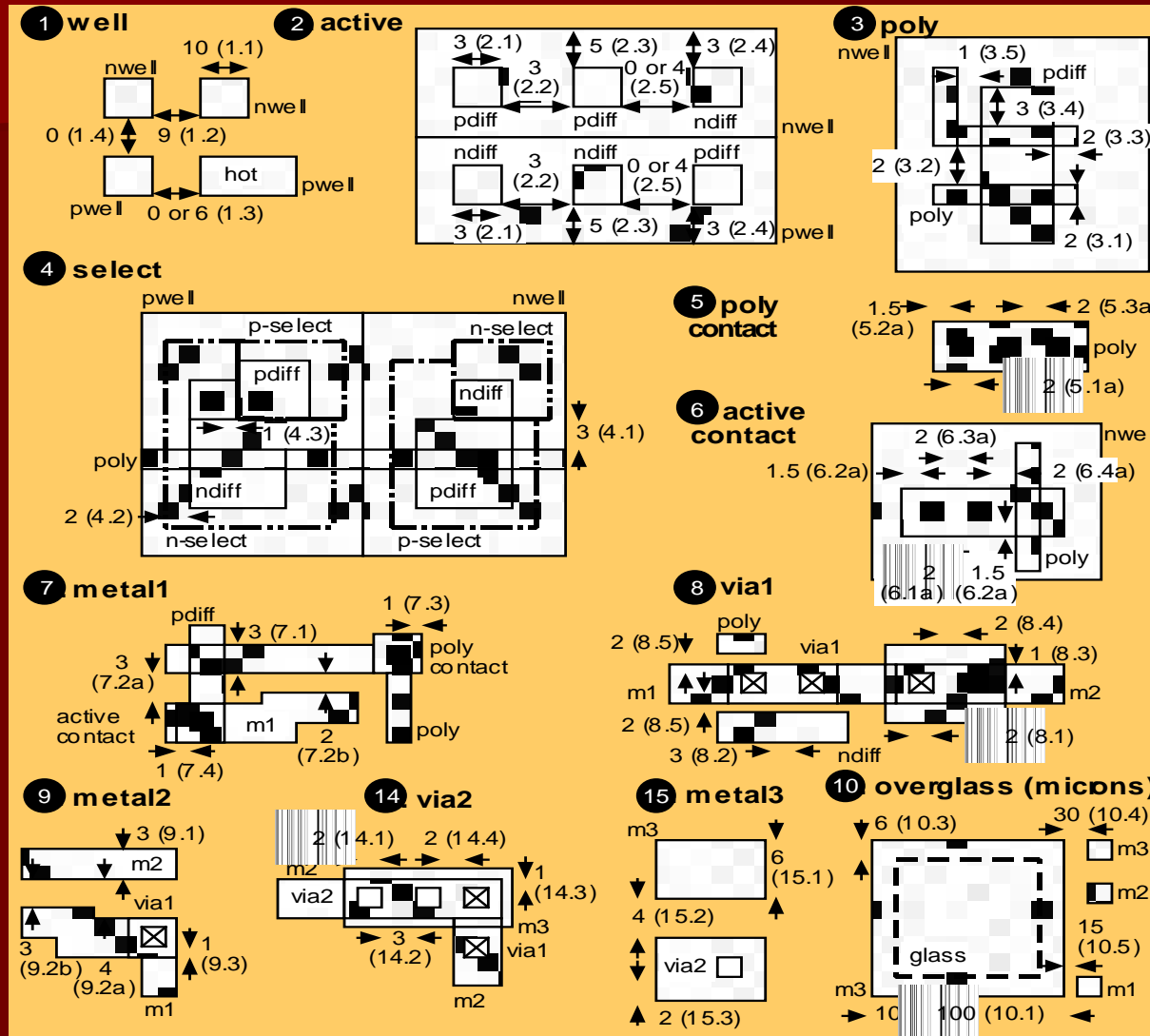
# MOSIS fab processes (<http://www.mosis.org>)

**Table 3.1** MOSIS design rule options

Vendor	Feature Size ( $\mu\text{m}$ )	Interconnect Layers	Stacked Vias	SCMOS	SUBM	DEEP
Orbit	2.0	2 metal	No	$\lambda = 1.0 \mu\text{m}$		
AMI	1.5	2 metal, 2 poly	No	$\lambda = 0.80 \mu\text{m}$	$\lambda = 0.80 \mu\text{m}$	
AMI	0.5	3 metal, 1-2 poly	Yes	$\lambda = 0.35 \mu\text{m}$	$\lambda = 0.30 \mu\text{m}$	
TSMC	0.35	4 metal, 1-2 poly	Yes		$\lambda = 0.20 \mu\text{m}$	
TSMC	0.25	5 metal	Yes		$\lambda = 0.15 \mu\text{m}$	$\lambda = 0.12 \mu\text{m}$
TSMC	0.18	6 metal	Yes		$\lambda = 0.10 \mu\text{m}$	$\lambda = 0.09 \mu\text{m}$

ASIC Design Kit

# CMOS process design rules



# MOSIS Design Rules

Table 3.2 MOSIS design rules					
Layer	Rule	Description	SCMOS	SUBM	DEEP
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surround by well	5	6	6
	2.4	Substrate/well contact surround by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field oxide	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate/well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4
Contact (to poly or active)	5.1, 6.1	Width (exact)	2x2	2x2	2x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/ active contacts	3	3	3
	6.8b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 $\lambda$	4	6	6

Smith text:  
Tables 2.7-2.9

# MOSIS Design Rules

Table 3.2 MOSIS design rules (continued)					
Layer	Rule	Description	SCMOS	SUBM	DEEP
Via1– Via(N-1)	8.1, 14.1, ...	Width (exact)	2x2	2x2	3x3
	8.2, 14.2, ...	Spacing to via on same layer	3	3	3
	8.4	Spacing to contacts (if no stacked vias)	2	2	n/a
	8.5	Spacing of via1 to poly or active edge	2	2	n/a
	14.4	Spacing of via2 to via1 (if no stacked vias)	2	2	n/a
Metal2– Metal(N-1)	9.1, ...	Width	3	3	3
	9.2, ...	Spacing to same layer metal	3	3	4
	9.3, ...	Overlap of via	1	1	1
	9.4, ...	Spacing to metal for lines wider than 10 $\lambda$	6	6	8
Metal3 (3-layer process)	15.1	Width	6	5	n/a
	15.2	Spacing to metal3	4	3	n/a
	15.3	Overlap of via2	2	2	n/a
	15.4	Spacing to metal for lines wider than 10 $\lambda$	8	6	n/a
Metal5 (5-layer process)	26.1	Width	n/a	4	4
	26.2	Spacing to metal5	n/a	4	4
	26.3	Overlap of via4	n/a	1	2
	26.4	Spacing to metal for lines wider than 10 $\lambda$	n/a	8	8
Metal6 (6-layer process)	30.1	Width	n/a	5	5
	30.2	Spacing to metal6	n/a	5	5
	30.3	Overlap of via5	n/a	1	2
	30.4	Spacing to metal for lines wider than 10 $\lambda$	n/a	10	10
Overglass Cut	10.1	Width of bond pad opening	60 $\mu\text{m}$		
	10.2	Width of probe pad opening	20 $\mu\text{m}$		
	10.3	Metal overlap of overglass cut	6 $\mu\text{m}$		
	10.4	Spacing of pad metal to unrelated metal	30 $\mu\text{m}$		
	10.5	Spacing of pad metal to active or poly	15 $\mu\text{m}$		

Smith text:  
Tables 2.7-2.9

# MOSIS Design Rules

Table 3.3 Micron design rules for 90nm process			
Layer	Rule	Description	90 nm rule (μm)
Well	1.1	Width	0.75
	1.2	Spacing to well at different potential	1.5
	1.3	Spacing to well at same potential	1.0
Active (diffusion)	2.1	Width	0.15
	2.2	Spacing to active	0.20
	2.3	Source/drain surround by well	0.25
	2.4	Substrate/well contact surround by well	0.25
	2.5	Spacing to active of opposite type	0.30
Poly	3.1	Width	0.09
	3.2	Spacing to poly over field oxide	0.15
	3.2a	Spacing to poly over active	0.15
	3.3	Gate extension beyond active	0.15
	3.4	Active extension beyond poly	0.15
	3.5	Spacing of poly to active	0.10
Select	4.1	Spacing from substrate/well contact to gate	0.25
	4.2	Overlap of active	0.20
	4.3	Overlap of substrate/well contact	0.10
	4.4	Spacing to select	0.30
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.12
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.15
	5.4	Spacing to gate	0.10
Metal1	7.1	Width	0.13
	7.2	Spacing to well metal1	0.13
	7.3, 8.3	Overlap of contact or via	0.01
	7.4	Spacing to metal for lines wider than 0.5 μm	0.40
Via1–Via5	8.1, 14.1, ...	Width (exact)	0.13
	8.2, 14.2, ...	Spacing to via on same layer	0.13

(continued)

# MOSIS Design Rules

<b>Table 3.3</b>		<b>Micron design rules for 90nm process (continued)</b>	
<b>Layer</b>	<b>Rule</b>	<b>Description</b>	<b>90 nm rule (<math>\mu\text{m}</math>)</b>
Metal2– Metal6	9.1, ...	Width	0.15
	9.2, ...	Spacing to same layer metal	0.15
	9.3, ...	Overlap of via	0.01
	9.4, ...	Spacing to metal for lines wider than 1.0 $\mu\text{m}$	0.40
Via6		Width	0.20
		Spacing	0.20
Metal7		Width	0.40
		Spacing to metal7	0.40
		Overlap of via6	0.10
		Spacing to metal7 for lines wider than 1.0 $\mu\text{m}$	0.50