Chapter 10
Bipolar Process Integration

- Bipolar junction transistor (BJT) is a pnp on npn junction transistor.
- BJTs can be used as amplifiers, switches, or in oscillators.
- BJTs can individual a discrete component or in ICs.
- Relationships between impurity profiles and the device parameters such as current gain, transit time, breakdown voltage, etc.
- Junction-isolated double-diffusion epitaxial bipolar transistor with buried layer
- “Standard Buried Collector” (SBC) process for understanding the limitations and fabrication processes

Physical Structure of BJTs

There are two types of BJTs \( \rightarrow \) npn and pnp types

- Consists of 3 alternating layers of n- and p-type semiconductor.
- Majority of current enters C, crosses B-region and exits through E. A small current also enters B-terminal, crosses B-E junction and exits through E.
Current-Voltage and current Flow Characteristics

Three operating regions
- **Cut-off**: considered as an open switch
- **Saturation**: when both junctions are forward biased (appears as a closed switch)
- **Active**: high voltage, current and power gain — works as an amplifier

- Carrier transport in the active base region directly beneath the heavily doped \((n^+\) emitter dominates \(i-v\) characteristics of BJT.
Relation to pn Junction Diode

nnp – BJT

In reality the devices are not this simple... simples one we will look at is called the SBC (standard buried collector) device / process

Bipolar Transistor (from Ch-1)
Top View and Cross-Section

- Bipolar Junction Transistor (BJT)
- Standard Buried Collector Process (SBC)
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Metal (Al) Interconnections

FIGURE 1.5
The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).
**Bipolar Transistor: Buried Collector**
(Schematic and Cross-Section View)

- **Active Transistor Region**

**SBC Process**
(see Ch-1 for further discussion)

- An n+ buried layer formed by selective diffusion
- Then an n-type epitaxy layer is formed
- Next, the n-type collector is formed
- Then base and emitter are formed by successive p-type and n-type diffusion into the epitaxy layer
- Finally, the contact windows formed, then metallization is completed
BJT Standard Buried Collector (SBC) Process (cont.)

FIGURE 10.1
(a) Photo of an SBC transistor (b) Cross section of a transistor fabricated with the SBC process showing the collector-base capacitances and the base and collector series resistances; (b) lumped circuit model for the transistor showing back-to-back diodes which provide isolation between adjacent transistors.

- Primary process for analog applications
- For digital applications, self-aligned oxide isolated process is used – will be discussed later
nnp BJT: SBC Process – Impurity Distribution

FIGURE 10.2
Vertical impurity profile in typical bipolar junction transistor. The shaded regions represent the emitter-base and collector-base space-charge regions. The metallurgical basewidth and electrical basewidth are indicated by $W_{met}$ and $W_{B}$, respectively.
**nnp Transistor: Forward Characteristics**

Forward transport current is

\[ i_C = i_F = I_S \exp \left( \frac{V_{BE}}{V_T} \right) - 1 \]

The Base current is

\[ i_B = \frac{i_F}{\beta_F} = \frac{I_S}{\beta_F} \exp \left( \frac{V_{BE}}{V_T} \right) - 1 \]

Emitter current is

\[ i_E = i_C + i_B = \frac{I_S}{\alpha_F} \exp \left( \frac{V_{BE}}{V_T} \right) - 1 \]

Saturation current

\[ 10^{-18} \text{ A} \leq I_S \leq 10^{-9} \text{ A} \]

Thermal potential

\[ V_T = kT/q = 0.025 \text{ V at room temperature} \]

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**Current Gain**

In forward active operation,

\[ \frac{i_C}{i_B} = \beta_F \quad \text{and} \quad \frac{i_C}{i_E} = \alpha_F \]

\[ 20 \leq \beta_F \leq 500 \]

Forward common-emitter current gain range – smaller values are for digital application and larger values are for amplifier (analog) applications

\[ 0.95 \leq \frac{\beta_F}{\beta_F + 1} \leq 1.0 \]

forward common-base current gain

- There is also the reverse operation and reverse current, reverse common-base current gain
- But we will not discuss them here
Current Gain (cont.)

The common-emitter forward current transfer ratio (or simply the current gain) $\beta$ is defined as:

$$\beta = \frac{I_C}{I_B} = \frac{\alpha_f}{1 - \alpha_f}$$

where $\alpha_f$ is common-base forward current transfer ratio

For large current gains $\beta^{-1}$ should be as small as possible
The ratio of the Gummel number should be low
The width of the base region should be small
Diffusion length for the minority carriers ($L_B$) should be large
In modern high-frequency transistors, base width is far less than diffusion length, so the first term determines the current gain

$W_B = \text{base width}$

$L_B = \text{diffusion length (of the minority carriers) in the base}$

$G_B$ and $G_E = \text{base and emitter Gummel numbers and are defined as:}$

Gummel Numbers Definition

$G_B = \text{base Gummel number}$

$G_E = \text{emitter Gummel numbers}$

Emitter must be heavily doped in order to get large gain

$$G_B = \int_{\text{base}} \frac{N(x)}{D_B(x)} \, dx \quad G_E = \int_{\text{emitter}} \frac{N(x)}{D_E(x)} \, dx$$

$D_B$ and $D_E$ are the minority-carrier diffusion constants

For wide-base transistors, $W_B \approx W_{\text{met}}$

Heavy doping usually limits the value of $G_E \approx 10^{13}$ to $10^{14}$ sec/cm$^4$
Diffusion Lengths (for p-type and n-type minority carriers)

As doping level increases, diffusion length decreases

FIGURE 10.3
Calculated minority-carrier diffusion lengths as a function of doping concentration for bulk silicon using lifetime equations from Ref. [1].

$L_B$ is about 10 µm for typical base-doping concentrations

Transit Time & Unity Gain Frequency

Delay incurred during carrier propagation between the emitter and collector terminals is an important parameter, determines switching speeds and frequency responses

Transit Time is defined by:

$$\tau = r_E C_{BE} + \frac{W^2_B}{\eta D_B} + (C_{JC} + C_{sub}) r_C + \frac{X_C}{2v_s}$$

- $r_E$: Small signal resistance of the emitter region
- $C_{BE}$: Emitter-base capacitance
- $W_B$: Base transit time (time required for a carrier to move across the neutral base region)
- $D_B$: Delay associated with charging the capacitances connected to the collector node through the collector series resistance (determined by the c-b and c-sub junction areas and by doping concentrations)
- $X_C$: Delay time associated with a carrier crossing the depletion region of the collector-base junction ($v_s$ is the saturation velocity of the carriers)
Transit Time & Unity Gain Frequency (cont.)

Unity-gain frequency is approximated by:

\[ f_T = \frac{1}{2\pi r_C} \]

To minimize transit time, the base width is made as narrow as possible, the buried layer is added to minimize the value of \( r_C \) and light doping is used to minimize the capacitances (calculated using Eq. 9.3, using the lightly doped sides concentration)

Basewidth: Depletion Layer Extends

- Device performance is improved by making \( W_B \) as narrow as possible!
- But restricted by breakdown voltage and tolerance (during fabrication processes)
- For low voltage logic devices 1\( \mu \)m is possible
- For high voltage devices (analog circuits or power electronics) \( W_B \) must be wide

Emitter and base area heavily doped at base emitter junction (see Ch-9; Fig 9.4)

 Depends on voltage across the junction
Base width (cont.)

- Increased base doping reduces the space-charge region size in the base, but increases the Gummel number (that means it reduces the current gain)
- Also increases the transit time

**FIGURE 10.4**
The space-charge region width as a function of voltage and doping for a p-n junction formed by a Gaussian diffusion into a uniformly doped substrate. (a) Total space-charge region width $x_T$; (b) fraction of total space-charge region width extending on the heavily doped side, $x_h$, and on the lightly doped side, $x_l$, respectively. After Ref. [4]. Reprinted with permission from the AT&T Technical Journal. Copyright 1960 AT&T.

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Junction Breakdown: Emitter-base Breakdown Voltage

Breakdown voltage is determined by doping concentration and radius of curvature of the junction (see Ch. 9). High Current gain => emitter region is doped heavily

**FIGURE 10.5**
Circular Emitters

Circular emitters improve breakdown voltages (by increasing the radius of curvature)

- Circular emitters are used to improve device matching
- Here a quad of transistors are cross connected to form a differential pair

Junction Breakdown: Collector-base Breakdown Voltage

- Two mechanisms to conduct excessive current:
  - Zener or Avalanche breakdown of collector-base junction (breakdown is localized to the region where the doping concentrations are the largest)
    - Avalanche breakdown is when the width of depletion region extends under the bias voltage as electrons accelerate by the electric field.
    - Occurs only in heavily doped diodes – high doping results in narrow depletion region/width. An application of bias voltage results in charge carriers tunnel through the junction.
  - Punch-through of the base region (epitaxial-layer doping, width of the region between the collector-base junction and the $n^+$ buried layer)
    - High Zener breakdown voltage requires low epitaxial-layer doping
    - Low epitaxial-doping requires relatively low epitaxial-layer thickness to prevent punch-through
    - Wide depletion region width in epitaxial-layer increases the transit time and reduces the frequency response of the device
Collector-base Breakdown Voltage (cont.)

![Graph showing collector-base breakdown voltage as a function of collector-doping concentration and punch-through limits.]

**FIGURE 10.7**
Collector-base junction breakdown voltage as a function of collector-doping concentration with collector-base junction depth and punch-through limits as parameters. After Ref. [4].

Punch-through Voltage

**FIGURE 10.8**
Collector-base space-charge region growth as the collector-base voltage is increased. (a) Zero bias; (b) intermediate collector-base voltage; (c) large collector-base voltage just below the punch-through voltage.
Other Elements in the SBC Technology

Other electronic elements such as resistors, diodes, and pnp transistors are required to build circuits in bipolar technology.

SBC technology is optimized around npn transistors, because of the high-mobility electron transport across the base region.

<table>
<thead>
<tr>
<th>Resistor layer</th>
<th>Sheet Resistance (Ω/sq)</th>
<th>Absolute Tolerance (%)</th>
<th>Matching (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Diffusion</td>
<td>5-20</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>Base Diffusion</td>
<td>100-200</td>
<td>20</td>
<td>0.2-2</td>
</tr>
<tr>
<td>Epitaxial Layer</td>
<td>1000-5000</td>
<td>30</td>
<td>5</td>
</tr>
<tr>
<td>Pinched Base</td>
<td>2000-10,000</td>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>Ion Implanted</td>
<td>100-1000</td>
<td>3</td>
<td>0.1-1</td>
</tr>
</tbody>
</table>

SBC Circuit Elements

n⁺ Resistor (from Emitter Diffusion)

- Resistor formed using n⁺ emitter diffusion into the (heavily doped p-type) isolation region
- Resistor-substrate isolation is maintained by a reverse bias across the pn junction
- Low sheet resistance 10-50 Ω/square
- Relatively large junction capacitance
- Low breakdown voltage
SBC Circuit Elements
p-type Resistor (Base Diffusion)

- Base diffusion (within an isolated n-type epitaxial region) used as a p-type resistor
- Body must be kept reverse-biased along its length
- An n+ region is placed below the Al contact to ensure the formation of ohmic contact (not a Schottky barrier diode)
- Typical sheet resistance 100-300 Ω/square

SBC Circuit Elements
n-type Resistor (Epitaxial Layer)

- Resistor formed in the epitaxial tub (by making two ohmic contacts to an isolated epitaxial region)
- High sheet resistance (but poorly controlled)
- 1000-10000 Ω/square
SBC Circuit Elements

p-type Pinch Resistor (Also JFET)

- Base region "pinched" down (narrowed the thickness of the base diffusion) to increase sheet resistance
- Similar to npn transistor
- Resistance value is highly dependent on the thickness of the pinched region
- JFET formed by the same structure (A and B as the source and drain, and n-region is as the gate)

SBC Circuit Elements

Substrate pnp Transistor

- Substrate pnp with transistor collector formed by wafer or "substrate"
- P-type diffusion (emitter), isolated epitaxial tub (base), and p-type substrate (collector)
- The base width $W_B$ is much wider than npn device
- Collector is tied to the most negative power supply level in the circuit
SBC Circuit Elements
Lateral pnp Transistor

- Lateral pnp (uncommitted collector, base, and emitter contact)
- Emitter and collector are formed from p-type regions
- Base width \(W_B\) determined by lithography capability (and is much wider than of the npn devices)
- Poor current gain and frequency response compared to vertical device

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SBC Circuit Elements
Schottky Diode

- Schottky diode can be readily formed by metal contact to a lightly doped n-type semiconductor
- p-type ring added to eliminate edge breakdown
- Wilamowski diode [7] adds diffusions to increase breakdown voltage. Depletion layers merge under reverse bias and a breakdown voltage similar to that of a pn junction is achieved.
SBC Process: Buried Layer Isolation (isolation of two BJTs from each other)

- Adjacent transistors separated by p-diffusion through the epitaxial layer.
- Diffusion must be wide enough to prevent space charge layers from merging.
- Base-isolation spacing must be large enough so that space charge layers do not merge.
- If the n+ buried layer intersects the p+ isolation, then breakdown voltage of the junction will decrease, capacitance will increase – not desirable and not allowed, if possible.

SBC Transistor Layout Considerations: Design Rules

<table>
<thead>
<tr>
<th>TABLE 10.1</th>
<th>Bipolar Transistor Design Rules (in μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum base-to-emitter spacing</td>
<td>2 μm</td>
</tr>
<tr>
<td>Minimum base-to-emitter diffusion</td>
<td>3 μm</td>
</tr>
<tr>
<td>Emitter-base junction depth</td>
<td>10 μm</td>
</tr>
<tr>
<td>Collector-base junction depth</td>
<td>5 μm</td>
</tr>
<tr>
<td>Minimum emitter-to-collector spacing at substrate</td>
<td>3 μm</td>
</tr>
<tr>
<td>Minimum base-to-emitter spacing at surface</td>
<td>2 μm</td>
</tr>
<tr>
<td>Minimum collector contact - diffusion to emitter spacing</td>
<td>1 μm</td>
</tr>
<tr>
<td>Minimum collector contact - diffusion to base spacing</td>
<td>1 μm</td>
</tr>
<tr>
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<td>3 μm</td>
</tr>
<tr>
<td>Minimum base-to-emitter spacing</td>
<td>5 μm</td>
</tr>
<tr>
<td>Emitter-base junction depth</td>
<td>2 μm</td>
</tr>
<tr>
<td>Collector-base junction depth</td>
<td>10 μm</td>
</tr>
</tbody>
</table>

Figure 10.17
SBC transistor layout using the design rules in Table 10.1
Advanced Bipolar Devices

Oxide Isolation

FIGURE 10.18
Process sequence for a high-performance oxide-isolated bipolar transistor.
(a) Buried-layer formation;
(b) epitaxial layer growth;
(c) mask for selective oxidation;
(d) boron implant prior to recessed oxide growth;
(e) selective oxidation;
(f) base mask and boron base implantation;
(g) emitter, base contact, and collector contact mask;
(h) p+ base contact implantation;
(i) arsenic implantation for emitter and collector contact;
(j) structure completed with multilayer metallization.
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Oxide Isolation (cont.)

FIGURE 10.18
Process sequence for a high-performance oxide-isolated bipolar transistor.
(g) Buried-layer formation;
(h) epitaxial layer growth;
(i) mask for selective oxidation;
(j) boron implant prior to recessed oxide growth;
(k) selective oxidation;
(l) base mask and boron base implantation;
(m) emitter, base contact,
(n) and collector contact mask;
(o) p+ base contact implantation;
(p) arsenic implantation for emitter and collector contact;
(q) structure completed with multilayer metallization.
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Advanced Bipolar Devices

Trench Isolation

FIGURE 10.19
A high-performance bipolar transistor structure with an $f_T$ of 10 GHz. (a) Isolation is achieved using deep-trench isolation with polysilicon and silicon dioxide refill; (b) structure following selective oxidation; (c) $p^+$ polysilicon deposited and patterned; (d) diffusion from doped polysilicon forms the extrinsic base region and base contacts; a self-aligned implantation forms the intrinsic base; (e) diffusion from $n^+$ polysilicon forms the emitter and the emitter and collector contacts of the transistor. Copyright 1997, IEEE. Reprinted with permission from Ref. [8].

Advanced Bipolar Devices

SiGe HBT

FIGURE 10.20
(a) Cross section of an epitaxial base silicon germanium heterojunction bipolar transistor (SiGe HBT) (b) Photomicrograph of actual structure with 5 μm deep trench isolation. Copyright 1985, IEEE. Reprinted with permission from Ref. [9].
Advanced Bipolar Devices
SiGe HBT

![Graph showing SiGe HBT impurity profile. The same profile applies to high performance silicon BJTs if the Ge is eliminated. Copyright 1985, IEEE. Reprinted with permission from Ref. [9].]

Other Bipolar Isolation Techniques
Collector Diffused Isolation

- Figure 10.22 - Cross section of a transistor fabricated with the CDI process [18]
Other Bipolar Isolation Techniques

Dielectric Isolation

![Diagram of Dielectric Isolation](image)

**Figure 10.23**
Several steps in the dielectric isolation process: (a) High performance bipolar transistors and (b) passive components fabricated on a SIMOX wafer using shallow trench isolation. Copyright 1999, IEEE, Reprinted with permission from Ref. [13].

Other Bipolar Isolation Techniques

SIMOX

![Diagram of SIMOX Process](image)
BiCMOS Processes
CMOS + Bipolar

FIGURE 10.25
BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs [15, 16, 17].
BiCMOS Processes
CMOS + Bipolar (cont.)

FIGURE 10.25
BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

End of Chapter 10
Work all the examples in this Chapter