ELEC 5730 – MICROELECTRONIC FABRICATION
(Elective for ECPE, Elective for ELEC)

Catalog Data: ELEC 5730. MICROELECTRONIC FABRICATION (3) LEC. 2, LAB. 3. Pr., ELEC 2210 or departmental approval. Introduction to monolithic integrated circuit technology. Bipolar and MOS processes and structures. Elements of layout, design, fabrication, and applications. Experiments in microelectronic technologies.

Instructor: Dr. Hulya Kirkici
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Email: kirkihu@auburn.edu


References: Archival journal and conference papers selected by the instructor.

Course Objectives:
1. To develop an understanding of the basic processes used in fabrication of bipolar and MOS integrated circuits.
2. To practice actual fabrication in the microelectronics laboratory.
3. To provide an exposure to the literature in the field of microelectronic fabrication.

Prerequisites by topic:
1. Elementary understanding of bipolar junction transistors.
2. Elementary understanding of field-effect transistors
3. Elementary understanding of electronic circuits

Grading (Fall 2015):
Typical methods for evaluating student performance:

<table>
<thead>
<tr>
<th>Component</th>
<th>ELEC 6730</th>
<th>ELEC 5730</th>
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<tbody>
<tr>
<td>Exams (total 2 during the semester)</td>
<td>45%</td>
<td>40%</td>
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<tr>
<td>Homework (approximately 10)</td>
<td>5%</td>
<td>10%</td>
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<tr>
<td>In-Class Work (approximately 10)</td>
<td>5%</td>
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<td>Laboratory notebook</td>
<td>20%</td>
<td>25%</td>
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<td>Final exam (during finals, 1)</td>
<td>25%</td>
<td>20%</td>
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Homework:
Homework problems will be assigned throughout the semester to reinforce the class material (May or may not be collected for grading, if not collected, a pop-quiz will replace the HW assignment).

Computer use
IC layout tools; SUPREME process simulator

Special Accommodations: It is the policy of Auburn University to provide accessibility to its programs and activities, and reasonable accommodation for persons defined as having a disability under Section 504 of the Rehabilitation Act of 1973, as amended, and the Americans with Disabilities Act of 1990. Students who need special accommodations should make an appointment to see the instructor as soon as possible or contact the Students with Disabilities Office at (334) 844-5943 (Voice/TT).

Class attendance: Class attendance is strongly encouraged. There will be no make-up given to any one who misses any of the assignments including the exams, HWs, In-Class work, and Quizzes, unless you furnish the instructor with a university approved excuse. If you miss an exam and have an official excuse then arrangements must be made with the Instructor before the end of the semester.
**Course Topics:**

1. Historical Overview / Semiconductor physics overview

2. Introduction to Integrated Circuit Processing: Photolithography Process, Dark Field/Light Field, Basic NMOS Process, Basic CMOS Process, Basic Bipolar Process

3. Lithography: Clean Room/Wafer Cleaning, Photoresist Application, Exposure, and Developing, Wet & Dry Etching, Mask Fabrication and Layout/Reduction/Step & Repeat

4. Thermal Oxidation: Reaction Kinetics, Derivation of Fick’s First Law, Linear and Parabolic Rate Constants, Oxidation Tables


8. Thin Film Deposition: High Vacuum Systems, Electron Beam Evaporation/Sputtering, Chemical Vapor Deposition, Epitaxial Growth/Molecular Beam Epitaxy


11. Yield: Defect Formation, Edge Dislocation, Stacking Faults

12. MOS Process Integration

13. Bipolar Process Integration
**Laboratory projects**
*(including major items of equipment and instrumentation used)*
*(Lab Experiment Sequence and number of experiments are subject to change depending on the availability of the equipment during that time):*

*Laboratory Attendance and Participation is Mandatory*

An integrated circuit chip is designed, fabricated and tested by the students using the facilities of the microelectronics fabrication laboratory.

**Laboratory Topics:**

WEEK 1: Safety manual, Introduction to LASI, Introduction to the AUNMOS design rules  
WEEK 2: Detailed instruction on LASI, Description of test structures, Test structure homework  
WEEK 3: Safety test, Process simulation using SUPREM program, Assign SUPREM homework, NMOS and test structure design layout  
WEEK 4: Wafer characterization, Oxide growth, Ellipsometery  
WEEK 5: Photolithography, Mask alignment, Wet chemical etching  
WEEK 6: MOS capacitance-voltage measurements, Mask 1 (Active) application, Field oxide etching, Gate oxide growth  
WEEK 7: Low pressure CVD of polysilicon, Mask 2 (Poly) application, Polysilicon patterning and etching  
WEEK 8: Phosphorus dopant deposition and drive in, Diffusion from spin on dopants, Diffusion furnace operation  
WEEK 9: Mask 3 (Contact) application, Contact hole etching, Plasma etching  
WEEK 10: Vacuum deposition of aluminum, Electron beam evaporation, Sputter deposition, Mask 4 (Metal) application, Aluminum patterning and etching, Alloy wafers  
WEEK 11: Basic operation of the HP4145 DC parameter analyzer, Characterization and parametric measurement of finished die  
WEEK 12: Characterization and parametric measurement of finished die, continued  
WEEK 13: Characterization and parametric measurement of finished die, continued

*Lab attendance:* Attendance to the lab-lecture attendance is strongly encourages. You are expected to finish your task for the lab during the week that is assigned to you. You will receive a “lab-completion” check at the end of each week. *If you miss any one lab assignment (didn't get completion check) at the end of the semester, you will automatically receive an F grade for this course regardless of the performance in other assignments.*