

A 2.4GHz Power Amplifier Driver Used in A WLAN IEEE 802.11b/g Transmitter Front-End

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Abstract — This paper presents a 2.4GHz power amplifier driver used in a WLAN IEEE 802.11b/g transmitter front-end which employs a walking IF architecture. The power amplifier driver is implemented in a 50GHz 0.5 μ m SiGe BiCMOS technology. And it consists of a differential cascode amplifier stage, an emitter follower and a common-emitter amplifier. It dissipates 28mA current under a 3.3 V power supply, and occupies 0.5 \times 0.56mm² die areas. The power amplifier driver exhibits 12dB power gain and delivers -10dBm power to an off-chip power amplifier with 50 Ω input impedance. It has good suppression of LO and image spurs, and its IIP3 is +10.2dBm.

Index Terms — Power amplifier driver, power amplifier, walking IF, SiGe BiCMOS technology, WLAN 802.11b/g transmitter

I. INTRODUCTION

With the increasing development of wireless communications, the simple low-cost single chip WLAN 802.11 transceiver is now considered for personal communication terminal applications [3-7]. The future WLAN systems are demanded to increase the link throughput and reliability, the network capacity and the transmit range. And it should be seamlessly merged into high-data rate wired networks.

Power amplifier driver is one of the most important circuit blocks of the WLAN transmitter front-end. It is typically the most power-hungry and die-area consuming building block. As the last stage of the transmitter, the power amplifier driver should deliver a considerable power to the off-chip power amplifier. Although the consumed current and the output power of the driver stage are smaller than that of power amplifier, the power amplifier driver also suffers some challenges as same as power amplifier. It should trade off efficiency and linearity, and this tradeoff is very important in a fully monolithic implementation.

In this paper, the design of a 2.4GHz differential input, single-ended output power amplifier driver used in a WLAN IEEE 802.11b/g transmitter front-end is presented. The power amplifier driver is implemented in a 50GHz 0.5 μ m SiGe BiCMOS technology, consisting of a differential cascode amplifier stage, an emitter follower, and a common-emitter amplifier. It consumes 28mA current under a 3.3V power supply, and occupies 0.5 \times 0.56mm² die areas.

II. TRANSMITTER FRONT-END ARCHITECTURE

Because of the low cost and low power demand, the choosing of WLAN transmitter architecture is thus critical. Compared with direct conversion architecture, superheterodyne architecture has a high level of performance, but requires two synthesizers. In order to obtain the benefit of a direct conversion radio, but retain the performance advantages of the superheterodyne radio, a walking IF architecture is used in this WLAN 802.11b/g transmitter where the RF LO is 4 times the IF LO. As a result, both RF and IF LO reference can be derived from a single Frac-N synthesizer.

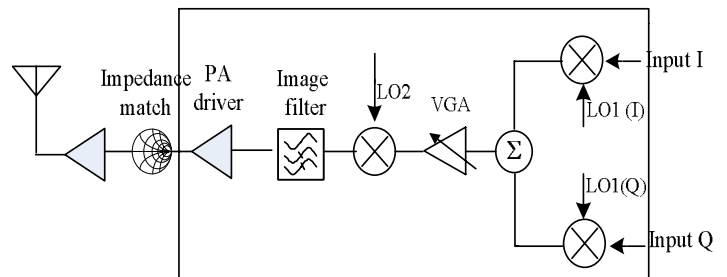


Fig.1 Transmitter architecture diagram

Fig.1 shows the architecture diagram of the WLAN 802.11b/g transmitter front-end. Here, the baseband I and Q channels undergo quadrature modulation which includes two mixers at an intermediate frequency (IF). The summation of the two mixers would remove the unwanted sideband. A two gain mode IF VGA follows the IQ modulator which could also help to suppress the harmonics of the IF signals. After converted by the RF mixer, the RF signal is delivered to a high efficiency 2.4GHz off-chip power amplifier with 50 Ω input impedance through the on-chip power amplifier driver.

There is an image filter between the RF mixer and power amplifier driver, because the simple up-conversion mixing operation produces both the wanted and unwanted sidebands with equal magnitudes. Thus the unwanted sideband must be rejected by a large factor, typically 50 to 60dB. Owing to higher center frequency, the filter is typically a passive, relatively expensive off-chip device [2].

However, if all of the transmitter front-end circuit blocks are implemented on-chip, the filter would not work so well. Then, as the last stage of the transmitter front-end, the power amplifier driver should act to remove the unwanted sideband and other frequencies harmonics as well. This is realized by a tank formed by a capacitor, an inductor and a resistor which

will be shown in next section.

Besides output power, the important properties of the power amplifier driver are a matched output impedance and linearity. Nonlinearities in the power amplifier driver introduce both spectral re-growth and signal compression, as well as phase distortion, thus distorting the original signal constellation for digital modulations. The linearity of the power amplifier driver presented in this paper will also be discussed in next section.

III. POWER AMPLIFIER DRIVER DESIGN

The power amplifier driver used in the WLAN 802.11b/g transmitter front-end is shown in Fig.2. It is differential input, single-ended output, consisting of a differential cascode amplifier, an emitter follower and a common-emitter amplifier. The transistors are biased by current sources which are mirrored from a band-gap-referenced bias current source.

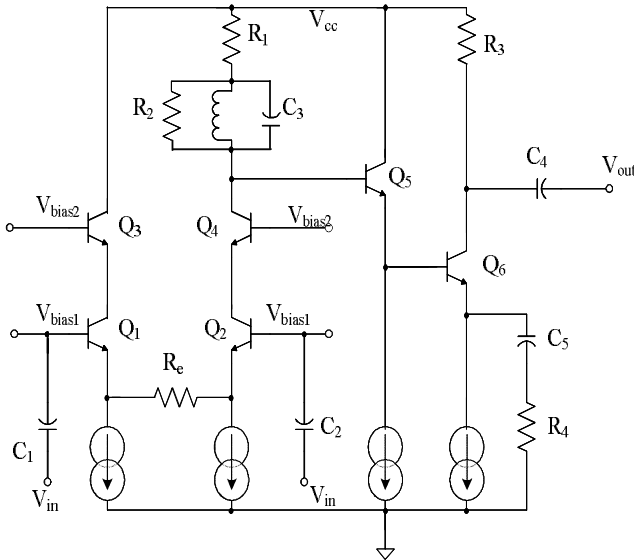


Fig.2 Schematic of power amplifier driver

A. Differential Cascode Amplifier Stage

The differential input amplifier can be directly cascaded to the Gilbert cell up-converter RF mixer. The cascode architecture is used over the common-emitter topology because at higher frequencies the extra transistors act to reduce the Miller effect and have superior reverse isolation (S12). Additional, the breakdown voltage of the transistors in this cascode topology is about twice that of other configurations. However, the cascode also suffers from reduced linearity due to the stacking of two transistors, which reduces the available output swing. To this problem, a tank formed by an inductor, a capacitor (C_3) and a resistor (R_2) is used to provide headroom. Besides this, the tank resonates at 2.4GHz, thus some other frequency harmonics, LO signals and the image spurs generated by RF mixer can be rejected.

Resistor R_1 is used to lower the base voltage of Q_5 in order to improve the linearity of the emitter follower. However, choosing R_1 should be critical, because R_1 also reduces the

output swing of the cascode amplifier.

The cascode amplifier stage also acts as a differential to single-ended converter. Since the off-chip power amplifier is usually single-ended input, it is more convenient for the single-ended output power amplifier driver to be matched to it, avoiding the use of an external element such as a balun. Thus the equivalent circuit of this stage is shown in Fig.3. In this case, v_{in} is half of the differential input.

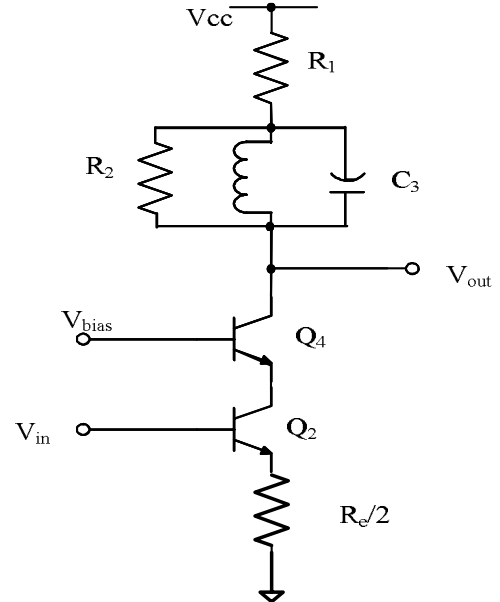


Fig.3 Cascode stage equivalent circuit

In this cascode architecture, the current i_{c2} through the transistor Q_2 is about the same as the current i_{c4} through the transistor Q_4 , since the common-base amplifier has a current gain of approximately 1. The gain of this cascode architecture is the same as for the common-emitter amplifier.

The gain of the cascode amplifier at the resonance frequency (2.4GHz) of the tank in the collector, ignoring the effect of C_{cb} , is found with the aid of Fig.4 and given by [1]

$$\frac{v_{out}}{v_{in}} = \frac{-g_m R_L}{\left(1 + \frac{Z_E}{Z_\pi} + g_m Z_E\right)} \approx -\frac{R_L}{Z_E} \quad (1)$$

where Z_E is the impedance of the emitter degeneration. In this paper, Z_E is equated to $R_e/2$, and R_L is equated to (R_1+R_2) . Thus, as the emitter degeneration becomes larger, the gain ceases to depend on the transistor parameters and becomes solely dependent on the ratio of the two impedances. This means that the circuit becomes less sensitive to temperature and process variations [1].

If the input impedance of the amplifier is matched to R_s , then the gain can be written out in terms of source resistance and f_T . v_{out} in terms of i_x in Fig.4 can be given by[1]

$$v_{out} = -g_m v_\pi R_L = -g_m i_x Z_\pi R_L \quad (2)$$

Noting that i_x can also be equated to the source resistance R_s as $i_x = v_{in} / R_s$:

$$\frac{v_{out}}{v_{in}} = -\frac{g_m Z_\pi R_L}{R_s} \quad (3)$$

Assuming that Z_π is primarily capacitive at frequency of interest:

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{g_m R_L}{R_s \omega_0 C_\pi} = \frac{R_L \omega_T}{R_s \omega_0} \quad (4)$$

where ω_0 is the frequency of interest[1].

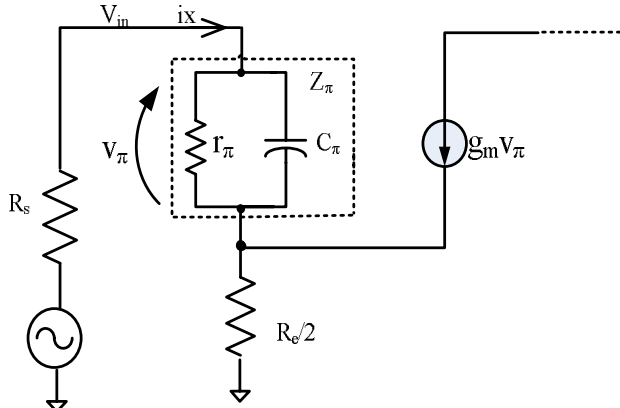


Fig.4 Equivalent circuit used to find the input impedance and gain

B. Common-Emitter Amplifier Stage

A typical common-emitter amplifier with emitter degeneration is shown in Fig.5. The bias current is determined by the bias base voltage and the degeneration resistance R_e . However, resistances have high temperature coefficient. The bias current of the transistor would not be stable if the temperature changes, especially for the large bias current of the power amplifier driver stage. The gain and the linearity of the stage would be seriously influenced by the temperature. To resolve this problem, the common-emitter amplifier used in this power amplifier driver is shown in Fig.6.

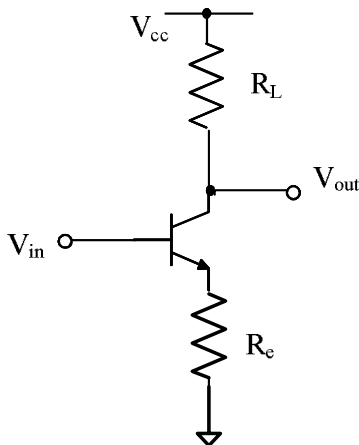


Fig.5 Typical common-emitter amplifier with emitter degeneration

In Fig.6, the bias current of the transistor is supplied by the

current source I_{bias} . It is mirrored from a band-gap-referenced bias current source, which has low temperature coefficient. So the bias current is more stable than that in Fig.5. Capacitance C_5 and resistance R_4 provide signal path, working the same as the degeneration resistance R_e in Fig.5. And they will not influence the DC operation.

Compared to the input stage of the power amplifier driver, the output stage includes only one transistor. It is because that the bias current of this stage is much larger than that of the input stage, and the large currents would introduce much higher loss with more active devices in the signal path. Additional, a resistor load R_L is used in this stage instead of an inductor in order to save the die area, while delivers the required power.

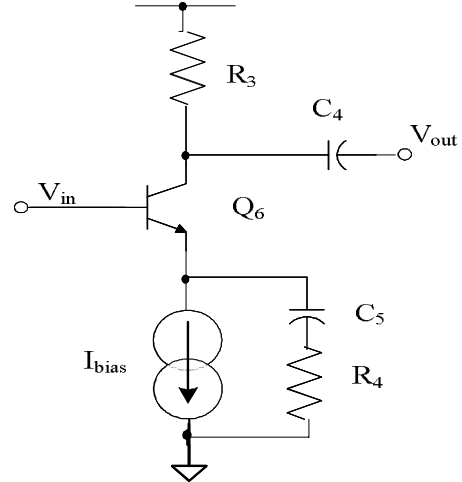


Fig.6 Common-emitter amplifier used in this paper

C. Linearity

The linearity of the power amplifier driver most depends on the linearity of the cascode amplifier stage and the common-emitter stage.

In the cascode stage, as mentioned above, the stacking of two transistors would reduce the linearity, because they reduce the available output swing. A tank is used to provide headroom. The resistor R_L over the tank should also be as small as possible. It trades off the linearity of this stage and the following emitter follower stage. Besides this, choosing the bias voltage V_{bias1} and V_{bias2} of the transistors is critical to improve the linearity.

Although the die areas are saved to place a resistor R_L instead of an inductor as the load of the common-emitter, the linearity would be reduced. The resistor R_L should be small enough to provide available headroom for the output swing.

Simulated in a two-tone test, the IIP3 of the power amplifier driver is +10.2dBm.

IV. MEASURED RESULTS

Fig.7 shows the die photograph of the 2.4GHz power amplifier driver, which occupies $0.5 \times 0.56 \text{mm}^2$ die areas.

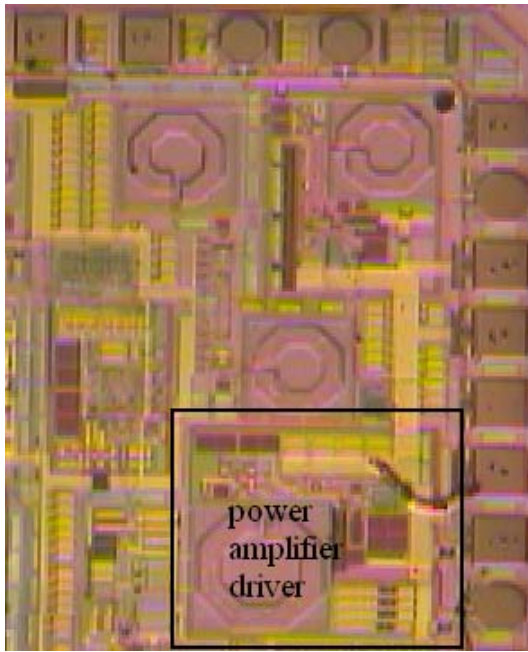


Fig.7 Die photo of the power amplifier driver

Fig.8 shows the output power measured at the output of the power amplifier driver which is matched to 50Ω, the same impedance as the input of the off-chip power amplifier. The frequency of carrier signal is 2.4GHz (2.399978GHz in Fig.8). When the 500 KHz quadrature signals are added to the IQ modulator, one sideband of 2.4005GHz (2.400478GHz in Fig.8) is suppressed by 25dB compared with the other sideband of 2.3995GHz (2.399478GHz in Fig.8), and the carrier signal is suppressed by 6dB. Fig.9 shows that the LO signals of 3.2GHz is 46dB smaller than the carrier signals of 2.4GHz, and the 4GHz image spur generated by RF mixer is very small, even smaller than the noise floor. It is shown that the transmitter has good suppression of LO and image spurs.

Fig.10 gives the measured error-vector-magnitude (EVM) for typical IEEE 802.11b/g transmission with 64 QAM OFDM modulation of the whole transmitter front-end. The measured EVM is 4.49%rms.

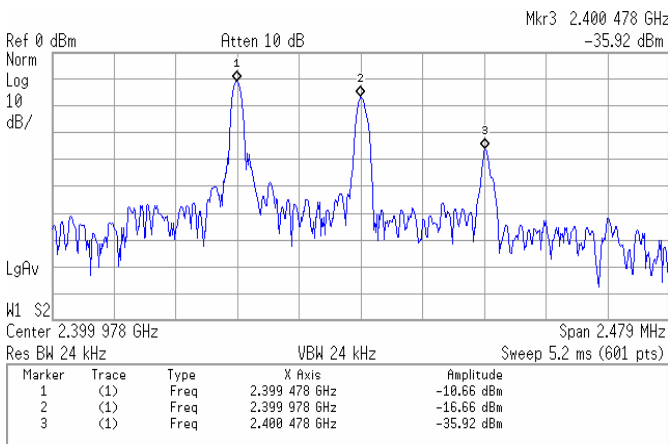


Fig.8 Output power measured at the output of the power amplifier driver

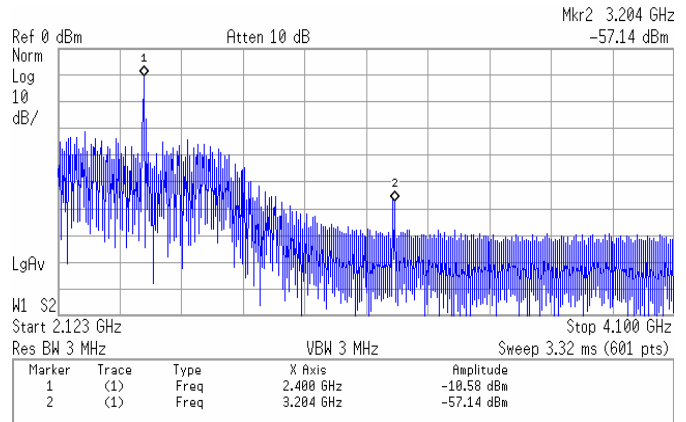


Fig.9 Suppression of LO signals and image spurs

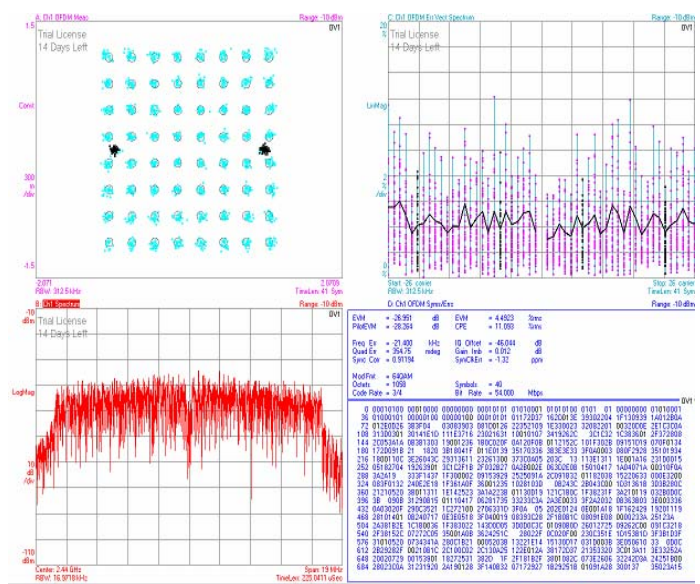


Fig.10 Measured EVM for IEEE 802.11b/g transmission of the transmitter front-end, EVM=4.49%rms

V. CONCLUSION

This paper presents a 2.4GHz power amplifier driver used in a WLAN IEEE 802.11b/g transmitter front-end. The current dissipation of the power amplifier driver is 28mA and the power supply is 3.3V. It has 12dB power gain with the IIP3 of +10.2dBm, delivering -10dBm power to an off-chip power amplifier. The WLAN transmitter front-end has good suppression of LO and image spurs, and the measured EVM is 4.49%rms.

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