

A Fully Integrated Zero-IF Mobile TV Tuner RFIC for S-band CMMB Application

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Abstract- We present a single-chip tuner RFIC for the newly established Chinese Mobile Multimedia Broadcasting (CMMB) standard. This mobile digital TV tuner covers the CMMB frequencies from 2.635GHz to 2.660GHz. Implemented in a 0.35 μ m SiGe technology with 4mm² die size, this tuner IC achieves noise figure of 2dB, input sensitivity of -100dBm, IIP3 of 17dBm, and total power of 162mW under a 2.8V supply.

I. INTRODUCTION

The mobile TV has been evolved into a wide variety of standards in different countries. With DVB-H established in Europe and US, ISDB-T in Japan and DMB in Korea, China recently announced the adoption of her own mobile TV standard CMMB based on Satellite-Terrestrial Interactive Multi-service Infrastructure (STiMi). As Fig. 1 shows, the STiMi system is a mixed satellite and terrestrial wireless broadcasting system designed to provide audio, video and data service for handheld receivers with less than 7 inch wide LCD display, such as PMP, mobile phone, PDA and UMPC. CMMB utilizes two S-band satellites to cover the digital video broadcasting (DVB) over the wide area. In the populated metropolitan areas, CMMB utilizes the cellular base stations to enhance the digital video transmission in order to allow DVB reception with low-cost terminals. The satellite and terrestrial complementary network is combined to create a Single Frequency Network (SFN) using the 2635-2660 MHz band. The CMMB service operates in the S-band frequency with 25MHz bandwidth in order to offer 25 video and 30 radio channels.

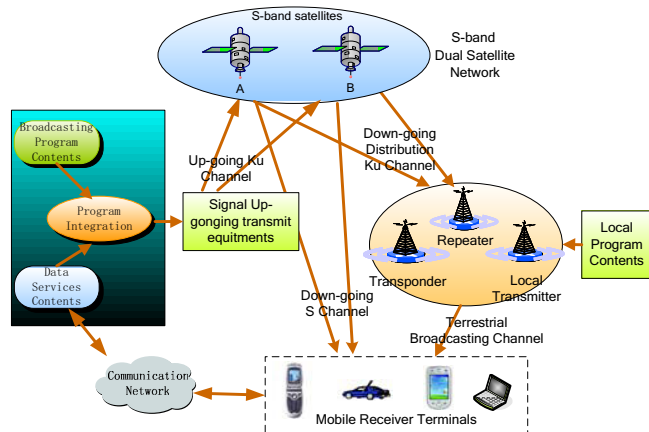


Fig.1 CMMB STiMi system

This paper presents the first reported CMMB tuner RFIC. In order to handle both satellite and terrestrial receptions, the

CMMB tuner requires very high input sensitive and wide dynamic range, which requires very low noise and high linearity; small form factor and low cost, which requires high degree of integration; and low power consumption.

This CMMB tuner RFIC achieves high input sensitivity of -100dBm and high linearity of 17dBm IIP3. The power consumption of 162mW is optimized for longer mobile usage, and the chip is design to be compact with only 4mm² die size.

In Section II, the CMMB tuner RFIC design will be discussed in detail. Section III presents the measurement results of the critical blocks and the whole receiver system.

II. CMMB TUNER RFIC DESIGN

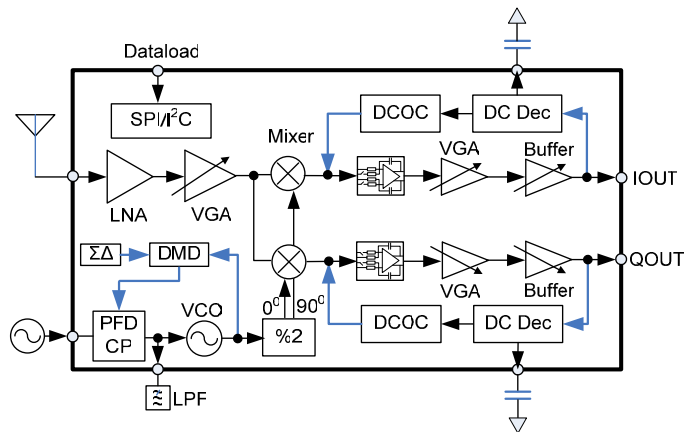


Fig. 2 Block diagram of the CMMB tuner RFIC.

As illustrated in Fig. 2, the fully integrated CMMB tuner includes all RF receiver functions without using any off-chip SAW filters. The front-end of the CMMB tuner consists of a single-ended low-noise amplifier (LNA) with dual gain mode (HG/LG), an RF VGA with continuously controlled variable gain, and a degenerated double-balanced Gilbert cell down-conversion I/Q mixer.

The LNA has a high-gain mode and a low-gain mode as shown in Fig. 3. For the high gain mode, an inductively degenerated cascode structure is used to achieve 15dB power gain and 1.6dB NF while drawing only 4mA. For the low gain mode, the MOS switch M0 is turned on, and the attenuation resistor R1 are used for -7dB power loss. The capacitor C1 is used for ac coupling. The IIP3 in the low gain mode can achieve more than +20dBm. In the high gain mode, the output capacitor C2 is designed to conjugate-match the output impedance of the LNA with that of the following RFVGA for

best power transmission. In the low gain mode, the value of the C2 may not be on the power matched value, but it is not important since the gain is attenuated in this mode.

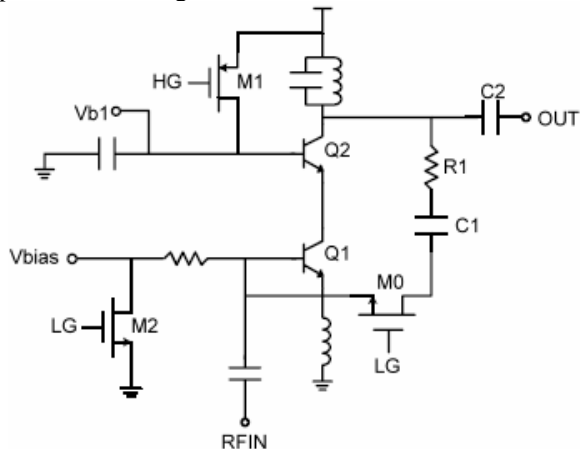


Fig. 3 Simplified schematics of the two-mode LNA.

In Fig. 3, the MOSFET switch M0, M1 and M2 are used to switch the gain of the LNA. In the high gain mode, all the switches are turned off, while in the low gain mode, all the switches will be turned on. In our design, we added the switch M1 for keeping the cascode transistor Q2 working in the safe area in the low gain mode. When the input signal is large and the circuit is in the low gain mode, the transistor Q1 is shut down by switch M2, the collector voltage of Q1 will be low without the switch M1. As a result, almost the entire supply voltage adding the large input signal swing will be added to the collector-emitter junction of the transistor Q2, potentially causing break down. However, with M1 turned on in the low gain mode, the base and emitter voltage of Q2 will be pulled to high and the collector-emitter junction voltage will be greatly reduced, which helped to keep Q2 working in the safe region in the low gain mode.

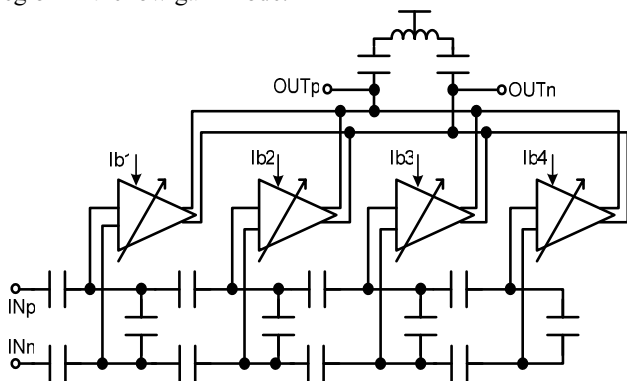


Fig.4 Simplified RFVGA schematic

The RF VGA consists of a three-stage capacitive attenuator with 13dB per stage attenuation and four amplifiers which smoothly switch outputs from the ladder attenuator, as shown in Fig. 4. The common load of the four core amplifiers is constructed by L and C1, C2, which act as a LC tank to

filter out the signal out of the band. This LC load also greatly released the critical headroom requirement, thus improved the gain and the linearity performance of the circuit.

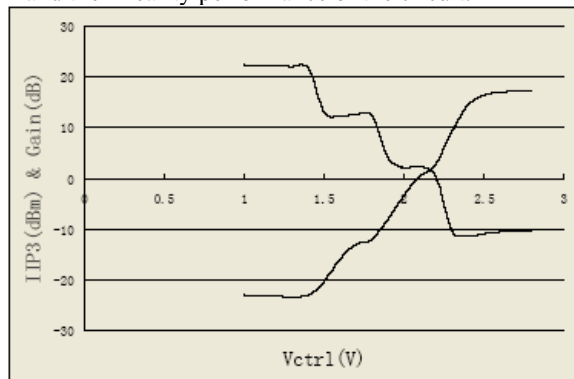


Fig. 5 Simulated gain and IIP3 dependence on control voltage of RFVGA

Fig. 5 shows the simulated IIP3 and gain of the RFVGA as control voltage changes. Comparing to the VGA used in [1], the proposed VGA greatly improves linearity and gain control range using the same amplifier structure with alternate current biasing.

A quadrature mixer shown in Fig. 6 has been developed to provide improved image rejection ratio (IRR) and reduced phase error [2]-[4]. It is basically a combination of two Gilbert mixers with shared transconductance stages. The total signals turn on in the order: LOQp, LOIp, LOQn, LOIn. For example, when the RF signal on transistor Q1 is high and the LOQp signal on Q7 is high, the voltage of the collector terminal of Q1 is pulled high and the transistors Q3, Q4 and Q8 are shut off. In this way, the total available current must flow through only a selected transistor according to the local signal sequence. This mechanism is called Q-I mutual interference and is useful for phase error suppression. In Fig. 6, the capacitors C1 to C4 are used to filter out the RF and LO frequency and their harmonics.

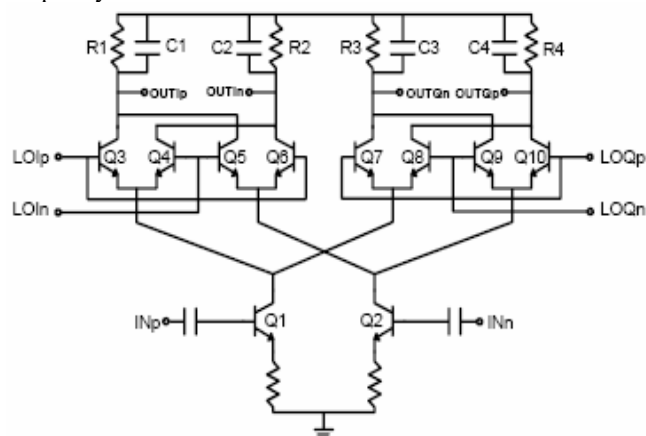


Fig. 6 Quadrature down-conversion I/Q mixer

The CMMB tuner IC comprises a baseband VGA, an 8th order Chebyshev filter and a DC offset compensation loop. The VGA is a cascode amplifier with current shunt from the load for gain tuning. The VGA achieves more than 40dB gain

tuning and 18dBm IIP3 with temperature compensation. Fig. 7 shows a detailed structure of the baseband filter.

The baseband output is filtered to extract its DC components used for DC offset compensation for the down mixer. The DC offset at the mixer output is measured as 56 mV without compensation and it reduces to 6mV when the compensation loop is closed. The DC offset compensation loop consumes 412uA. The 8th order Chebyshev filter is implemented using Op-amp-RC integrator in a leapfrog configuration as shown in Fig. 7. It is less sensitive to the variation of component values, comparing to cascaded biquad. The filter provides 0.5dB passband ripple and -35dB attenuation at 6MHz with the cutoff frequency at 4MHz. An on-chip frequency auto-calibration is accomplished using a capacitor switching technique. The 5-bit capacitor arrays are controlled by the frequency auto-tuning circuits shown in Fig. 7. After calibration, the auto-tuning circuits can be turned off without additional power consumption.

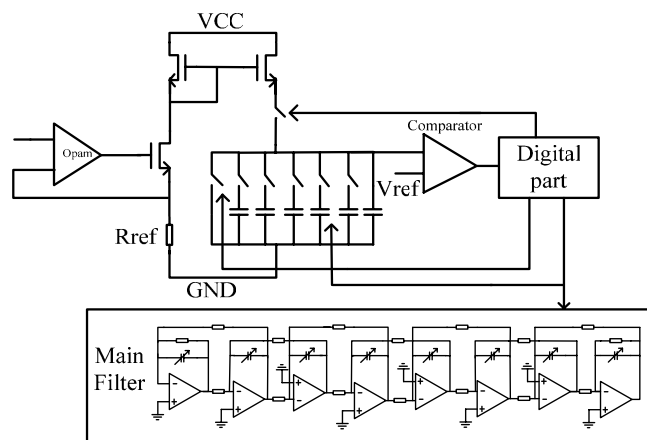


Fig. 7 Simplified 8th order Chebyshev filter with corner frequency auto-calibration.

The CMMB tuner includes an Fractional-N PLL comprising low noise PFD, current variable charge pump, a low phase noise VCO, P/P+1 dual modulus divider (DMD), and a 3 order MASH sigma-delta noise shaping digital block. DMD input is a high speed prescaler with 32 or 33 divide ratios. DMD provides a divide range from 352 to 354. The VCO output is divided by 2 as LO signal which can cover the 2635MHz to 2660MHz. This divider also provides the I/Q phase LO signal for I/Q down-conversion mixer. The VCO is designed to be a wide frequency tuning range from 5.1GHz to 5.75GHz. Wide-tuning range PMOS VCOs are designed to allow the tank referenced to the ground, which leads to lower phase noise. The VCO design provides good ambient-proof characteristics over process, temperature and frequency variations. The in-band phase noise of the phase-locked loop is measured as -90dBc/Hz at 100kHz offset.

III. CMMB TUNER RFIC MEASUREMENT RESULTS

The die photo of CMMB tuner RFIC with a compact die size of 4mm² is shown in Fig. 8. It is the first CMMB tuner RFIC reported so far.

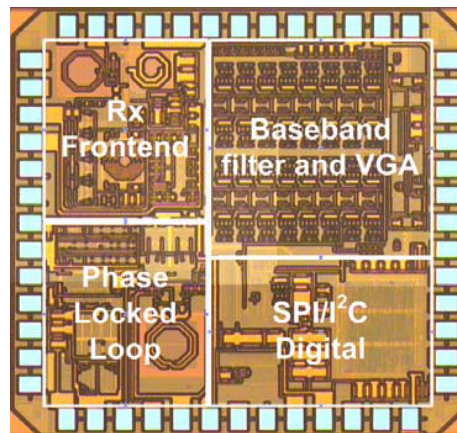


Fig. 8 Die photo of the CMMB tuner RFIC.

Fig. 9 shows the measured LNA S11 and NF plots. It can be seen from the NF curve that in the operation band from 2.635GHz to 2.660GHz, the NF is measured below 2.25dB.

Fig. 10 shows the measured RFVGA gain versus control voltage. The gain varies from -21dB to 19dB when the control voltage changes from 1.1V to 2.5V, achieving more than 40 dB variable gain. The measured curve fits the simulated one well. Fig. 11 shows the measured baseband VGA gain versus control voltage. The gain varies from about 7 dB to 48dB in 85 Degree Celsius ambient temperature. In the room temperature about 25 Degree, the measured curve fits the simulated curve well.

The measured baseband filter transfer characteristics are shown in the Fig. 12. The filter shows a cut-off frequency of 4.13MHz at -10 Degree Celsius and 4.41MHz at 85 Degree when the corner frequency auto-calibration circuit is turned on.

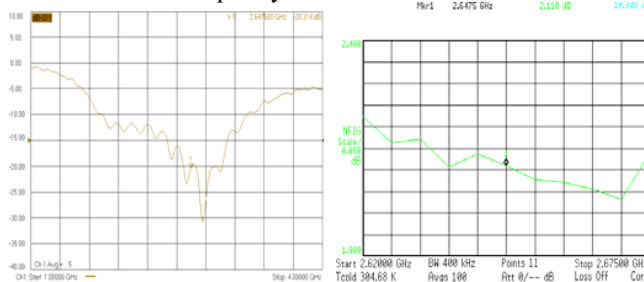


Fig. 9 Measured CMMB tuner LNA S11 and NF.

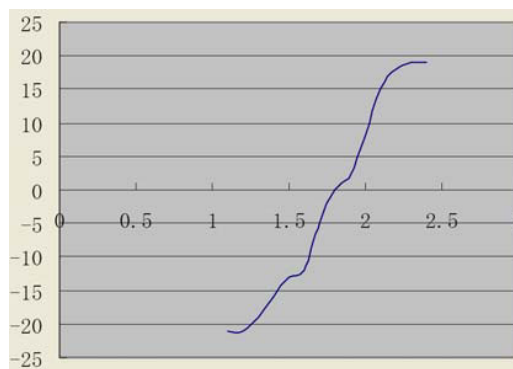


Fig. 10 Measured gain versus control voltage of RFVGA.

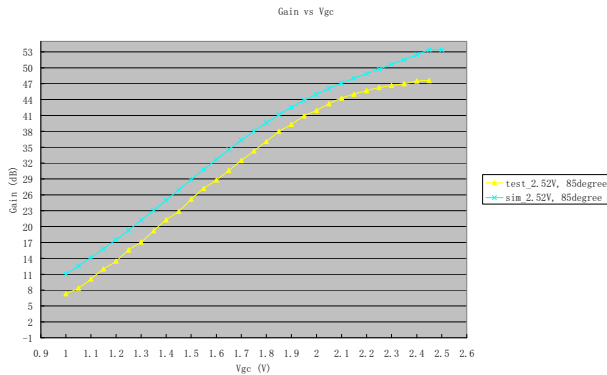
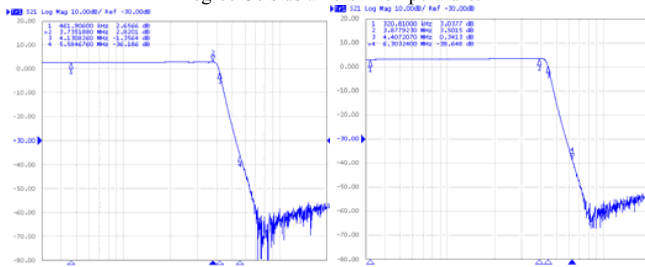


Fig. 11 Measured gain versus control voltage of baseband VGA in 85 Degree Celsius ambient temperature.



(a) -10 Degree Celsius (a) 85 Degree Celsius
Fig. 12 Measured tuner baseband filter transfer function at different temperature

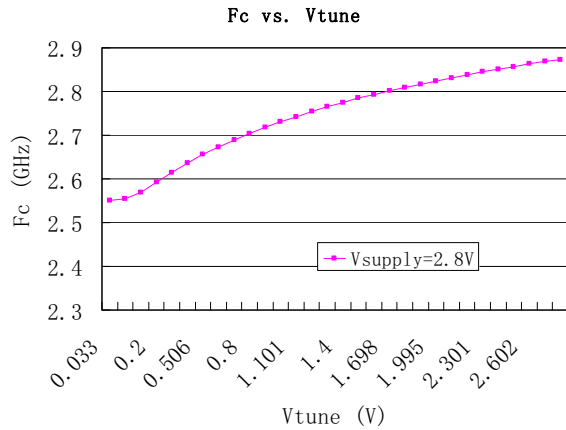


Fig. 13 Measured LO frequency tuning curve

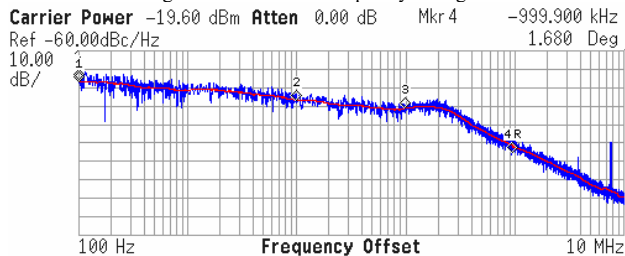


Fig. 14 Measured LO phase noise

Fig. 13 shows the measured LO frequency tuning curve. When VCO tuning VCO is varied from 0.5V to 2.5V, the LO frequency can covers the frequency band from 2.6GHz to 2.85GHz. The VCO frequency is twice the LO frequency from 5.2GHz to 5.7GHz.

Fig. 14 shows the measured LO phase noise. The carrier frequency is 5295MHz, the LO output power is -19.6dBm. The measured integrated rms phase noise is about 1.68 Degree.

Table 1 summarizes the tuner performances in which tuner sensitivity is measured when the output signal amplitude is beyond -20dBv and the waveform looks without obvious distortion. The tuner IC achieves low noise figure, high input sensitivity and high linearity, while consuming low power.

Table.1 Summary of CMMB tuner RFIC performance.

Parameters	Conditions	Meas.	Unit
Input signal power	LNA input	-100~0	dBm
IIP3	@0dB power gain	17	dBm
IIP2	@0dB power gain	44	dB
Noise figure	High gain	2.2	dB
System gain	Power gain	-15~89	dB
LO phase noise	@10kHz @100kHz @1MHz	-84 -90 -113	dBc/Hz
VCO tuning range		5.1~5.75	GHz
IQ amplitude mismatch		-32	dBc
Pass band		3.8	MHz
Pass band ripple		<1	dB
Stop band rejection		>50	dB
Settling time	DCOC PLL	<100 200	μ s μ s
Power consumption	Power supply: 2.5~3.1V Temp range: -40~85 ^o C	46~58	mA
Current consumption	Sleeping mode	97	μ A
Die size		2x2	mm ²

IV. CONCLUSION

In conclude, this paper presents a single-chip tuner RFIC for CMMB S-band applications which is never reported before. It was realized in 0.35 μ m SiGe BiCMOS technology with 4mm² total die size. The power consumption is only 162mW under a 2.8V supply. This mobile digital TV tuner covers the CMMB frequencies from 2.635GHz to 2.660GHz., it achieves noise figure of 2dB, input sensitivity of -100dBm, IIP3 of 17dBm. This ensures the tuner RFIC has high sensitivity, wide dynamic range, fast switching and ambient-proof performance with low power consumption and low cost.

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