

A 2.6-GHz Zero-IF Mobile-TV Front-end RFIC for CMMB Applications

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Abstract — A RF 2.6-GHz direct-conversion receiver front-end for CMMB (China Mobile Multimedia Broadcasting) tuner system is implemented in SiGe BiCMOS technology. It consists of a low noise amplifier (LNA) with high-gain/low-gain (HG/LG) modes, a continuously tuned radio frequency variable gain amplifier (RFVGA) and a down-conversion mixer. The receiver delivers a power gain of 36dB, an input-referred-3rd-order-intercept-point (IIP3) of 18dBm at low gain mode and an overall noise figure of 2 dB with an input return loss (S11) of -18dB at high gain mode. The total front-end consumes 16mA from a 2.8-V supply.

Index Terms — BiCMOS technology, CMMB, tuner, front-end, LNA, RFVGA, continuously gain-controlled, mixer, down-conversion.

I. INTRODUCTION

“Mobile TV” is recently emerging across the world. In Chinese markets, the next generation digital broadcasting service, China Mobile Multimedia Broadcasting (CMMB) system, has been developed for automotive and handheld terminals. Because CMMB service is mobile and personalized, the market demand is expected to be higher and broader than existing household-based broadcasting services. CMMB system is a mixed satellite and terrestrial wireless broadcasting system designed to provide audio, video and data service for handheld receivers with less than 7 inch wide LCD display, such as PMP, mobile phone, PDA and UMPC. The satellite and terrestrial complementary network is combined to create a Single Frequency Network (SFN) using the 2635-2660 MHz band. The CMMB system is based on the Satellite Terrestrial interactive Multiservice Infrastructure (StiMi) channel transmission technology. The service operates in the 2.6-GHz frequency band with 25MHz bandwidth in order to offer 25 video and 30 radio channels.

Main challenges of a CMMB tuner design are good sensitivity and wide dynamic range, which requires very low noise and high linearity; small form factor and low cost, which requires high degree of integration; and low power consumption. In this paper, a fully integrated CMMB receiver front-end is presented. The proposed solution has an NF of less than 2dB, an IIP3 of more than 18dBm in the low gain mode and a power

consumption of 45mW. A simplified block diagram of a typical CMMB tuner receiver is shown in Fig. 1. This work reports the design and implementation of a 2.6-GHz BiCMOS SiGe mobile tuner front-end RFIC design. Next, we will present the circuit design and implementation of the tuner front-end RFIC in details. The experimental results are given in Section III.

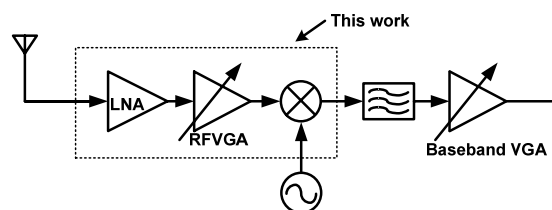


Fig. 1 Block diagram of the proposed CMMB tuner front-end RFIC.

II. CIRCUITS DESIGN

As illustrated in Fig.1, the tuner receiver front-end consists of a single-ended low-noise amplifier (LNA) with two gain modes (HG/LG), a continuously tuned RFVGA, and a degenerated double-balanced Gilbert cell mixer for down conversion.

A. Low-Noise Amplifier

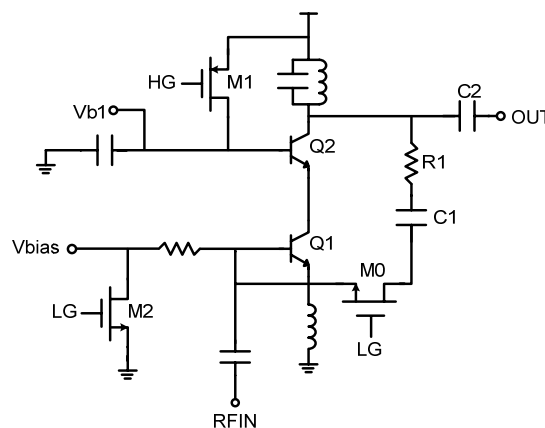


Fig. 2 LNA architecture

In the RF receiver front-end, the noise of the LNA is the biggest contributor to the overall noise of the tuner system. In our design, we used the inductor-degenerated cascode single-stage LNA achieve the required noise performance. As shown in Fig. 2, the LNA has two gain modes: high gain mode (HG) and low gain mode (LG). For the high gain mode, an inductively degenerated cascode structure is used to achieve 15dB power gain and 1.6dB NF while drawing only 4mA. For the low gain mode, the MOS switch M0 is turned on, and the attenuation resistor R1 are used for -7dB power loss. The capacitor C1 is used for ac coupling. The IIP3 in the low gain mode can achieve more than +20dBm. In the high gain mode, the output capacitor C2 is designed to conjugate-match the output impedance of the LNA with that of the following RFVGA for best power transmission. In the low gain mode, the value of the C2 may not be on the power matched value, but it is not important since the gain is attenuated in this mode.

In Fig. 2, the MOSFET switch M0, M1 and M2 are used to switch the gain of the LNA. In the high gain mode, all the switches are turned off, while in the low gain mode, all the switches will be turned on. In our design, we added the switch M1 for keeping the cascode transistor Q2 working in the safe area in the low gain mode. When the input signal is large and the circuit is in the low gain mode, the transistor Q1 is shut down by switch M2, the collector voltage of Q1 will be low without the switch M1. As a result, almost the entire supply voltage adding the large input signal swing will be added to the collector-emitter junction of the transistor Q2, potentially causing break down. However, with M1 turned on in the low gain mode, the base and emitter voltage of Q2 will be pulled to high and the collector-emitter junction voltage will be greatly reduced, which helped to keep Q2 working in the safe region in the low gain mode.

B. RF Variable Gain Amplifier

The variable gain amplifier followed after the LNA, is used to get enough power gain for the front-end and achieve wide tunable gain range of the front-end. Since the CMMB receiver must be able to handle signals with a wide input dynamic range from -100dBm to 0dBm, wide gain tuning at the front-end is thus necessary to meet the noise and linearity requirements in the entire input range. As shown in Fig. 3, the core of the RFVGA circuit consists of a three-stage capacitive attenuator with 14dB per stage attenuation and four amplifiers which smoothly switch outputs from the ladder attenuator. Fig. 4 shows the simulated IIP3 and gain of the RFVGA as control voltage changes. The

VGA architecture has its origin in the VGA using a resistive attenuator proposed by [1]. The modification with capacitive attenuator is reported in [2]-[4].

In the common load of the four core amplifiers, L and C1, C2 used as a LC tank to filter out the signal out of the band. Using the differential inductor L reduces the chip area. In the 2.8V RF circuit design, the LC tank load also greatly released the critical headroom requirement, thus improved the gain and the linearity performance of the circuit. Of course, power match between stages will be more critical and challengeable.

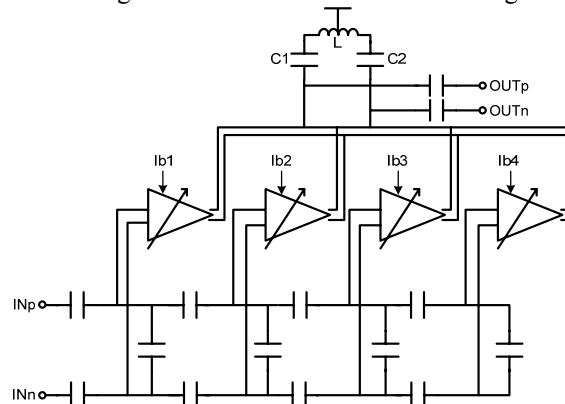


Fig. 3 RFVGA schematic diagram.

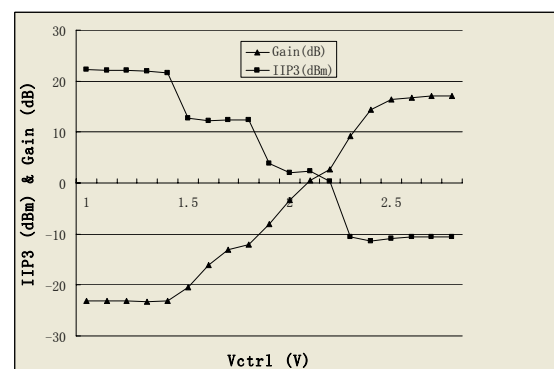


Fig. 4 Simulated gain and IIP3 dependence on control voltage of RFVGA.

As shown in Fig.3, by controlling the bias current Ib1~Ib4 of the four amplifiers, the gain of VGA can be controlled. The bias current control shown in Fig. 5 is proposed in [2]. As can be shown in Fig. 6, the current of each branch of Ib1~Ib4 will be distributed with an appropriate ratio corresponding to the input control voltage Vctrl while the total current of the four branches remains the same.

In Fig. 7, the core amplifier of the RFVGA is presented. In our design, the bias current Ib is mirrored from the bias transistor Q0 to the amplifying transistors Q1 and Q2, and it is also mirrored to Q5 that provides

the bias voltage to cascode transistors Q3 and Q4. As I_b grows from min to max, not only Q1 and Q2 will change from off state to on state, Q3 and Q4 will also change. For the four amplifiers have common loads, the collector of Q3 and Q4 will always be on the working state. For the core amplifier which is not turned on, if the base voltage of Q3 and Q4 is pulled up to supply voltage, then the collector-emitter voltage of Q3 and Q4 will be the lowest, and there will not be a breakdown even very large input signal is added on the collector of Q3 and Q4.

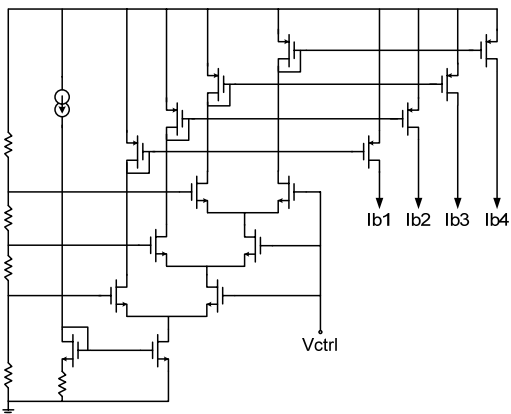


Fig. 5 Programmable bias current of RFVGA.

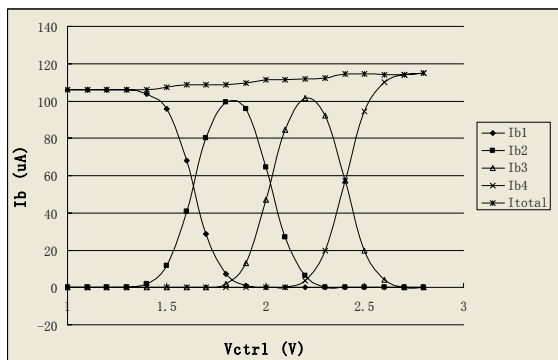


Fig. 6 Bias current versus control voltage

A quadrature mixer shown in Fig. 8 has been developed to provide improved image rejection ratio (IRR) and reduced phase error [5]-[7]. It is basically a combination of two Gilbert mixers with shared transconductance stages. The total signals turn on in the order: LOQp, LOIp, LOQn, LOIn. For example, when the RF signal on transistor Q1 is high and the LOQp signal on Q7 is high, the voltage of the collector terminal of Q1 is pulled high and the transistors Q3, Q4 and Q8 are shut off. In this way, the total available

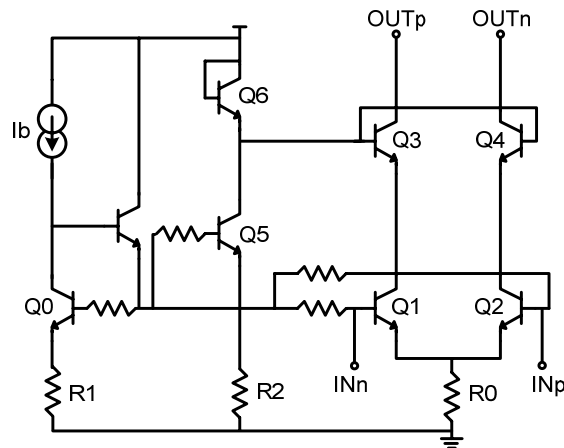


Fig. 7 Simplified schematics of RFVGA.

C. I/Q Down-Conversion Mixer

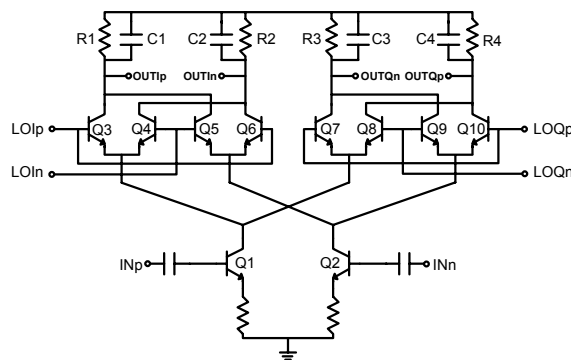


Fig. 8 Quadrature down-conversion mixer.

current must flow through only a selected transistor according to the local signal sequence. This mechanism is called Q-I mutual interference and is useful for phase error suppression. In Fig. 8, the capacitors C1 to C4 are used to filter out the RF and LO frequency and their harmonics.

III. EXPERIMENTAL RESULTS

The die photo of the CMMB tuner front-end implemented in a 0.35um SiGe BiCMOS technology is shown in Fig. 9. The presented tuner RFIC has been tested and the front-end performs meet the CMMB system requirements. The measured overall performance of the front-end is summarized in TABLE I. The measured overall tuner NF is 2dB. Its IIP3 is 18dBm in lowest gain. In Fig. 10, the measured front-end gain versus control voltage is shown.

For narrow-band and high frequency tuner design, the package effect is important for the performance of

the front-end. In the design of the LNA, degeneration parasitic impedance contributes large noise to the LNA, and the added impedance also deteriorates the input return loss that further degrades the power gain of the LNA, thus it is critical to decrease the influence of the added parasitic degeneration impedance. Among all the added degeneration impedance, the dominant one is the package bondwire impedance. For a QFN package and a 48-pad 7mm² chip, the bondwire inductance will be as large as more than two nanohenries (nH). Such big inductor will greatly degrade the performance of the single-ended LNA. Hence, in our package, we use downbond wire connected to the ground of the LNA, which greatly decrease the added degeneration inductance from 2nH to 600pH. Moreover, we packaged three downbond wires to the LNA ground pad to further reduce the inductance from 600pH to 200pH. It should be pointed out that adding too more downbonds will increase parasitic capacitance to the degeneration of the LNA. In the layout, the wire from the degeneration inductor to the ground pad should as short and as thick as possible to reduce its loss.

TABLE I
SUMMARY OF MEASURED TUNER FRONT-END
PERFORMANCE

Parameter	Value
Noise figure@Max gain	2dB
Total gain of front-end	36dB
IIP3@min gain	18dBm
LNA gain tuning step	20dB
RFVGA control range	41dB
Supply voltage	2.8V
Current consumption	16mA

IV. CONCLUSION

A zero-IF CMMB tuner front-end RFIC has been implemented in a 0.35um BiCMOS SiGe technology. The measurement results show that the front-end tuner RFIC is compliant with the newly released Chinese CMMB mobile TV requirements with a state of the art gain control range of 61dB and overall NF of 2dB. Low power consumption of 45mW is achieved, which is suitable for the CMMB receiver integrated in a mobile environment.

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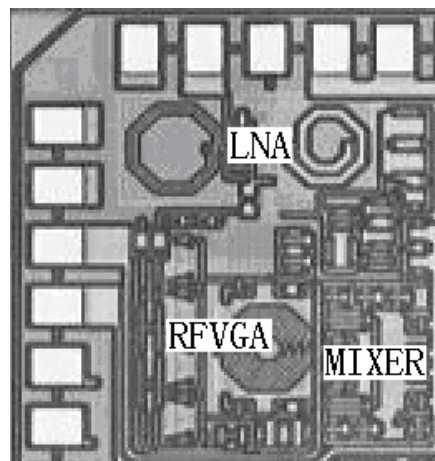


Fig. 9 Chip micrograph.

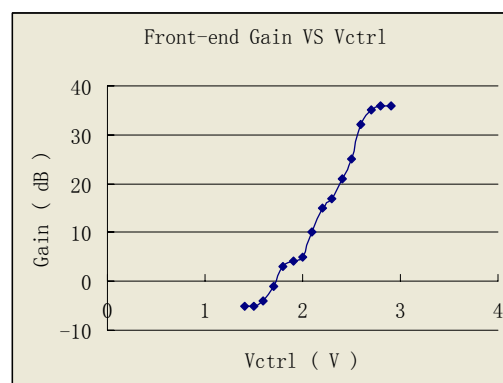


Fig. 10 Measured front-end gain versus control voltage.

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