

MIMO RFIC Transceiver Designs for WLAN Applications

Fa Foster Dai¹, *Senior Member, IEEE*, Yin Shi², Jun Yan², Xueqing Hu²

1. Dept of Electrical and Computer Eng., Auburn University, Auburn, AL 36849-5201, USA.
2. Suzhou-CAS Semiconductors Integrated Technology Research Center, 328 Airport Road, Suzhou Industrial Park, Suzhou 215021, China.

Abstract — This paper presents a low-power single chip WLAN 802.11a transceiver RFIC for personal communication terminal applications. The 5.2GHz transceiver RFIC is implemented in a 0.5 μ m SiGe technology with 16 mm² die size. It consumes 110/130mA in receive/transmit mode under a 3.3V supply. The receiver path shows a 6.4dB noise figure and a -20dBm IIP3 under a maximal 67dB gain. The transmitter path OIP3 is measured as 29.7dBm. The LC-tuned VCO has a tuning range from 4.08GHz to 4.7GHz and the measured phase noise is -112dBc/Hz @ 1MHz offset. Also discussed are design considerations for multiple-input-multiple-output (MIMO) transceiver RFIC implementations.

Index Terms — WLAN, 802.11a, SiGe, MIMO, RFIC, low power, low noise, linearity, EVM.

I. INTRODUCTION

TRADITIONAL wireless communication systems employ a single transmitter antenna and a single receiver antenna (SISO). But SISO system cannot meet the ever-increasing requirement of higher data rate and reliability in future wireless communication systems. In recent years the digital communication systems using multiple-input-multiple-output (MIMO) have been developed to achieve better performance without additional costs of bandwidth and transmitted power. This technology is being rapidly adopted by modern commercial communication standard such as wireless local area network (WLAN) standard IEEE802.11n and beyond third generation (B3G) mobile communication system. The underlying thought of MIMO is to exploit the rich spatial dimension and turn the multiple-path wireless link into two types of benefits: diversity gain and throughput increase. These two benefits actually can be traded off and make MIMO flexible enough to fit into different communication standard. At the same time of the MIMO theory development, the MIMO RFIC design has been attracting more attention. The effort to design practical IC has been made in [1] where a 2 \times 2 radio IC for WLAN system is implemented.

Wireless communications has attracted great attentions

recently, fueled by the emerging of wireless local area networks (WLAN) and the third generation W-CDMA technology [1-6]. The ever-increasing demand for wireless multimedia applications such as video streaming keeps pushing future WLAN systems to support higher data rates (54 MBit/s up to 1 GBit/s) at high link reliability and over greater distances.

With WLAN standards operating in very different frequency bands, market leading WLAN solutions have to offer multi-mode interoperability with transparent worldwide usage. Moreover, the frequency allocation of the WLAN standards in the "unlicensed" 5-GHz band is constantly evolving. In particular, Japan proposed four additional RF channels in the 4.9 to 5.0-GHz band and further three channels in the 5.03 to 5.09-GHz band for this standard. This change could significantly increase the available channels for 5-GHz WLAN in Japan, and create yet another difficulty for WLAN chipmakers by requiring them to enable access to this lower-frequency band. It is thus desirable to design a WLAN transceiver with a future-proofed multi-band frequency synthesis scheme against evolutions and changes in allocated spectrum worldwide.

This paper represents a low-power and low-cost WLAN 802.11a transceiver RFIC for personal communication terminal applications. The 5.2GHz transceiver RFIC is implemented in a 0.5 μ m SiGe technology with 16 mm² die size. It consumes 110mA in receive mode and 130mA in transmit mode under a 3.3V supply. The receiver path provides a maximal 67dB and a minimal 20dB gain. The receiver path noise figure is measured as 6.4dB in maximal gain mode and its IIP3 is measured as -20dBm. The transmitter path OIP3 is measured as 29.7dBm. The LC-tuned VCO has a tuning range from 4.08GHz to 4.7GHz and the measured phase noise is -112dBc/Hz @ 1MHz offset.

II. MIMO TRANSCIVER DESIGN CONSIDERATIONS

A simple 2 \times 2 MIMO communication system is illustrated in Fig. 1. MIMO technology allows greater transmission range at the same transmitted power level

and for the same data rate. Alternatively with MIMO technology, the system signal-to-noise-ratio (SNR) requirement can be relaxed for a given data rate. Reference [1] presents the first published RFIC transceiver designed for MIMO WLAN applications. With the exception of the synthesizer loop filter, and the LNA, and PA matching networks, the entire 2x2 MIMO radio system was integrated in one chip with 29.1mm² die size.

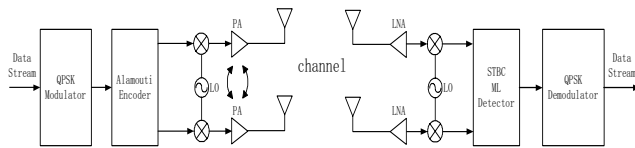


Fig. 1. A 2x2 MIMO communication system.

As a trade-off between level of integration and complexity/yield, Ref [1] integrated two multi-band dual radio paths on the same die. A 2x2 MIMO link can therefore be formed using only two MIMO transceiver ICs, compared to four SISO chips. The presented MIMO WLAN transceiver IC supports the 802.11b/g and 802.11a low and middle bands. In this system only two radios were integrated because more would have led to more expensive packaging, lower yield, and for many applications a 2x2 MIMO system with two radios is sufficient. However, if more than two radios are desired in a particular application, then even two, three, or more dual-radio transceiver chips can be used in a single link, provided that their local oscillations (LO) are all phase synchronized. For instance, two pairs of dual-radio transceiver chips can be used to form a 4x4 MIMO radio system. Each transceiver pair consists of a master and a slave dual-radio transceiver chip. The slave chip synchronizes its LO to the master chip by means of the LO porting circuitry, in which the master chip's $\Sigma\Delta$ fractional-N synthesizer can be used to drive the slave chip's LOs for synchronization.

MIMO transceiver RFIC design is a challenge. When multiple radios are integrated in the same die, interference among the transceiver building blocks will be a big concern. In particular, when multi-band power amplifiers are in operation, their radiation may inject-lock the VCOs and generate cross-talk noise through substrate, package, power supply, or ground. Careful floor planning and proper isolation of the MIMO transceiver layout are critical. The on-chip synthesizer has been carefully designed so that all the VCOs are operating at different frequencies from the PA transmit bands. In a MIMO system, all the LOs in different radio paths need to be

synchronized. MIMO calibration requires a loop back measurement through transmit and receive paths. A loop back measurement is performed by connecting the transmitter to one antenna and the receiver to the other antenna on the same chip and then matching the gain and phase of both paths. If more than one PLL is used to generate the LO tones, static phase error and time variant phase variations among the PLLs will occur. To avoid many of these LO phase drift issues resulting from the use of multiple PLLs, all the RF and IF LOs can be generated using a single frequency synthesizer.

III. WLAN TRANSCEIVER ARCHITECTURE

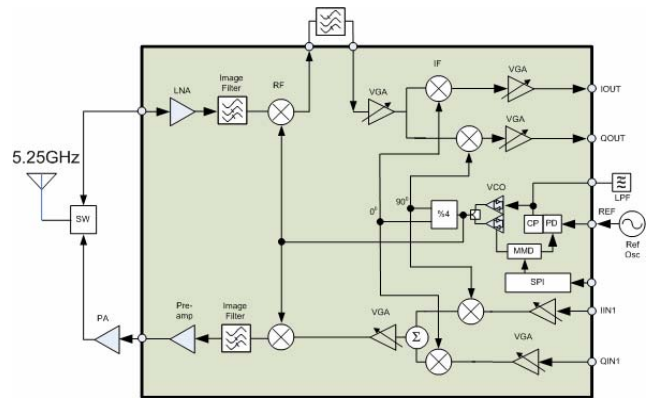


Fig. 2 WLAN 802.11a transceiver RFIC block diagram.

Since the WLAN market is very cost-sensitive, for a competitive radio, it must be low cost and low power. Choosing the transceiver architecture wisely is thus critical. Superheterodyne radios require two synthesizers, but have a high level of transceiver performance. Their inherent frequency diversity reduces DC offset and VCO pulling effects as compared to direct conversion receivers. Although by comparison direct conversion receivers require only one local oscillator, often times mixing schemes are used to achieve similar frequency diversity, resulting in a more complicated transceiver. A compromise between the two approaches is to use a walking IF architecture where the RF LO is 4 times the IF LO [7]. Thus both LOs can be derived from a single synthesizer obtaining the benefit of a direct down conversion radio, but retaining the performance advantages of the superheterodyne radio.

This paper implemented a transceiver RFIC as illustrated in Fig.2. The walking IF architecture is chosen because a single integer-N frequency synthesizer with a 16MHz reference would be enough to supply both RF and IF LO frequencies. In addition, only one VCO with wide-tuning range is needed to cover the 802.11a low and middle bands from 5.18GHz to 5.32GHz. The receiver

includes a low noise amplifier (LNA) followed by an image filter to reject the RF image tone at about 3.2GHz. The RF mixer down-converts the received signal to IF frequency at about 1.05GHz. The IF mixers further demodulate the IF signal to baseband quadrature signals. The baseband block includes the VGAs for gain tuning and the baseband filter is off-chip. The transmitter starts with the baseband VGA blocks, followed by IF up-converters. The IF signal is further up-converted to 5.2 GHz signal by an RF mixer followed by an image filter. A pre-driver amplifies the 5.2GHz signal with -5dBm output power for driving the off-chip power amplifier.

III. RF FRONT-END DESIGN

Receiver front-end includes a differential LNA, an image-rejection filter and a down-converter mixer. The differential LNA has good noise performance and less dependence on the package parameters. Image-rejection filter is constructed with an inductor and two capacitors to remove the 3.2GHz image tones. RF mixer is also a differential structure to interface with differential LNA. Down-mixer output goes off-chip to a SAW filter, which has 1.05GHz center frequency and 30MHz bandwidth with 30dB out-of-band attenuations.

The circuit schematic of the mixer is shown in Fig. 3, which is a typical Gilbert cell with differential inputs and outputs. Inductor L_E is used as emitter degeneration to increase the linearity of the mixer while consuming little voltage headroom. Since mixer's IIP3 is proportional to $\omega G_m L_E$, L_E should be carefully chosen to compromise between the gain and the IIP3. Noise matching is achieved by selecting the sizes of L_E and the transistors and operating the RF transistors at the current density required for minimum noise figure. Combining with the matching network, L_E also achieves simultaneous noise and power matching. Minimizing the noise of the mixer relies upon fast switching of the top quad-transistors. Note that the current in the quad switching transistors is identical to that flowing through the RF transistors below, where the bias current is tuned to the minimal noise figure current. Therefore, the top quad-transistors are sized such that their current density is close to that corresponding to the peak f_T . In this design, the ratio of the quad-transistor size to the RF transistor size is 1/6. The LO signals are applied to the base of the quad transistors through LO buffers, so that their amplitude can be kept large enough for completely switching. L_f and C_f are tuned to the LO+RF frequency to get rid of the unwanted sideband. The LC tank formed by L_T and C_T are tuned to the second RF harmonic, acts as a filtered current source in the emitter of the input transistors.

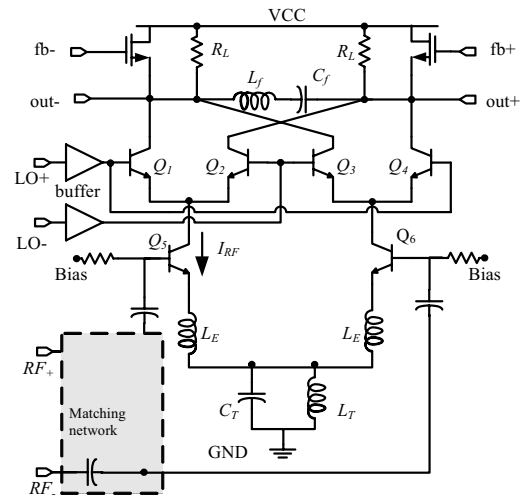


Fig. 3 schematic of the up-mixer.

IV. FREQUENCY SYNTHESIZER DESIGN

In a walking-IF transceiver, the channel frequency is defined as $F_{ch} = RF + IF = 5180 + 20k$, where $k=0,1,\dots,7$ represents the 8 channels in WLAN 802.11a low and middle bands. The RF mixer has a local oscillation frequency (LO) at 4 times of the IF frequency, namely, $RF = 4IF = 4144 + 16k$. Thus, the VCO frequency is required to cover 4144MHz to 4256MHz for 802.11a low and middle bands. The IF frequency is given by $IF = RF/4 = 1036 + 4k$. Therefore, the walking IF is from 1036MHz to 1064MHz.

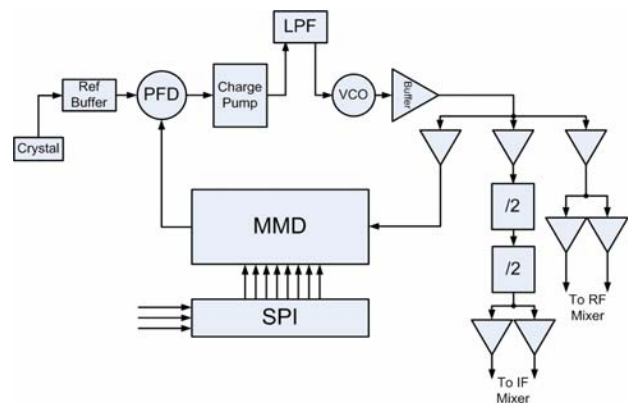


Fig. 4 PLL for RF and walking IF generations.

The integer-N phase lock loop (PLL) frequency synthesizer is shown in Fig. 4. It consists of an LC-tuned VCO which has a wide linear tuning range from 3.9GHz to 4.258GHz. Thus, the VCO can cover the entire 5.15~5.35GHz 802.11a bands. Schematics of the VCO is

shown in Fig. 5, where P-MOSFETs are used for the oscillation transistors such that the tank can be referenced to the ground for low phase noise. The VCO design also employs an automatic-amplitude-control (AAC) circuitry that can keep the VCO in current-limit region and alleviate the AM and AM to PM noise. AAC also provides perfect ambient-proof characteristics over process, temperature and frequency variations.

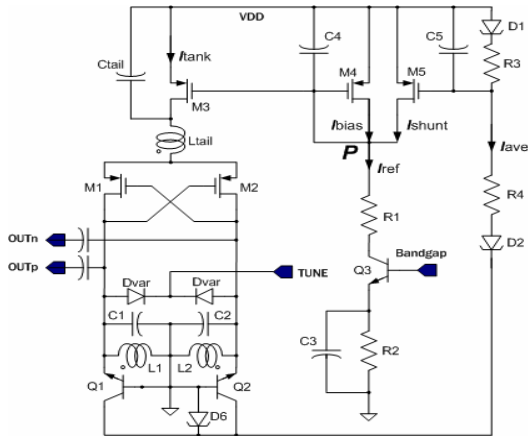


Fig. 5 Schematic of the wide tuning VCO with AAC.

V. CHIP MEASURED RESULTS

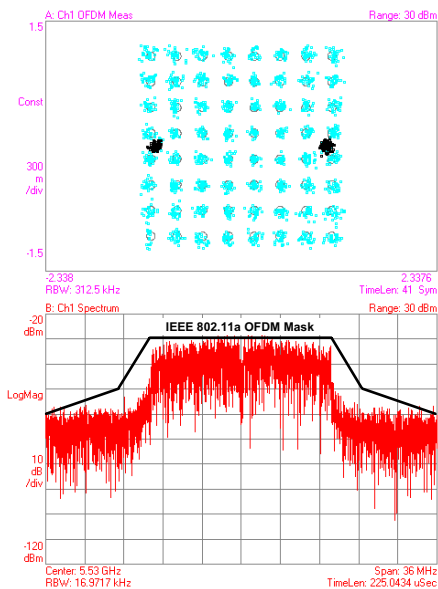


Fig. 6 Measured EVM for IEEE 802.11a transmission, EVM=6.3%, meeting IEEE 802.11a OFDM requirement.

The 5.2GHz transceiver RFIC is implemented in a $0.5\mu\text{m}$ SiGe technology. The transceiver RFIC occupies 16mm^2 areas and is packaged using a 48-pin leadless

package. Fig. 6 gives the measured error-vector-magnitude (EVM) for typical IEEE 802.11a transmission with 64 QAM OFDM modulation. The measured EVM indicates that the presented transceiver meets the IEEE 802.11a OFDM requirement. Table I summarizes the WLAN transceiver performances. The receiver consumes 110mA current and the transmitter consumes 130mA current, respectively.

TABLE I
SUMMARY OF TRANSCEIVER PERFORMANCE

Spec	RX High Gain	RX Low Gain	TX High Gain	TX Low Gain
Gain	67.1dB	20dB	14.8dB	5.5dB
NF	6.4dB	16.7dB	38.4dB	38.5dB
IIP3	-25.4dBm	5.3dBm	-5dB	3.2dB
Current	110mA		130mA	

VI. CONCLUSIONS

This paper represents a low-power and low-cost SiGe RFIC WLAN 802.11a transceiver RFIC design for personal communication terminal applications. The transceiver meets the IEEE 802.11a OFDM requirement. The receiver consumes 110mA current and the transmitter consumes 130mA current under a 3.3V supply.

REFERENCES

- [1] Dave G. Rahn, Mark S. Cavin, Foster F. Dai, Neric Fong, Richard Griffith, Jose Macedo, David Moore, John W. M. Rogers, and Mike Toner, "A Fully Integrated Multi-Band MIMO WLAN Transceiver RFIC," *IEEE Journal on Solid State Circuits*, Vol. 40, No. 8, pp. 1629-1641, August, 2005.
- [2] M. Zargari, et al. "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g WLAN", *IEEE International Solid-State Circuits Conference (ISSCC)*, p.96, Feb. 2004.
- [3] T. Maeda, et al. "A direct-conversion CMOS transceiver for 4.9-5.95GHz multi-standard WLANs", *IEEE International Solid-State Circuits Conference (ISSCC)*, p.90, Feb. 2004.
- [4] J. Bouras, et al. "A digitally calibrated 5.15-5.825GHz transceiver for 802.11a wireless LANs in $0.18\mu\text{m}$ CMOS" *IEEE International Solid-State Circuits Conference (ISSCC)*, p.352, Feb. 2003.
- [5] P. Zhang, et al. "A direct conversion CMOS transceiver for IEEE 802.11a WLANs"; *IEEE International Solid-State Circuits Conference (ISSCC)*, p.354, Feb. 2003.
- [6] A. Behzad, et al. "Direct-conversion CMOS transceiver with automatic frequency control for 802.11a wireless LANs"; *IEEE International Solid-State Circuits Conference (ISSCC)*, p.356, Feb. 2003.
- [7] J. W.M. Rogers, Foster F. Dai, Mark S. Cavin, and Dave G. Rahn, "A Multi-Band $\Delta\Sigma$ Fractional-N Frequency Synthesizer for a MIMO WLAN Transceiver RFIC," *Journal of Solid State Circuits*, vol. 40, No. 3, pp. 678-689, March 2005.