

# A 10-bit 2GHz Current-Steering CMOS D/A Converter

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**Abstract** — This paper presents a 2GS/s 10-bit CMOS digital-to-analog converter (DAC). This DAC consists of a unit current-cell matrix for 6MSBs and another unit current-cell matrix for 4LSBs, trading off between the precision and size of the chip. The Current Mode Logic (CML) is used to ensure high speed, and a double Centro-symmetric current matrix is designed by the  $Q^2$  random walk strategy in order to ensure the linearity of the DAC. The DAC occupies  $2.2 \times 2.2$  mm<sup>2</sup> of die area, and consumes 790mw at a single 3.3V power supply.

## I. INTRODUCTION

Digital-to-analog converters (DACs) are essential components of a large number of modern communication systems, such as wired and wireless transmitters, direct digital synthesis, arbitrary waveform generations, and local oscillators. In these applications, DACs, typically with 10-bit or higher linearity and sampling rates up to 1GSamples/s, are required. To meet these specifications, current-steering DACs and the technique of MOS Current-Mode Logic (CML) can be used, since they have an advantage of combining high conversion rate and high resolution.

Current-steering DACs are based on an array of matched current source which are unity decoded or binary weighted. Architecture variants are often used, such as the two-stage, the interpolated, and the segmented architectures. The difficulty to meet a certain intrinsic accuracy specification due to the random mismatches between the current sources, however, is the same for all architectures. For signal processing applications, the segmented architecture, that combines unity and binary weighted current cells, is the most often used for the following reason: it allows a tradeoff of reduction in the glitch energy and differential nonlinearity (DNL), with an increase in the decoding logic complexity and the overall layout area.

The design proposed in this work is a high-speed (up to 2GSamples/s) 10-bit intrinsic accuracy (no trimming, no calibration, or dynamic averaging) current-steering segmented architecture DAC implemented in a standard twin-well 4-metal layer 0.35  $\mu$  m CMOS technology. The main features of the DAC are discussed in the next sections. In Section II, an overview of the DAC architecture is presented. In Section III, the implementation of CMOS current mode logic is discussed. In Section IV, the main technique of the DAC layout is described, including  $Q^2$  random walk strategy. In Section V, the simulation performances of the DAC are presented.

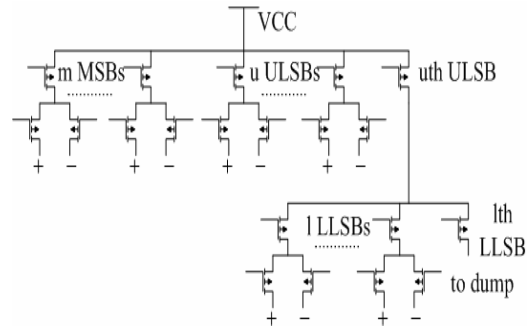


Figure 1. Conventional DAC architecture

## II. DAC ARCHITECTURE

For high-speed and high-resolution applications, the current source switching architecture is preferred since it can drive a resistive load directly without the need for a voltage buffer. A conventional high-performance DAC architecture used in such applications is shown in Figure 1, the n-bit DAC consists of  $m$  thermometer (linearly) decoded most significant bits (MSBs),  $u$  thermometer decoded upper least significant bits (ULSBs), and  $l$  binary decoded lower least significant bits (LLSBs). The current sources are taken directly to a pair of resistive loads. Modern high-speed and high-resolution DACs all use variations of this basic architecture [1]-[3]. Assuming  $I_{unit}$  is the unit current source, the output current is given by

$$I_{out} = (2^{l+u} I_{unit}) \sum_{k=l+u+1}^{l+u+m} a_k \cdot 2^{k-l-u-1} + (2^l I_{unit}) \sum_{k=l+1}^{l+u} a_k \cdot 2^{k-l-1} + I_{unit} \sum_{k=1}^l a_k \cdot 2^{k-1} \quad (1)$$

Where  $n=l+u+m$ ,  $a_k$  ( $k=1, 1 \dots l+u+m-1$ ) is the digital signal input into the DAC

In our design, the binary segment is omitted, then the 10-bit DAC is implemented as a segmented thermometer current DAC, which consists of two thermometer decoded parts: the  $m$  thermometer decoded most significant bits (MSBs) and the  $l$  thermometer decoded least significant bits (LSBs). Assuming  $I_0$  is the unit current, the output current is given by

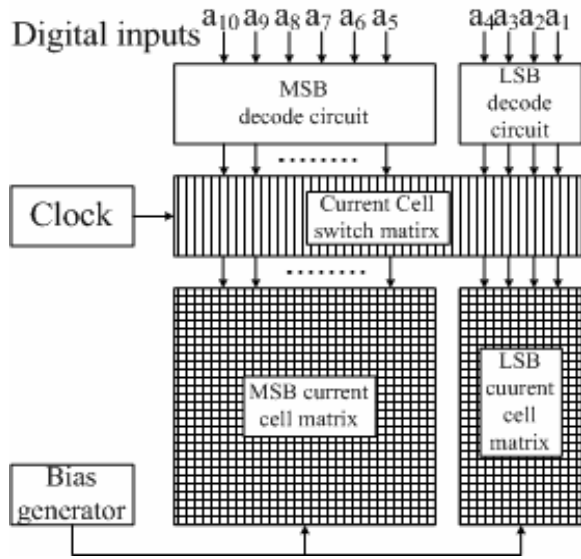


Figure 2. Simplified DAC architecture

$$I_{out} = (2^l I_0) \sum_{k=l+1}^{m+l} a_k \cdot 2^{k-l-1} + I_0 \sum_{k=1}^l a_k \cdot 2^{k-1} \quad (2)$$

The unit current of LSBs is  $I_0$ , while the unit current of MSBs is  $2^l I_0$ . Thermometer decoding has the well-known advantages of monotonicity and reductions of glitch at major carries, but full thermometer decoded architectures are impractical to implement for high resolution, mainly because of the large core area. So we choose the segmented thermometer decoding architecture in order to reduce the decoding cells. The DAC we design consists of 6 MSBs and 4 LSBs. The input bits are respectively taken to the MSB and LSB thermometer decoding cells, which control the  $36 \times 16$  current switch array. The current sources are taken directly to a pair of  $50 \Omega$  resistors through the current switch array. Figure 2 gives a schematic representation of the realized chip.

### III. CIRCUIT IMPLEMENTATION

The decoder has historically been the critical path which

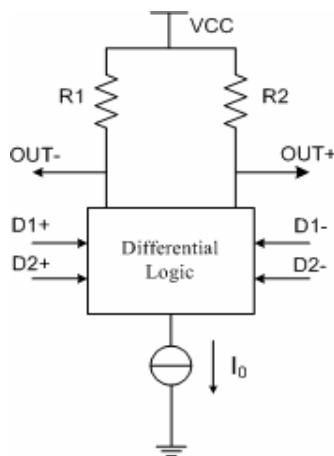


Figure 3. CMOS current mode logic circuit

limits the conversion speed of DACs. Like emitter-coupled logic (ECL) commonly used in high-speed bipolar circuits, Current Mode Logic (CML) [4] which is a technique adapted from ECL is a good choice when high-speed circuits are implemented. Figure 3 shows the common representation of CMOS CML circuit, all of the currents in constant current source  $I_0$  flow through one of the two branches, depending on the value of the differential pull down network (PDN), providing complementary output signals. The delay of the CMOS CML circuit can be approximated as (3)

$$\tau = \frac{\Delta V}{I_0} C_L = R_L \cdot C_L \quad (3)$$

Where  $\Delta V$  is the output voltage swing,  $I_0$  denotes the current that flows through the current source,  $C_L$  is the load capacitance, and  $R_L$  is equivalent load resistance.

We take a CML buffer for an example. Figure 4 gives the schematic of a CML buffer. The simple square law voltage-current relationship for a CMOS transistor is (4)

$$i_D = \frac{\mu C_{OX}}{2} \left(\frac{W}{L}\right) (v_{GS} - V_T)^2 \quad (4)$$

Which can be rewritten as (5)

$$v_{GS} = \sqrt{\frac{2}{\mu C_{OX}} \left(\frac{L}{W}\right)} \sqrt{i_D} + V_T \quad (5)$$

Therefore, the input voltages  $v_1$  can be written as (6)

$$\begin{aligned} v_1 &= v_{GS1} - v_{GS2} \\ &= \sqrt{\frac{2}{\mu C_{OX}} \left(\frac{L}{W}\right)} (\sqrt{i_{D1}} - \sqrt{i_{D2}}) \\ &= \sqrt{\frac{2}{\mu C_{OX}} \left(\frac{L}{W}\right)} (\sqrt{i_{D1}} - \sqrt{I_{EE} - i_{D1}}) \end{aligned} \quad (6)$$

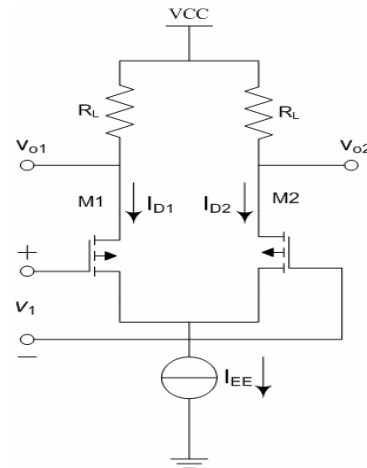


Figure 4. CML buffer

From the equation above,  $i_{D1}$  can be solved as (7)

$$i_{D1} = \frac{I_{EE}}{2} \left[ 1 \pm \sqrt{v_1^2 \frac{\mu C_{OX}}{I_{EE}} \left(\frac{W}{L}\right) - \frac{(\mu C_{OX})^2}{4I_{EE}^2} \left(\frac{W}{L}\right)^2 v_1^4} \right] \quad (7)$$

The term inside the brackets will have a peak value of two at some input voltage of  $v_{1max}$ . This voltage can be determined by setting the derivative of (6) to zero, and the result is given by (8)

$$v_{1max} = \sqrt{\frac{2I_{EE}}{\mu C_{OX} \left(\frac{W}{L}\right)}} \quad (8)$$

The current becomes (9)

$$i_{D1} = \frac{I_{EE}}{2} (1 \pm \sqrt{2-1}) = \frac{I_{EE}}{2} (1 \pm 1) = 0, I_{EE} \quad (9)$$

Clearly, (9) is no longer valid for values greater than  $v_{1max}$ , as the equation then incorrectly predicts that the current starts to decrease again. For larger values of voltage, one side continues to take all the current, and the other side just becomes more firmly off. In real circuits, for large  $v_1$ , the source voltage then starts to follow input voltage, limiting the total voltage to  $v_{1max}$ .

From (8), it can be seen that for larger current, the required switching voltage increases, while for larger  $W/L$  ratios, the switching voltage decreases. On one hand, large swing of switching voltage is robust for circuits and logic operation; on the other hand, considering the speed, large swing of the switching voltage is not appropriate according to (3). So tradeoff between speed and robust should be made carefully. Normally, the swing of the switching voltage for CMOS circuits is about 0.4V, we choose 0.6V in our design and 150  $\mu A$  as the tail current. Figure 5 shows the actual CML circuits used in the implemented DAC. Here, we use PMOS transistors as resistive loads instead of resistors for the reason that it has advantages of simplicity in layout and high integration density. More schematics of the Current Mode

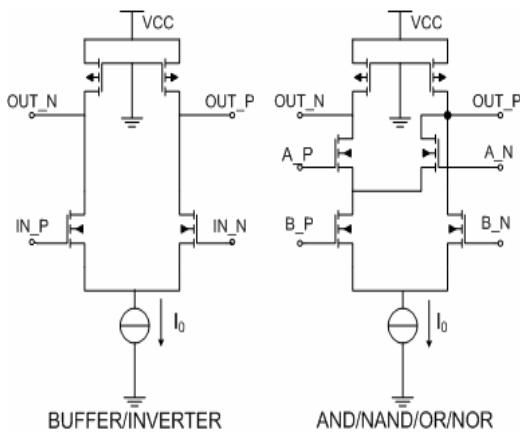


Figure 5. CML circuits

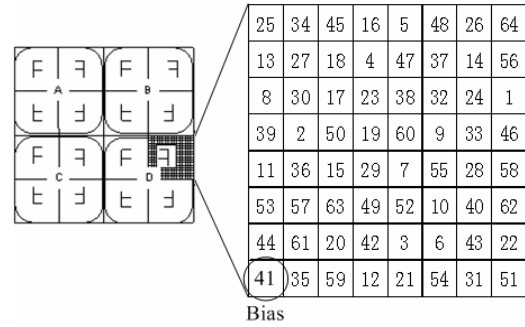


Figure 6. Sequence of the Q2 random walk scheme

Logic can be referred to [4], [5].

#### IV. LAYOUT IMPLEMENTATION

Two important parameters of DACs' static performance are integral nonlinearity (INL) and differential nonlinearity (DNL), which are related to the strategy of the layout implementation [7]. Inappropriate layout implementation can be great harmful to INL and DNL, because in the unit decoded matrix, it is difficult to make current sources identical due to layout mismatches, output impedance of the current source and switch, edge effects, voltage drops in the supply lines, thermal gradients, doping gradient, and oxide thickness. The nonlinear secondary effects which cause graded, symmetrical, and random errors also reduced linearity of DACs.

The DAC proposed in this paper employs a novel layout strategy to minimize the degradation of linearity caused by mismatches of current sources. This layout strategy will be referred to as quad quadrant ( $Q^2$ ), because four (quad) units in every quadrant compose one current source [6]. The unit sequence of the unit current cells in the matrix for the DAC is illustrated in Figure 6.

The 1024 current sources are divided into 16

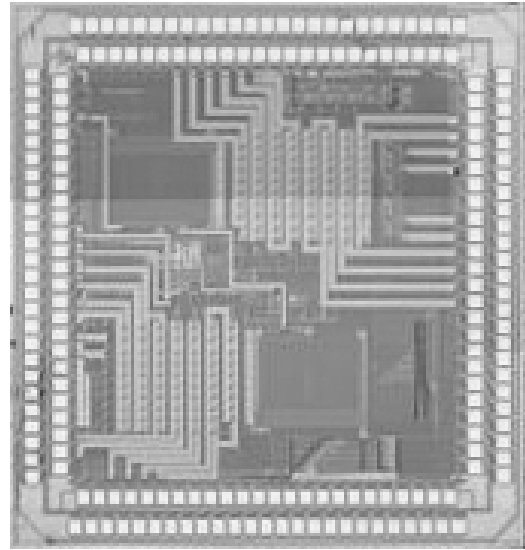


Figure 7. Die photo of DAC chip

Centro-symmetric regions, and then the 16 current sources in every region are divided into 8 Centro-symmetric regions. Since the 16 current sources in every region do not have exactly the residue, there is a remaining small second-order residue. By “random walking” through the 64 current sources, the residual error is not accumulated but rather “randomized”, hence named  $Q^2$  random walk scheme. Only 64 current sources are required for the DAC function. One of the 64 current sources is used as a biasing circuit.

The chip photograph is shown in Figure 7. The chip has been implemented in a 2-poly, 4-metal  $0.35 \mu\text{m}$  CMOS

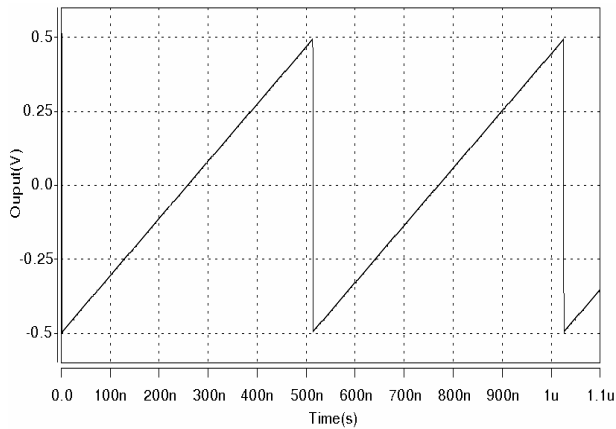


Figure 8. DAC Output

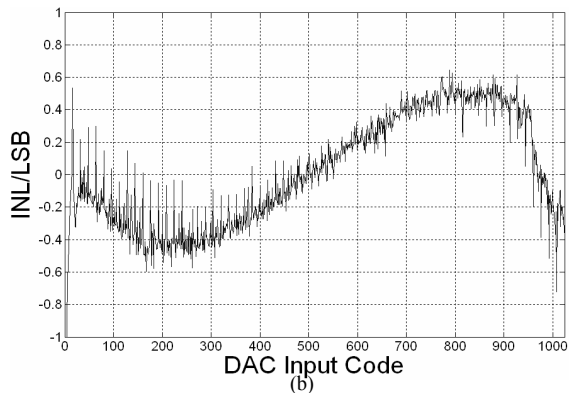
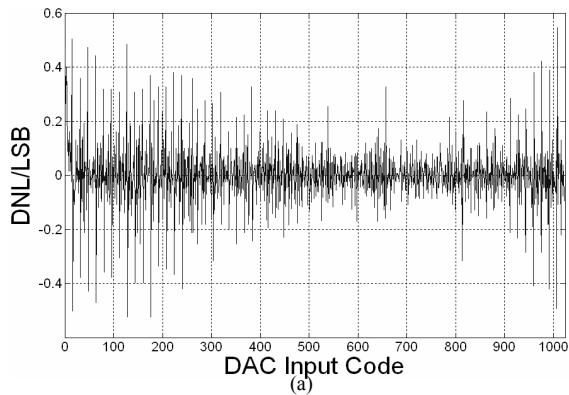


Figure 9. DNL(a) and INL(b) measurement

technology by Chartered Semiconductors, and occupies the active area of  $2.2 \times 2.2 \text{ mm}^2$ . The chip is divided into 2 parts: a simple DAC on the left side of the chip and another DAC with control circuits for certain applications on the right side of the chip.

## V. EXPERIMENT RESULTS

The DAC is simulated in HSpice at a single power supply of 3.3V and the maximum output current for a pair of  $50 \Omega$  termination resistors is 20mA to obtain the maximum single-ended analog output voltage of 0.5V. Figure 8 shows the simulated output of the DAC at a 2GHz update rate, while the input code changes from 0 to 1024. Figure 9 shows the DNL and INL of the DAC. As we can see, the measured DNL and INL of the DAC are both within  $\pm 0.6\text{LSB}$ .

## VI. CONCLUSION

In this paper a 3.3V 10bit 2GHz CMOS DAC is designed. In order to achieve higher speed performance and lower power dissipation, CMOS CML is used to implement the logic cells. The DAC also employs a novel switching scheme called  $Q^2$  random walk in order to improve the linearity of the DAC. The measured DNL and INL of the DAC are both within 0.6LSB. The DAC implemented in Chartered  $0.35 \mu\text{m}$  CMOS technology is in fabrication. The chip die area is  $2.2 \times 2.2 \text{ mm}^2$  and the total power consumption is about 790mw at 3.3V power supply.

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