A 12-bit 300 MHz CMOS DAC for High-speed System Applications

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***Abstract*—This paper describes a 12-bit 300 MHz CMOS DAC for high-speed system applications. The proposed DAC consists of a unit current-cell matrix for 8 MSBs and a binary-weighted array for 4 LSBs. In order to ensure the linearity of DAC, a double Centro symmetric current matrix is designed by using the Q^2 random walk strategy. To minimize the feedthrough and improve the dynamic performance, the drain of the switching transistors is isolated from the output lines by adding two cascoded transistors.**

I. INTRODUCTION

Digital to Analog Converter (DAC) is a very important component of the interface widely used in the modern digital and analog circuits. The performance and the method to build DAC directly influence the range of utilization and the cost of digital and analog mixed system. The trends of VLSI, Mixed Signal and SOC integrated circuits demand high performance DAC. Conventional high-speed high-resolution CMOS DACs have employed a current-steering architecture with advantage of speed and linearity, while some performances have been degraded due to process variation, current-source mismatch, and high glitch energy at outputs.

Current steering DAC's are based on an array of matched current cells organized in unary encoded or binary weighted elements that are steered to the DAC output depending on the digital input code. The segmented architecture is most frequently used to combine high conversion rate and high resolution. In this architecture the least significant bits steer binary weighted current sources, while the most significant bits are thermometer encoded and steer a unary current source array.

The proposed DAC is mainly used in high-speed Direct Digital Frequency Synthesizers (DDFS) modem communication system. Its goal is to design a high performance DAC without trimming based on the 0.35μm CMOS platform. The proposed DAC is composed of a unit current-cell matrix for 8 MSBs and a binary-weighted array for 4 LSBs to obtain high linearity at 12b level. In double centro symmetric current matrix, the Q^2 random walk strategy is adopted to improve the nonlinearity, which can be degraded by symmetrical error and the two-dimensional graded error of the DAC. The delay time difference of digital signals is minimized with the intermediate latches placed in front of the related decoders. In addition, a clock tree is designed to make sure that the difference in delay among all the branches from the source pin to drive pins after routing is minimized.

II. DAC ARCHTETURE

Consider an N bit current steering segmented DAC with a unit current source I: the N1 MSBs control 2^{N1}-1 equal current source of value $2^{N2}I$, and the N_2 LSBs control N_2 binary weighted current sources multiple of I. A simple estimate for the integral nonlinearity (INL) is found by adding the variances of 2^N-1uncorrelated current sources [1].

$$INL \approx \sqrt{2^{N-1}}\left(\frac{\sigma}{I}\right)LSB \qquad (1)$$

Where σ / I is the unit current source relative standard deviation. Equation (1) shows that the INL spec is independent of the segmentation used and it is only a function of the required accuracy. The worst differential nonlinearity (DNL) is defined in the transition from the binary weighted LSBs to the unity decoded MSBs[1].

$$DNL \approx \sqrt{2^{N_2}}\left(\frac{\sigma}{I}\right)LSB \qquad (2)$$

The INL related yield specification imposed a maximum constraint on the allowed mismatch of the unit current source. This constraint results in a minimum channel area dimension for the transistor as is given in Equation (3).

$$W * L = \frac{1}{\frac{2\sigma^2}{I^2}}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right] \qquad (3)$$

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Where A_β and A_{VT} are mismatch technology parameters, and $(V_{GS}-V_T)$ is the gate overdrive voltage of the current source transistor.

To achieve a good DNL and INL specification, the number of bits implemented in the binary weighted part of the DAC has to be small [2]. For every extra bit implemented in the unity decoded part, however, the number of control lines needed to select the current sources doubles, and the decoding logic complexity increases significantly. A direct consequence is often a reduction in the maximum operating speed. Equally important is the fact that the area used by the decoding inside the matrix increases, and consequently the process and electric systematic errors become more difficult to compensate [2]. We will refer to a fully binary-weighted design as 0% segmented, whereas a fully thermometer-coded design is refer to as 100% segmented. Fig. 1 shows the normalized required area versus percentage of segmentation. Based on DNL=0.5LSB performance only, the minimum analog area for 100% segmentation is A_{unit} and the minimum analog area for 0% segmentation is $4096A_{unit}$. On a logarithmic scale, the minimum analog area requirement as a function of segmentation will form a straight line connecting the above mentioned points. If A_d is the required area for the digital decoding logic per current source, the total digital area equals $2^M A_d$, where M is the number of bits in the MSB section. In addition, the area occupied by interconnections insides the decoding circuit quickly increases with the augment of M. On a logarithmic scale, the area of decoding logic and interconnections as a function of segmentation is a curve line as shown in Fig. 1. The area of interconnections is obtained using Silicon Ensemble (SE) that is used to produce a layout of the netlist generated by the synthesis tool. With the increasing of the percentage of segmentation, the required total area is first dominated by the DNL requirement, then by the INL requirement, and finally by the decoding logic. As a result, when the system requirement is DNL=0.5LSB and INL=1LSB, the required area versus percentage of segmentation is as indicated by the thick line in Fig. 1. In addition, thermometer coding has additional advantages with respect to glitch performance. As soon as the segmentation is less than 100%, glitches will contribute to distortion, particularly at higher frequencies. As a result, the best performance is obtained at the “optimal point” in Fig. 1, the point locate in 0.6~0.7

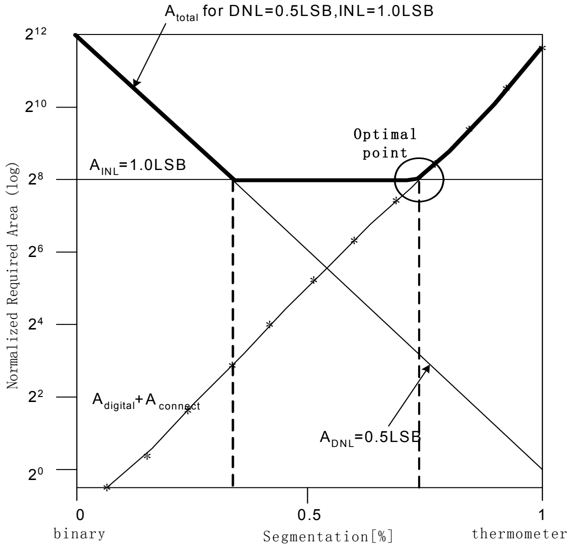


Fig. 1. Normalized required area versus percent of segmentation

III. DAC IMPLEMENTATION

The 12-bit DAC is implemented as a segmented current DAC. Fig.2 gives a schematic representation of realized chip. The DAC is composed of the unit current-cell matrix for 8 MSBs and the binary-weighted array for 4 LSBs, considering the error of circuit, yield, and chip area at 12-bit resolution.

In the unit decoded matrix, it is difficult to make current sources identical due to layout mismatches, output impedance of the current source and switch, edge effects, voltage drops in the supply lines, thermal gradients, doping gradient and oxide thickness. The nonlinear secondary effects cause graded, symmetrical, and random errors, resulting in the reduced linearity of DAC’s. The proposed DAC employs a novel switching scheme to minimize the degradation of integral linearity caused by mismatches of current sources. This switching scheme will be referred to as quad quadrant (Q^2), as four (quad) units in every quadrant altogether compose one current source [3]. The proposed DAC employs extra digital latches just before the unit current cells to synchronize the digital inputs as well as the cascoded current sources to minimize the current variation effect [4].

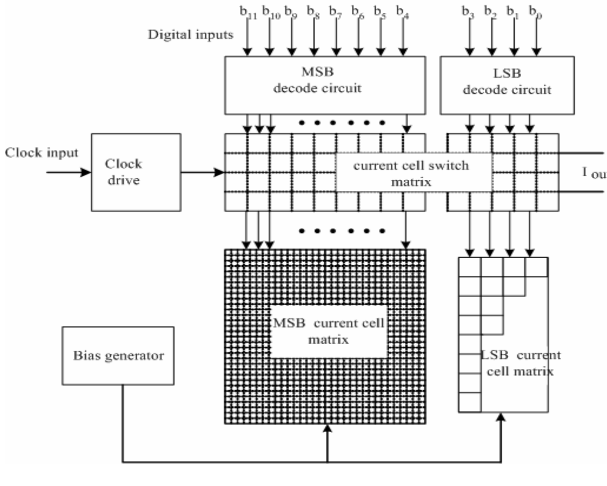
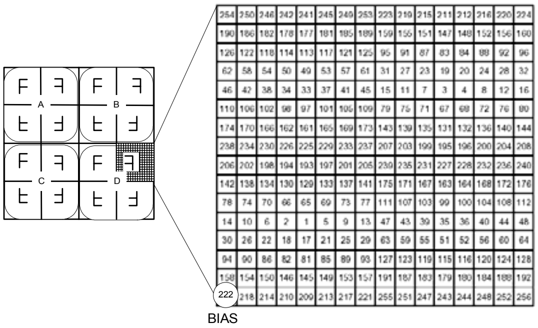


Fig. 2. Simplified DAC architecture with current steering matrix.

In the 12-bit DAC presented in [5], every source array is split into four units of 1/4 the value. By splitting the current source, a spatial averaging of the error is achieved. However the quadratic errors are left unaltered. In order to suppress the quadratic error, the current source must be split in a higher number of current source units. By splitting the current source into 16 units, the systematic and graded errors are suppressed. The 256 current sources are divided into 16 Centro symmetric regions, and then the 16 current sources in every region are divided into 16 Centro symmetric regions, as shown in Fig. 3. Since the 16 current sources in every region do not have exactly the same residue, there is a remaining small second-order residue. By "random walking" through the 256 current sources, the residual error is not accumulated but rather ""randomized", hence the name Q^2 Random Walk switching scheme. Only 255 current sources are required for the DAC function. One of the 256 current sources is used as a biasing circuit. The simulated DNL and INL of the proposed switching scheme are ±0.3LSB and ±0.4LSB.



254	250	246	242	241	245	249	253	223	219	215	211	212	216	220	224
190	186	182	178	177	181	185	189	159	155	151	147	148	152	156	160
126	122	118	114	113	117	121	125	95	91	87	83	84	88	92	96
62	58	54	50	49	53	57	61	31	27	23	19	20	24	28	32
46	42	38	34	33	37	41	45	15	11	7	3	4	8	12	16
110	106	102	98	97	101	105	109	79	75	71	67	68	72	76	80
174	170	166	162	161	165	169	173	143	139	135	131	132	136	140	144
238	234	230	226	225	229	233	237	207	203	199	195	196	200	204	208
206	202	198	194	193	197	201	205	239	235	231	227	228	232	236	240
142	138	134	130	129	133	137	141	175	171	167	163	164	168	172	176
78	74	70	66	65	69	73	77	111	107	103	99	100	104	108	112
14	10	6	2	1	5	9	13	47	43	39	35	36	40	44	48
30	26	22	18	17	21	25	29	63	59	55	51	52	56	60	64
94	90	86	82	81	85	89	93	127	123	119	115	116	120	124	128
158	154	150	146	145	149	153	157	191	187	183	179	180	184	188	192
222	218	214	210	209	213	217	221	255	251	247	243	244	248	252	256

Fig. 3. Switching sequence the Q^2 *Random Walk* switching scheme

It is well known that the dynamic performance of current steering DAC's is limited by digital signal feed-through through the gate-drain capacitance from the current switches directly to the output. This project is to minimize the feedthrough to the output lines, the drain of the switching transistors is isolated from the output lines by adding two cascoded transistors (with the same dimensions as the switching transistors), as shown in Fig. 4 [6].

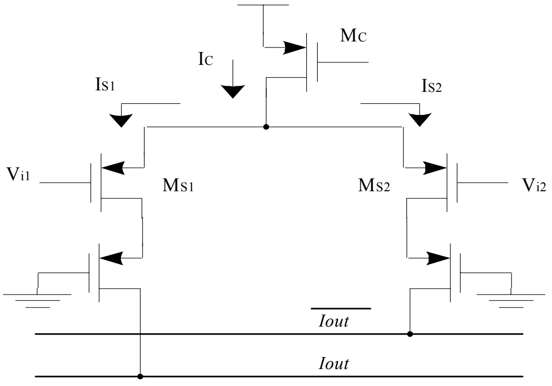


Fig. 4. Current cell with cascaded transistors

The chip photograph is shown in Fig. 5. The chip has been implemented in a 2-poly and 4-metal 0.35μm CMOS process and occupies the active die area of 2.2 mm × 1.6 mm. The digital encoder was placed on the top of the chip, far away and well shielded form the sensitive analog parts. During the layout of the current sources matrix, Cadence Skill language is used to help the sorting and routing of the unit current sources, which greatly improves the design efficiency and guarantees the success of the tape out. Different power supply lines have been used for different parts of the circuit to reduce the noise coupling to the sensitive analog blocks [7]. Finally, in the very few exceptions where digital signals cross sensitive analog lines, a cleanly biased metal line is used as shield. The clock driver which drives the digital encoder and the analog latches in the switch array has been added the chip. The clock is distributed through a tree, to ensure low skew between the different analog latches (see Fig. 5). The clock tree is routed on the top level metal layer (lowest capacitance).

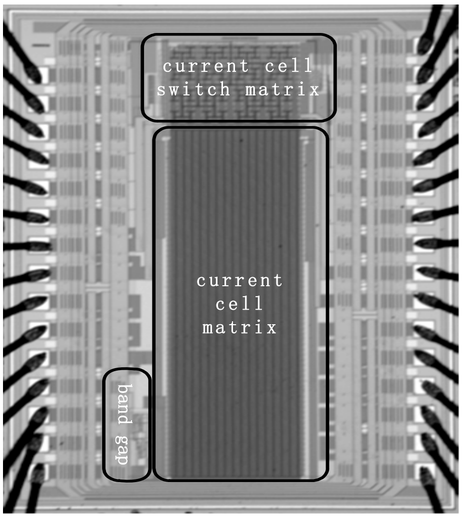


Fig. 5. Chip photograph of the D/A converter

IV. EXPERIMENTAL RESULTS

The DAC was measured at a 3.3V and the maximum output current to the 50Ω termination resister is 20mA to obtain the maximum single-ended analog output voltage of 1V. As show in Fig.6 and Fig. 7, the measured DNL and INL of the prototype DAC are within ±0.5LSB and ±0.6LSB, respectively. Fig. 8 shows the output spectrum of the DAC with a 10MHz input signal at the sampling frequency of 300MHz. The measured spurious-free dynamic range (SFDR) is 62dB. Fig. 9 shows the measured SFDR of the prototype DAC with different input signal frequencies at 300MHz.. The measured performance of the prototype DAC is summarized in Table Ⅰ

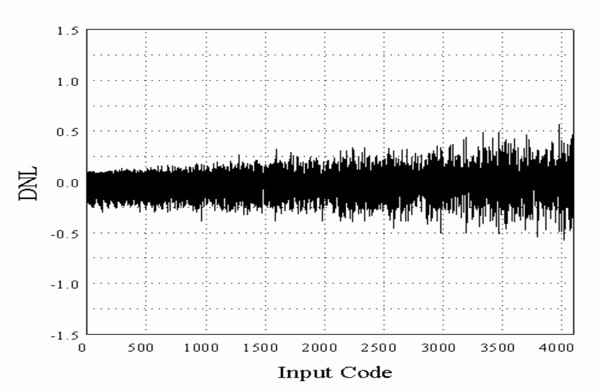


Fig. 6 DAC differential nonlinearity characteristic

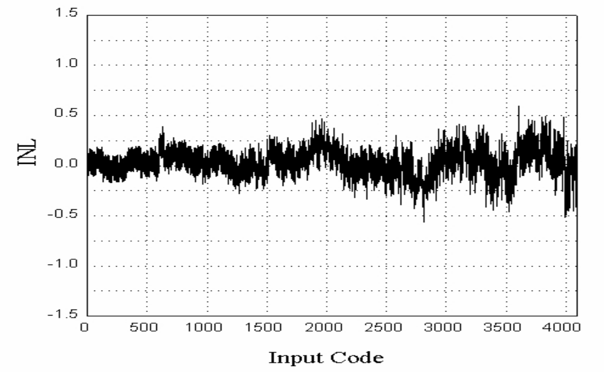


Fig. 7 DAC integral nonlinearity characteristic

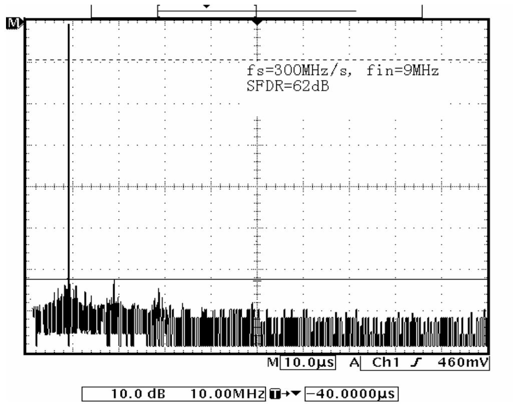


Fig. 8 output spectrum of the prototype DAC

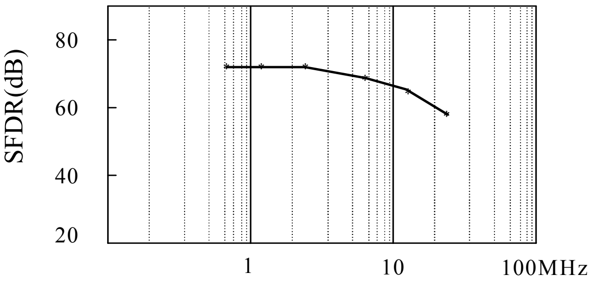


Fig. 9 Measured SFDR

TABLE I.
MEASURED PERFORMANCE OF THE PROTOTYPE DAC

Resolution	12bit
Update rate	300Mhz
DNL	±0.5LSB
INL	±0.6LSB
SFDR	62dB(9Mhz@300MSPS)
Power voltage	3.3V
Power dissipation	150mW@300Mhz,3.3V
Process	0.35µm

V. CONCLUSION

In this paper a 3.3V 12b 300MS/s CMOS DAC for high-speed system applications is proposed. The DAC employs a novel switching scheme called Q^2 Random Walk and a variety of layout techniques simultaneously to improve the static and dynamic performances. DAC consumes 82mW in the total power consumption with a 3.3V supply at 300MHz. The measured DNL and INL are within ±0.5LSB and ±0.6LSB, respectively, and the SFDR is 62dB for a 9MHz input at 300MHz.

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