

An High Speed Integrated Equalizer for Dispersion Compensation in 10Gb/s Fiber Networks

Vasanth Kakani, *Student Member, IEEE*, Foster F. Dai, *Senior Member, IEEE*, Richard C. Jaeger, *Fellow, IEEE*
 Department of Electrical and Computer Engineering
 200 Broun Hall, Auburn University, Auburn, AL 36849-5201, USA

Abstract—This paper presents the design of a high-speed analog transversal equalizer for dispersion compensation in 10Gb/s fiber networks. We present design details of a seven tap transversal equalizer with delay amplifiers and tap variable gain amplifiers. The seven tap equalizer is implemented in a 47GHz SiGe technology¹.

I. INTRODUCTION

Modal, chromatic and polarization mode dispersions are the major sources of transmission impairments in high data rate fiber communications. Optical solutions are only capable of compensating one form of the dispersions with very high cost, high insertion loss and slow tuning speed if they are tunable at all. Further cost reduction is possible if electronic equalizer and other circuits on the receiver are integrated on the same die. Continuous time equalizers based on Gm-C ladder and switch capacitor filters have been explored previously for high speed applications but failed to reach 5GHz speed. In recent years integrated Microwave waveguides and microstrip lines having linear delay versus frequency characteristic in the centre of their pass-band have been used to compensate linear delay distortion, however they must be built to precisely match the linear delay and are not adaptive[1]. Transversal equalizers using SiGe technology have been reported previously [2] but no detailed information is provided about the circuit implementations. In [3] a fractionally spaced equalizer was designed in a distributed traveling wave fashion using passive transmission lines as delay elements. Our design is based upon a commonly used SiGe technology with $f_t=47\text{GHz}$ and thus has the potential to be integrated in the whole receiver IC for cost reduction.

II. INTEGRATED TRANSVERSAL EQUALIZER

The block diagram of the transversal equalizer chip is shown in Fig.1, and the schematic of the fractional-spaced transversal equalizer is illustrated in Fig.2. The equalizer structure is a tapped analog delay line with feed forward taps forming an FIR filter. The transfer function of the integrated equalizer can be adaptively adjusted by its tap weights. Changing the tap weights affects the locations of zero's, while the poles of the filter are fixed, and hence it is always stable. The aliasing problem in T (symbol period) spaced equalizer can be eliminated in fractional spaced equalizer there by improving the equalizer performance [1]

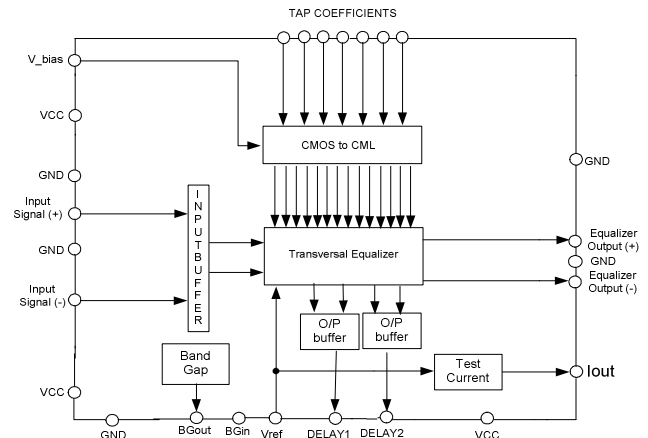


Figure.1 Block diagram of the equalizer chip.

Delay of half the symbol period has been found to be adequate for dispersion compensation in most light wave systems [1]. It should be noted that any phase nonlinearity introduced by the equalizer can add additional dispersions that can not be rectified by the equalizer itself and reduces the compensation range of the equalizer.

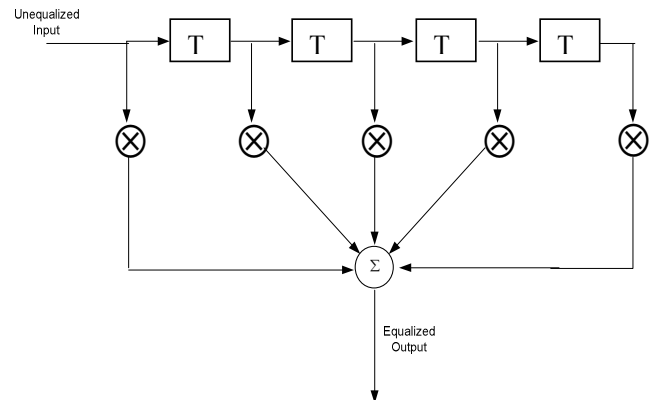


Figure.2 Linear transversal equalizer.

A. Delay Stage

As shown in figure.3, the delay stage is implemented using unity gain amplifiers, where the circuit is dimensioned to provide 50ps delay. For application in 10Gbit/s circuits the delay amplifier has to maintain constant unity gain from low frequency to at least 7 GHz and provide a delay of 50ps while maintaining a high cutoff (3-dB) frequency. Therefore to satisfy the stringent bandwidth and group-delay requirements it is necessary to use wideband amplifiers that have complex pair of poles.

¹The fabrication of this work is supported by MOSIS under the MEP research program.

The delay stage consists of series-shunt cascade (Cherry-Hooper amplifier [4]) where the series feedback stage is a trans-conductance amplifier and shunt feedback stage is a trans-impedance amplifier. The amplifier with serial feedback is driven from a low resistance voltage input obtained from the output of shunt feedback stage, and conversely the amplifier with shunt feedback is driven from a high resistance current input obtained from the output of serial feedback stage. This arrangement is advantageous since while cascading several such delay stages the impedance level requirements at the input and output of the delay stage will be satisfied. A seven tap equalizer consists to 6 delay stages cascaded in series. Emitter followers are used in between the delay stages for level shifting and creating stronger impedance mismatch between succeeding stages

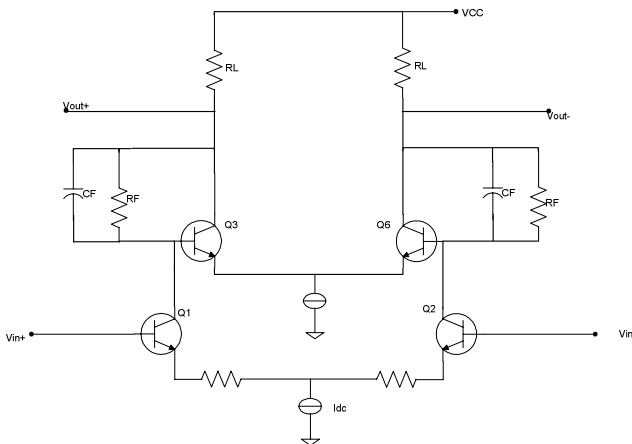


Figure.3 Delay amplifier.

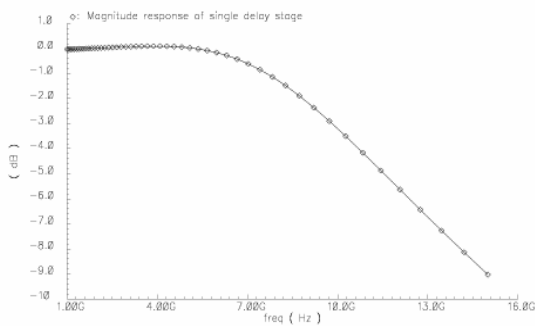


Figure.4 Magnitude response of the delay stage with 3-dB bandwidth at 10 GHz.

Figures 4 and 5 give the magnitude and phase response of the delay amplifier. The 3-dB cutoff frequency is 10 GHz and phase response is linear up to 9GHz. Figure 6 shows the signal being delayed by 50ps as it passes through individual delay stage. With input signal at 5 GHz, and a delay of 50ps per stage, the inputs of tap1 and tap5 are in phase as expected, also the signal amplitude is maintained constant as it is passed through six stages of delay amplifier. Figure 7 shows the magnitude response of six delay amplifiers in cascade. Since the input output

impedances of the two feedback stages are frequency dependant, the frequency response of the amplifier could be compensated (linear phase relation between input and output signal) by using feedback capacitors.

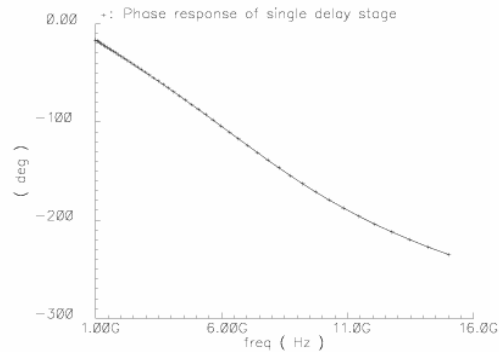


Figure.5 Phase response of delay stage.

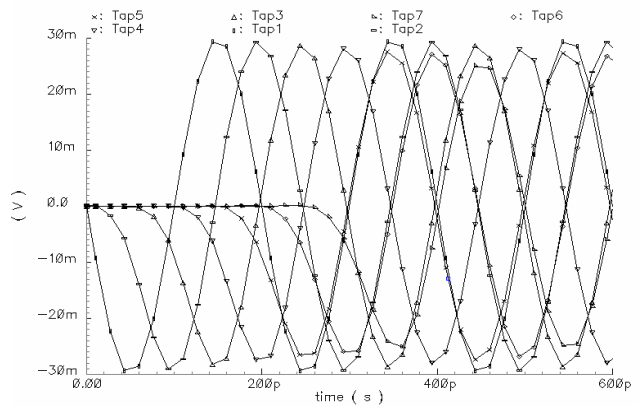


Figure.6 Waveforms delayed by 50ps as it passes through each delay amplifier.

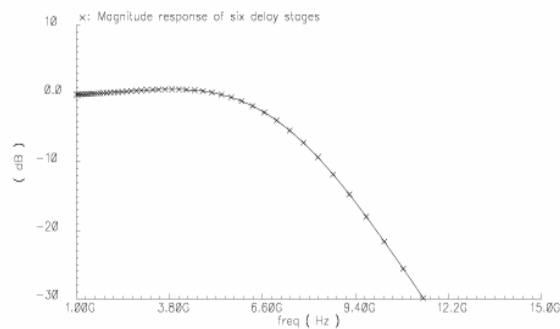


Figure.7 Frequency response of six delay cascaded stages with 3-dB bandwidth at 7 GHz.

B. Gain Stage

The tap gain stage is implemented using Gilbert variable gain amplifier shown in Fig.8 to adjust the tap weights between 0 and 1. Thus, the variable gain stage is in

fact a variable loss stage. Changing the polarity of gain control coefficients a phase shift of 180° is obtained for providing negative coefficients. Figure 9 shows the small signal model of the gain control circuit in Gilbert cell. Since it is a differential operation, analysis of its half circuit is sufficient. The Gilbert cell is basically a current amplifier with the following current gain transfer function. Figures 10 and 11 show the magnitude and phase response of the Gilbert cell.

$$I(s) = \frac{gm_3(1+sC_{x3}r_b) - gm_4(1+sC_{x3}r_b)}{\left(gm_3 + sC_{x3} + \frac{1}{r_{x3}}\right)(1+sC_{x4}r_b) + \left(gm_4 + sC_{x4} + \frac{1}{r_{x4}}\right)(1+sC_{x2}r_b)} \quad (1)$$

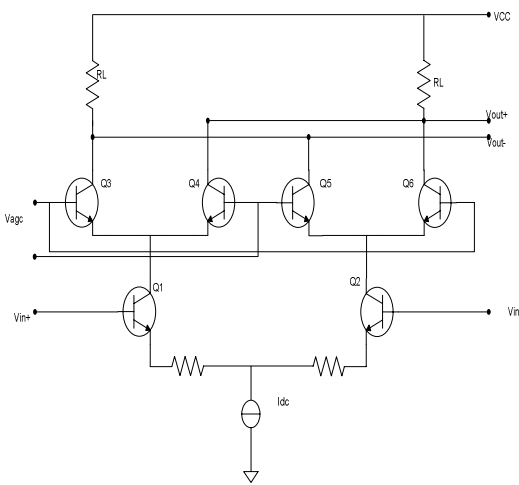


Figure.8 Tap variable gain stage using Gilbert cell.

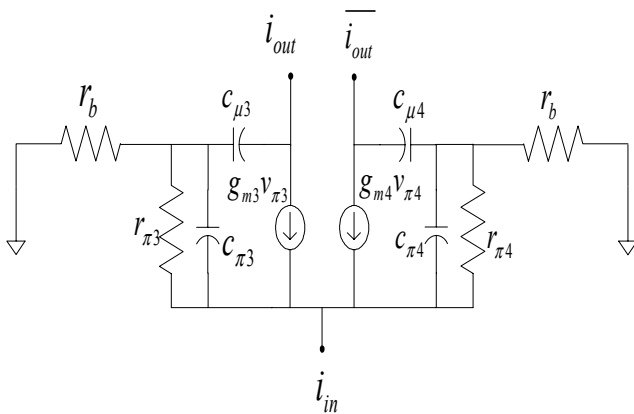


Figure.9 small signal model of the gain control circuit.

C. Summation

Summation is performed in current mode. The current signal outputs of all the taps are tied together to a pull up resistor via a current buffer (common-base amplifier).

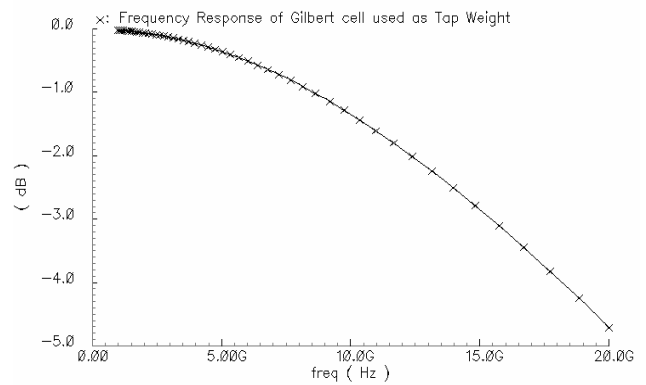


Figure.10 Magnitude response of the Gilbert variable gain amplifier. The 3-dB frequency is 14.5 GHz.

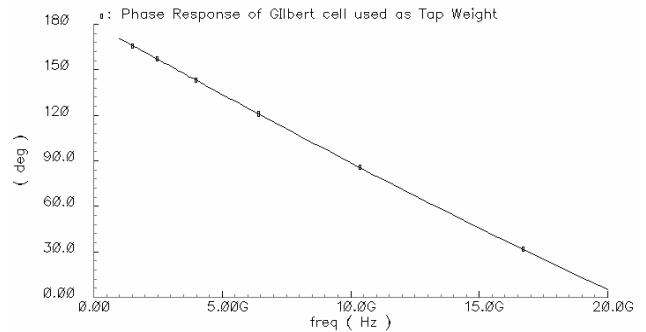


Figure.11 Phase response of the Gilbert variable gain amplifier

III. FIBER DISPERSION COMPENSATION USING EQUALIZER

To demonstrate the effect of electronic equalizer on fiber dispersion compensation, we have conducted system level simulations in MATLAB. The transfer function for first order polarization mode dispersion (PMD) is

$$|H(f)| = \sqrt{1 - 4\gamma(1 - \gamma)\text{Sin}^2\left(\frac{\pi\tau}{T}\right)} \quad (2)$$

where γ is the splitting ratio of the signal as it travels through the two modes of propagation in a single mode fiber, τ is the differential group delay (DGD) between the signal's traveling through the two modes, T is the bit period. Figure.12 shows the first order PMD transfer function for different values of γ .

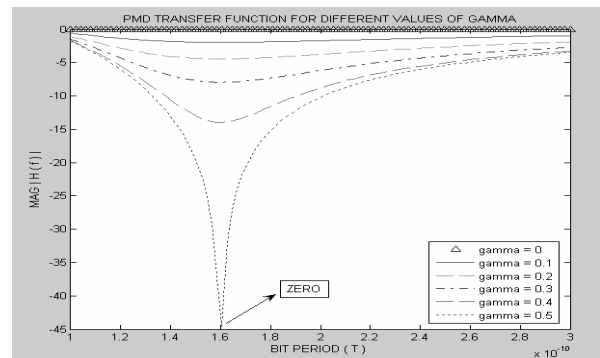


Figure.12 PMD Transfer functions for different power splitting ratio γ .

We simulated a 7-tap analog feed forward equalizer with an LMS feedback algorithm for PMD compensation. The severely distorted signal can be compensated using just 7 taps in an analog transversal equalizer [5]. For a fixed network, we can thus predetermine the equalizer tap coefficients and load them into the equalizer, which is very attractive from a cost reduction point of view.

For chromatic dispersion, tap coefficients can be programmed based on the length and type of the fiber, providing a much more economic way than the current solution using dispersion compensation fiber (DCF), which is static and also wavelength dependent.

IV. SIMULATION RESULTS

A high speed analog equalizer with 7 taps is implemented in a 47GHz SiGe technology. Each tap is modeled as a delay stage and a variable gain amplifier. The average tap delay was measured to be 50ps. The single tap bandwidth is between 10 GHz to 7 GHz depending on the considered tap. Band width of the second tap when all other taps are set to zero is 8.4 GHz and bandwidth of seventh tap when all other taps are set to zero is 7 GHz. The change in the tap bandwidth required to provide 300ps delay is 1.4GHz.

Adjusting the tap coefficients it is possible to adapt zero's at various frequencies and implement different filter characteristics such as band-pass, low-pass, notch filters as shown in Figure 13 and 14. Thus the equalizer can effectively mimic the inverse transfer function of dispersive channels that introduce linear distortion. Figure 15 shows the equalizer layout diagram with 1.2 x 1.8 mm² die size including input/output pads. The power consumption of entire chip is 250mw.

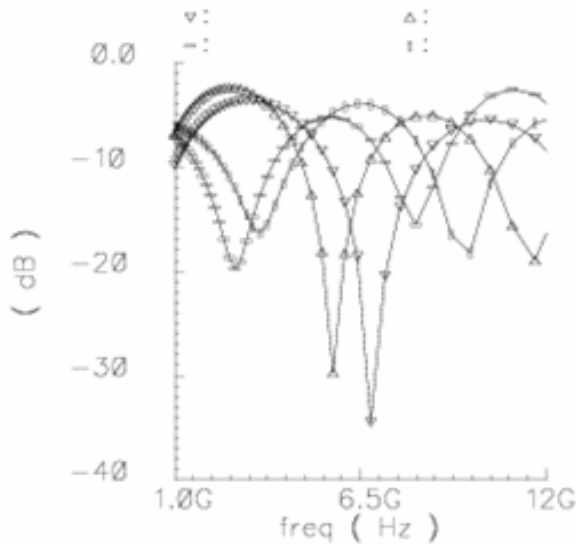


Figure.13. Adapting zero's at various frequencies by tuning tap coefficients.

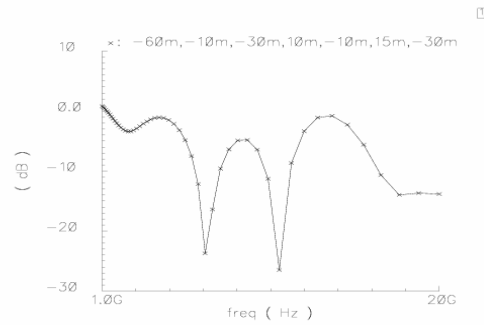


Figure14. Bandpass response with equalizer coefficients of -60m,-10m,-30m,30m,-10m,15m,-30m.

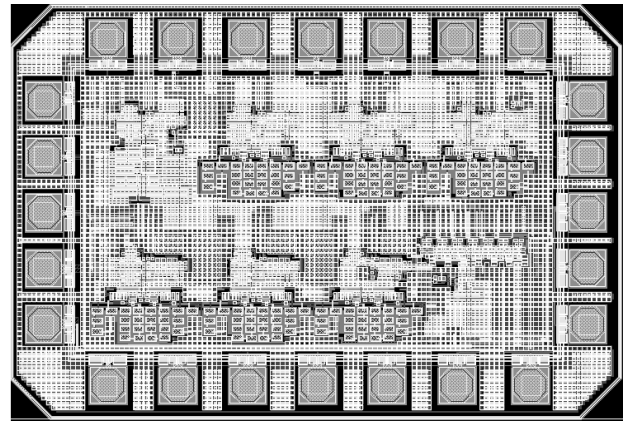


Fig.15. SiGe transversal equalizer layout diagram.

CONCLUSIONS

We have implemented a 10Gb/s high-speed analog equalizer with 7 taps in a low cost 47GHz SiGe technology. The circuit is optimized for minimum group delay and maximum bandwidth. The power consumption of the proposed delay amplifier to provide a delay of 50ps is 4.2mw. The power consumption of entire chip is 250mw. The chip dimensions are 1.2mm*1.8mm.

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