

Integrated Electronic Equalizer For Dispersion Compensation In 10Gb/s Fiber Networks

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ABSTRACT: This paper presents the design of a high-speed transversal equalizer for dispersion compensation in 10Gb/s fiber networks. The five-tap equalizer is implemented in a 47GHz SiGe technology. The equalizer circuit is optimized for minimum group delay and maximum bandwidth. With added feedback in equalizer gain stage, we achieved minimum group delay of 0.7% data period. Polarization mode dispersion compensation has been demonstrated using the proposed transversal equalizer.

Index Terms — transversal equalizer, SiGe, high-speed integrated circuits, fiber dispersion.

I. INTRODUCTION

Modal, chromatic and polarization mode dispersions are the major sources of transmission impairments in high data rate fiber communications. The presence of high dispersion will increase the bit error rate (BER) to unacceptable rates due to intersymbol interference (ISI) thereby imposing restrictions on the maximum link length that can be covered with out the need for signal regeneration. Without proper compensation, the performance of the fiber communication systems will thus be severely limited. Till recently techniques to compensate dispersion has occurred in optical domain with expensive and bulky solutions. The available dispersion compensation fiber is static in nature, and does not support agile optical networks. Other optical solutions are only capable of compensating one form of the dispersions with very high cost, high insertion loss and slow tuning speed if they are tunable at all. This paper presents an electronic equalizer for the compensation of fiber dispersions. Further cost reduction is possible if electronic equalizer and other circuits on the receiver are integrated on the same die. An electronic equalizer

module is superior considering its cost, size, reliability, flexibility and speed. In this work integrated electronic equalizer is designed for dispersion compensation at 10Gb/s fiber networks. A constant modulus blind adaptive algorithm is proposed to provide reference-free feedback. The blind feed back algorithm is to be implemented in an FPGA with 100MHz operation frequency.

II. EQUALIZER CIRCUIT DESIGNS

In the recent years integrated 10Gb/s signal processing MMIC using SiGe technology have been reported [2-5]. However no detailed information is provided about the circuit implementations. In [6] a fractionally spaced equalizer was designed in a distributed traveling wave fashion using passive transmission lines as delay elements. The 10Gb/s equalizer design in [6] used an expensive SiGe technology with $f_T=120\text{GHz}$, which does not match the technology used for most 10Gb/s receiver ICs and thus cannot be integrated with the existing 10Gb/s CDR chips for further cost reduction. Our design is based upon a commonly used SiGe technology with $f_T=47\text{GHz}$ for 10Gb/s fiber networks and thus has the potential to be integrated in the whole receiver IC for cost reduction. The proposed equalizer design achieves high bandwidth and low group delay variation due to the circuit optimizations for gain and delay elements.

The idea of using signal processing techniques for compensating dispersion in optical fiber communications was first mooted by [1]. The proposed linear transversal equalizer with one bit period delay is illustrated in Fig.1. The poles of the equalizer are fixed and its zeros can be adjusted by changing the tap-weights. The tap gain stage is implemented using Gilbert cells as shown in Fig.2 to adjust the tap weights between 0 and 1. Thus, the variable

gain stage is in fact a variable loss stage and its output ensures the equalizer output will not be blown up under any circumstance. The variable gain stage should also be able to provide a phase shift of 180° for negative coefficients. The tap gain stage has to be designed to have maximal flat response and minimum group delay.

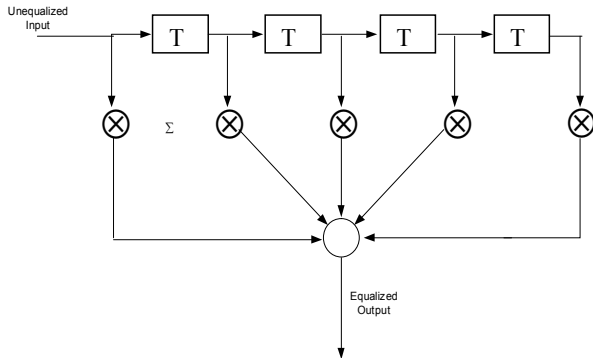


Fig. 1 Linear transversal equalizer.

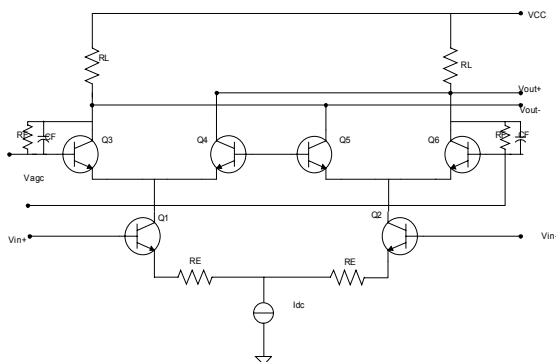


Fig. 2 Gain control circuit (Gilbert Cell) to adjust the tap weights

Figure 3 shows the small signal model of the gain control circuit in Gilbert cell. Since it is a differential operation, analysis of its half circuit is sufficient. Iout is the sum of currents flowing through the collectors of Q3 & Q4.

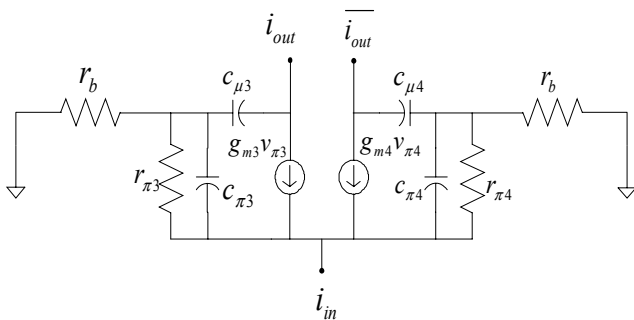


Fig. 3. Small signal model of the gain control circuit.

The Gilbert cell is basically a current amplifier with the following current gain transfer function

$$I(s) = \frac{gm_3(1 + sC_{\mu 3}r_b) - gm_4(1 + sC_{\mu 4}r_b)}{\left(gm_3 + sC_{\pi 3} + \frac{1}{r_{\pi 3}}\right)(1 + sC_{\mu 3}r_b) + \left(gm_4 + sC_{\pi 4} + \frac{1}{r_{\pi 4}}\right)(1 + sC_{\mu 4}r_b)} \quad (1)$$

The magnitude and phase response of the Gilbert cell is shown in Fig.4. It can be seen in Fig.4 that the maximum group delay variation over a frequency range of 18GHz is 700fs, which is only 0.7% of the data period. The bandwidth of the variable gain stage is larger than 15GHz, which is enough to handle the 10Gb/s NRZ signal. The weighted differential signals are summed at the output through a pair of external pull-up resistors. The design challenge is to keep the equalizer with minimum group delay since any phase nonlinearity introduced by the equalizer can add additional dispersions that can not be rectified by the equalizer and reduce the compensation range of the equalizer.

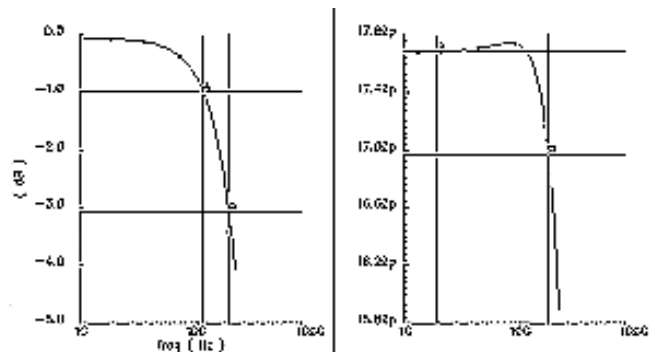


Fig. 4 Gain and group delay of the Gilbert cell with feedback. The maximum group delay variation over a frequency range of 18 GHz is about 700fs.

The delay stage provides propagation delay of 100ps. We have selected the series shunt cascade (Cherry-Hooper) amplifier with unity gain as the delay element as shown in Fig.5. since while cascading the delay blocks it is advantageous to alternate between series feedback and shunt feedback such that impedance level requirement of each stage is satisfied. The shunt feed-back stage provides a low impedance drive for the series cascade and the series feedback stage output provides the high impedance drive for the shunt feed back stage. This is advantageous for cascading the delay cells as it creates strong impedance mismatching between succeeding stages [7]. The delay is an analog delay since no clock has been extracted yet. The group delay of the delay cell can be

further improved at high frequency using additional elements such as feed back capacitors CF2 and CF1.

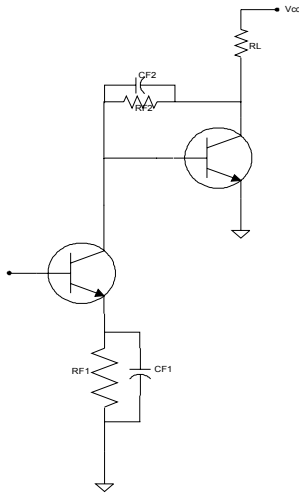


Fig. 5 Series shunt cascade Cherry-Hooper amplifier used as a delay element. Double-ended differential form is used in the circuit.

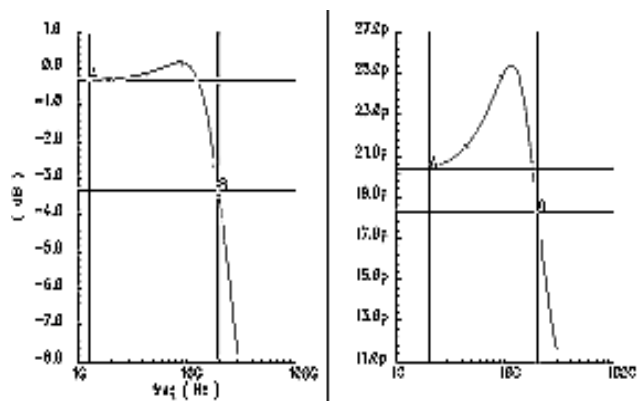


Fig. 6 Gain and group delay of the delay cell. The group delay through one delay stage is 2ps.

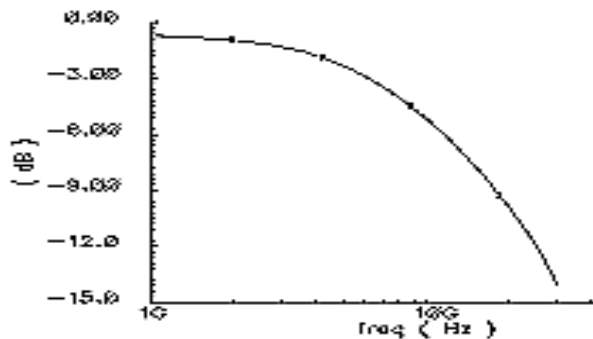


Fig. 7. The equalizer tap band-width including the variable gain stage and the delay stage.

Fig.6 shows the simulated magnitude and phase response of the delay cell implemented in a 47 GHz SiGe technology. The group delay through one delay-stage is 2ps, which is about 2% of the bit period. For a linear

transversal equalizer operating at 10Gb/s data rate, the delay should be 100ps. Hence we need to select a proper transistor size and bias point to get a required 100ps delay. The equalizer tap band-width including the variable gain stage and the delay stage is about 7GHz as shown in Fig. 7.

III. EQUALIZER SIMULATION RESULTS

Using the gain and delay blocks described above, a five tap equalizer has been implemented in a 47 GHz SiGe technology. Fig.8-Fig.11 gives the simulated equalizer outputs with specified tap gains. It demonstrates that the equalizer can adapt zero's at various frequencies depending on the tap settings and hence can implement various filter characteristics such as low-pass, notch, band-pass and high-pass. Thus, the equalizer is capable of constructing an inverse transfer function of the dispersive channel for dispersion compensation. T1~T5 are the 5 tap weights in the transversal equalizer.

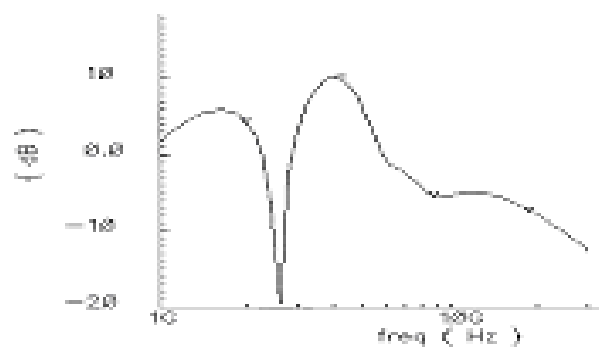


Fig. 8. A notch filter implemented using the equalizer with the following tap weights T1=150m, T2=25m, T3=140m, T4=50m, T5=75m.

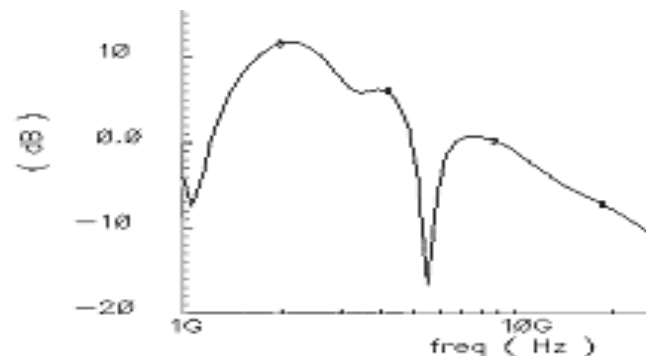


Fig. 9. A band-Pass filter implemented using the equalizer with the following tap weights T1 = - 30m, T2 = - 125m, T3=150m, T4=50m, T5 = - 85m.

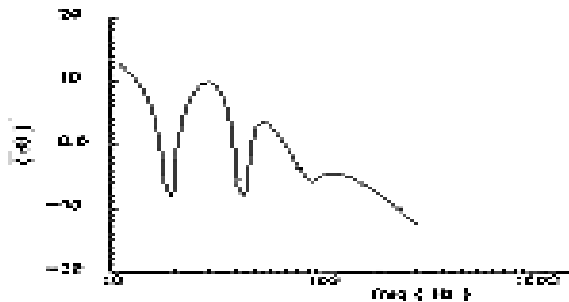


Fig. 10. Two notch filters implemented using the equalizer with the following tap weights $T1 = -30m$, $T2 = -125m$, $T3=150m$, $T4=50m$, $T5 = -85m$.

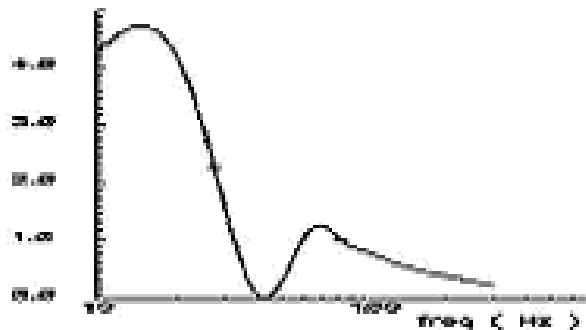


Fig. 11. A low pass filter implemented using the equalizer with the following tap weights $T1 = -30m$, $T2 = -125m$, $T3=150m$, $T4=50m$, $T5 = -85m$.

IV. DISPERSION COMPENSATION USING THE PROPOSED EQUALIZER

To demonstrate the effect of electronic equalizer on fiber dispersion compensation, we have conducted system level simulations in MATLAB. We simulated a 7-tap analog feed forward equalizer with an LMS feedback algorithm for PMD compensation as shown in Fig.12. Notice that the severely distorted signal can be compensated using just 7 taps in an analog transversal equalizer. With adaptive feedback, the tap coefficients are constantly adjusted based on the error signal. Even without feedback, the fixed coefficient equalizer can still open the distorted eye. For a fixed network, we can thus predetermine the equalizer tap coefficients and load them into the equalizer, which is very attractive from a cost reduction point of view.

LMS algorithm requires the training sequence, which adds an overhead and thus reduces the throughput of the system. In a blind equalization, instead of using the training sequence, one or more properties of the transmitted signal are used to estimate the inverse transfer function of the channel. We propose to a blind equalization scheme using constant-modulus adaptive algorithm, which provides a reference-free equalization

and meets the current fiber communication transmission standard. Blind equalization is critical for agile optical networks, where the channel environment varies constantly. Polarization mode dispersion compensation has been demonstrated using the proposed transversal equalizer with a CMA blind equalization algorithm.

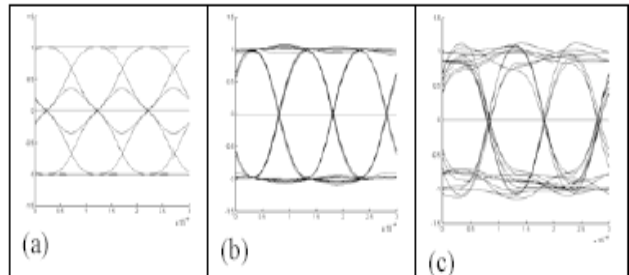


Fig.12. PMD compensation using a 7 tap transversal equalizer. (a) Eye diagram distorted by 1st order PMD with power splitting ratio = 0.5 and DGD = 0.8 period. (b) Compensated eye diagram with LMS adaptive feedback. (c) Compensated eye diagram with fixed tap coefficients.

V. CONCLUSIONS

We have implemented a 10Gb/s high-speed analog equalizer with 5 taps in a low cost 47GHz SiGe technology. The circuit is optimized for minimum group delay and maximum bandwidth. The equalizer MMIC is capable to compensate fiber dispersions, modal and polarization mode dispersions. The designed equalizer MMIC is to be fabricated in a 47 GHz SiGe processing.

VI. REFERENCES

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