

A Low Power 5 GHz Direct Digital Synthesizer Designed In SiGe Technology

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Abstract—This paper presents a low power high-speed direct digital synthesizer (DDS) design designed in a 47GHz SiGe technology. The ROM-less DDS includes an 8-bit accumulator and an 8 bit cosine-weighted digital-to-analog converter (DAC) operating at maximum 5GHz clock frequency. The DDS core occupies an area of 2 mm² and consumes less than 2W power with a 3.3V supply voltage. The 5GHz MMIC provides a frequency synthesis and modulation means for L-band applications.

Index Terms—direct digital synthesizers, DAC, frequency synthesizers, SiGe, high-speed integrated circuits.

I. INTRODUCTION

Direct digital synthesis (DDS) provides precise frequency resolution and direct modulation capability. However, the majority of the DDS designed so far is limited to low frequency applications with clock frequencies less than a few hundred MHz. Digitally generating highly complex wide bandwidth waveforms at the highest possible frequency instead of down near baseband would considerably reduce the transmitter architecture in terms of size, weight and power requirements as well as cost.

This paper presents a low power high-speed DDS design with maximum clock frequency of 5GHz to synthesize and modulate the inter-median frequency (IF) of up to L-band. The high-speed DDS includes an 8-bit accumulator, column/row decoders and a cosine-weighted DAC with 8-bit resolution to achieve better than -45dB spectral purity. The cosine weighted DAC eliminates the sine look-up table, which is the speed and area bottleneck for high-speed DDS implementations. The DDS modulation waveform configurations include chirp, step frequency, FM, MSK, PM, AM, QAM, and other hybrid modulations. The DDS is implemented in a 47GHz SiGe technology with 2 mm² die size and less than 2W power under a 3.3V supply voltage. The low power consumption we achieved using SiGe technology is much lower than that of an equivalent DDS implemented in a 137GHz InP technology [1], where the

DDS consumes about 15 W, operating at 9.2GHz clock frequency with an 8bit accumulator and an 8-bit nonlinear DAC.

II. DDS CIRCUIT DESIGNS

The conventional DDS architecture utilizes a ROM look-up table to convert the accumulated phase word into sine/cosine words that are further used to drive a linear binary weighted DAC. The speed bottleneck of a conventional DDS architecture lies upon the large look-up table with multi-level decoders. The huge look-up table not only restricts high speed operation, but also occupies large area and consumes large amount of power. To reduce the power dissipation and the die size, a nonlinear DAC with cosine-weighted current cells is employed in this design as shown in Fig.1. The nonlinear DAC converts the digital phase information directly into an analog output. The proposed architecture exploits the quadrant symmetry property of the sine function around $\pi/2$ and π . Thus the 2 MSB's of the accumulator output signify the different quadrants of the sinusoid. The remaining $w-2$ bits from the complementor are used to generate the waveform of sinusoid in the first quadrant.

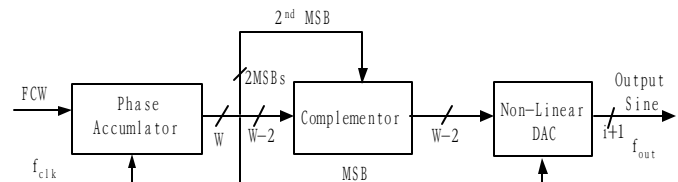


Fig. 1. High-speed DDS with a nonlinear cosine-weighted DAC.

Phase accumulator is the first module in the DDS. The phase accumulator adds the N-bit input frequency control word to itself once every clock cycle. The speed of the phase accumulator depends upon the N bit adder and the flip-flop design. In the proposed architecture, even though the nonlinear DAC operates at 10 GHz, the speed of the DDS is limited by the speed of accumulator. This paper discusses two different architectures for the 8-bit phase accumulator, the pipelined accumulator and the pipelined accumulator with Carry Look Ahead (CLA) adders. The last section of the paper discusses the nonlinear DAC architecture.

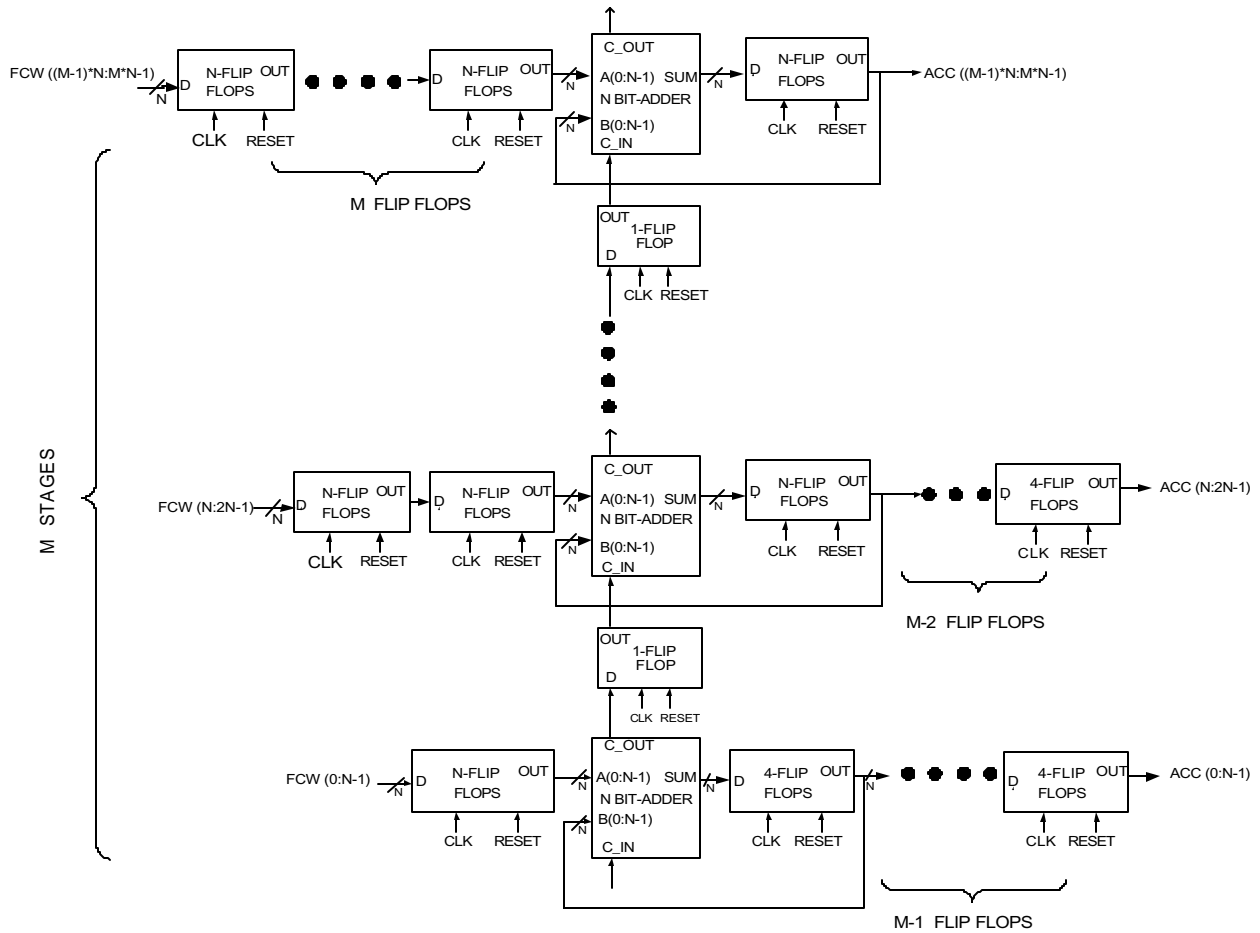


Fig. 2. Generic Architecture of N x M Pipelined Accumulator.

III. PIPELINED ACCUMULATOR

The proposed architecture uses an 8 bit pipelined accumulator. Fig. 2 shows generic architecture of an NxM pipelined accumulator. To realize an 8 bit accumulator we have taken N=1 and M=8. Pipelining enables us to run the NxM bit accumulator at the speed of N bit accumulator. Therefore the 8 bit accumulator runs at the speed of a 1 bit accumulator consisting of a full-adder and a reset flip-flop. Maximum frequency attained by a 1-bit accumulator implemented using CML logic with 400uA tail bias current is about 6.5 GHz. The gate delay to obtain the output includes a delay of the flip-flop and 3-gate delay of the full adder circuit. The accumulator flip-flops are rising-edge triggered master slave flip-flops with reset. The reset is active low asynchronous reset. The accumulator flip-flops are rising edge triggered master slave flip-flops with active low asynchronous reset. For low supply voltage, the reset transistors cannot be vertically stacked at the bottom of the CML circuitry without saturating the latch transistors. It is rather critical for high-speed circuit to keep all the transistors from saturation. We therefore propose a novel reset CML latch circuitry that implements the reset in a parallel structure with only three levels of transistors including the current source transistor as shown in Fig.3. The proposed reset CML flip-flop circuitry is very suitable for low supply voltage

applications. Each CML gate delay is about 45 ps. This architecture has a latency period of about 7 clock cycles.

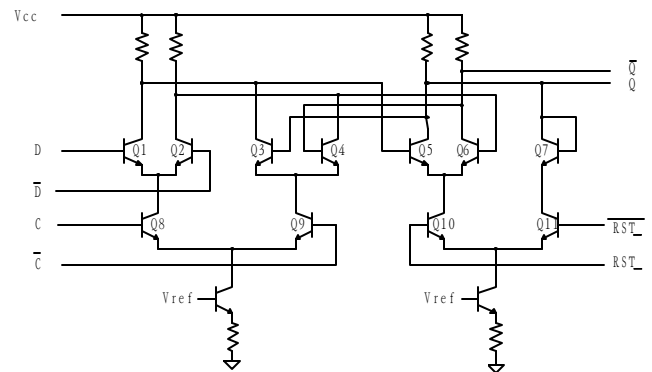


Fig. 3. A novel CML latch with active low reset for low supply voltage applications.

The full adder used in the accumulator architecture is realized using the following equations:

$$CARRY = A \cdot B + B \cdot C + C \cdot A \quad (1)$$

$$SUM = A \oplus B \oplus C \quad (2)$$

Maximum frequency attained by a 1-bit full adder is about 10GHz. All the gates used to realize the full adder are two input

gates. Hence the maximum delay to obtain the carry in a full adder is 3 gate delays. A fully pipelined 8-bit accumulator contains about 210 gates and consumes about 150mA. The simulated output of the 8-bit accumulator operating at 6.5GHz clock frequency is shown in Fig. 4. The number of clock cycles till the vertical line in the Fig. 4 indicates the latency period.

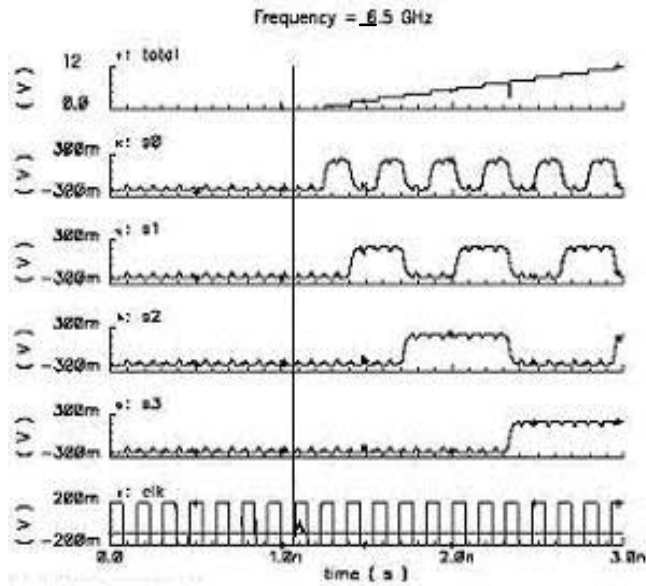


Fig. 4 Output waveform of an 8-bit fully pipelined adder.

IV. ACCUMULATOR WITH CARRY LOOK AHEAD ADDERS

The proposed DDS architecture can incorporate various modulation schemes as shown in Fig. 5. The DDS modulation waveform configurations include chirp, step frequency, FM, MSK, PM, AM, QAM, and other hybrid modulations. To allow DDS to operate with modulations, the developed pipelined accumulator needs to be modified to allow variable frequency control words (FCW) as its inputs. In chirp or step frequency modulation the FCW input of the DDS changes continuously. To incorporate frequency modulation techniques in DDS, the latency period has to be reduced.

The 8 bit pipelined accumulator architecture has a large latency period of 7 clock cycles. This latency can be reduced to 1 clock cycle using a 8 bit accumulator with two 4-bit CLA adders (N=4 and M=2). The latency can be reduced to zero using an 8-bit CLA adder with (N=8 and M=1). However, the architectures suffer a considerable reduction in speed.

The maximum speed attained by N=4 and M=2 pipelined accumulator with CLA adders is same as the maximum speed attained by a 4-bit accumulator, which runs at maximum speed of 3.5 GHz. The speed of the 4-bit accumulator depends upon the speed of the 4-bit CLA adder and the reset flip-flops. All the gates used are two input gates. The basic building blocks in the adder circuit are NAND gate and EXOR gate. Any other logic gates such as NOR gate, AND gate and OR gate can be realized from NAND and XOR gates.

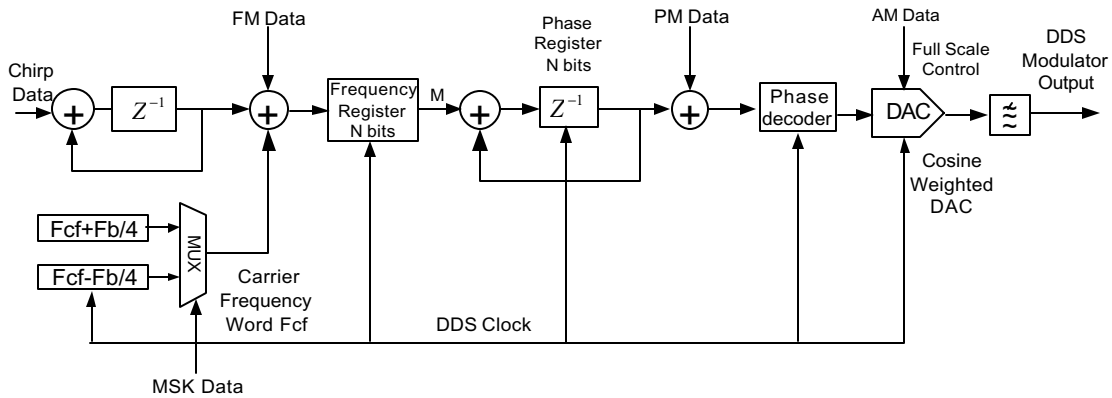


Fig. 5. DDS incorporated with various modulation schemes.

Differential topology has been used to build the basic building blocks for the improvement of noise characteristics. SiGe npn transistors with an emitter length of 1um have been used. The power dissipation per gate is about 1.32mw. The total delay to obtain the output sum and carry is 6-gate delay for a 4-bit CLA adder, while the delay in a fully pipelined architecture is 3-gate delay. The generation of carries in the CLA can be summarized as:

$$C1 = g_0 + p_0 \cdot c_0 \quad (3)$$

$$C2 = (g_1 + p_1 \cdot g_0) + (p_1 \cdot p_0 \cdot c_0) \quad (4)$$

$$C3 = (g_2 + p_2 \cdot g_1) + (p_2 \cdot p_1 \cdot g_0) + p_2 \cdot (p_1 \cdot p_0 \cdot c_0) \quad (5)$$

$$C4 = (g_3 + p_3 \cdot g_2) + (p_3 \cdot p_2 \cdot g_1) + p_3 \cdot (p_2 \cdot p_1 \cdot g_0) + (p_3 \cdot p_2 \cdot p_1 \cdot p_0 \cdot c_0) \quad (6)$$

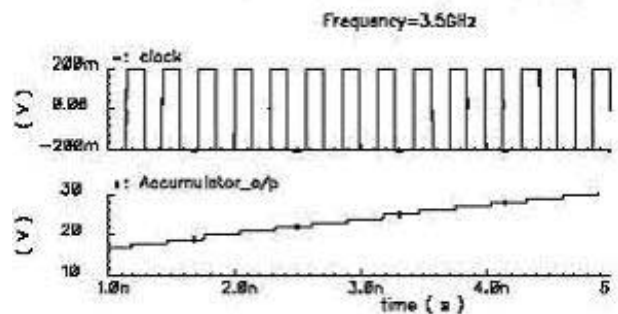


Fig. 6. Simulated output of an 8 bit pipelined accumulator with CLA adders (N=4 and M=2) operating at 3.5 GHz clock frequency.

where $g_n = A_n \cdot B_n$ is the carry generator and $P_n = A_n \oplus B_n$ is the carry propagate to calculate $(n+1)$ th carry.

V. COSINE WEIGHTED DIGITAL TO ANALOG CONVERTER

The high-speed DDS utilizes a cosine-weighted DAC operating in current mode, which does not require op-amp buffer at the output and its speed would not be limited by the bandwidth of the op-amp. The DAC contains a current-cell matrix as shown in Fig. 7. Each DAC cell outputs a current proportional to cosine value of the corresponding phase indicated by the $a+b$ bits. The sinusoidal output is obtained by summing the output currents from all the cells through an external pull-up resistor. We used npn transistors with minimum emitter length of 1um to switch the current cells. The transistors are biased at 400uA that is slightly smaller than their peak f_T current. The 8bit DAC output current thus varies from a minimum of 400uA to maximum of 102.4mA. The bias current is carefully chosen considering the speed, power consumption and DAC output full scale voltage swings. The accuracy of the bias current is ensured using an optimized band-gap reference design with calibrating capability. Dynamic performance of the DDS rapidly degrades with frequency due to transient glitches in the DAC. These glitches can be minimized by using thermometer decoding scheme that ensures the minimum number of cells switching simultaneously. In addition, all switching control signals are buffered to ensure differential synchronous switching for all cells. The 8-bit nonlinear DAC with the column and row decoders can operate beyond 10GHz clock frequency.

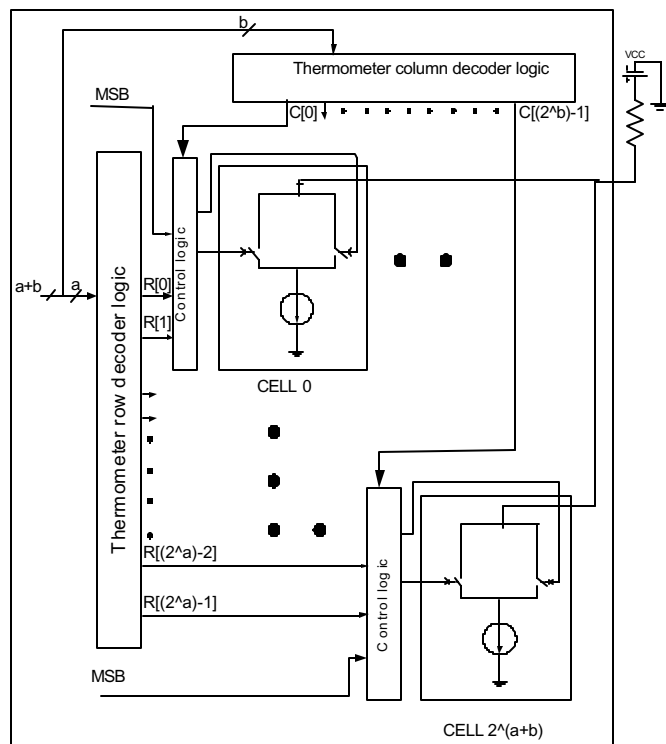


Fig. 7. Nonlinear DAC with current cells.

The DAC control logic is shown in Fig. 8, where the signal MSB represents the MSB bit of the phase accumulator output. Signals A and B are differential pair signals which control the current switches in the DAC cell. Fig. 9 gives the simulated DDS output waveform at 2.5GHz after the deglitch filter.

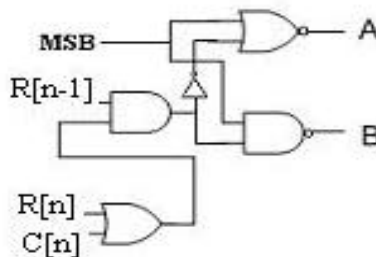


Fig. 8. Control logic of the n th DAC cell.

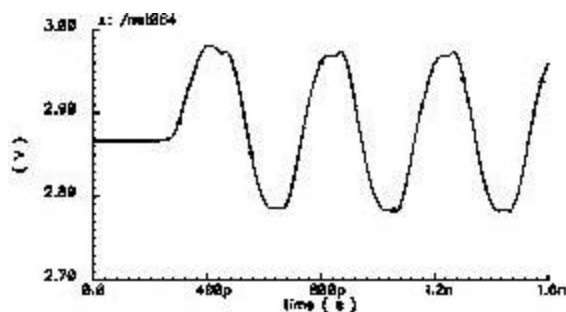


Fig. 9. Simulated DDS output at 2.5GHz after the deglitch filter.

VI. CONCLUSIONS

We have designed a low power 5GHz high-speed DDS with a cosine weighted DAC in SiGe technology. The simulated DDS power consumption is less than 2 W, which is much smaller than a prior art DDS MMIC implemented in an InP technology. Novel CML circuits have been developed for low power high-speed applications. The simulated DDS circuitry can operate up to 5 GHz with output frequency at L band. The designed DDS MMIC is to be fabricated in a 47GHz SiGe technology.

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