

DELAY ANALYSIS AND OPTIMAL BIASING FOR HIGH SPEED LOW POWER CURRENT MODE LOGIC CIRCUITS

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ABSTRACT

This paper presents a delay analysis for Current Mode Logic (CML) circuits operating at the GHz range. The optimal biasing for CML circuits is obtained considering the circuit speed and power consumption. We propose and analyze a novel “keep alive” CML circuit that biases the upper level transistors at the slightly higher current than the lower level transistors. A speed improvement of about 11% at low bias range is demonstrated using the proposed biasing scheme.

1. INTRODUCTION

In recent years, modern communication systems demand for high performance circuits has increased. Apart from required high frequency of operation, low power consumption has become an important feature for wireless communication systems. In the design of these high performance circuits, series gated two-level transistor topologies such as current mode logic (CML) and emitter-coupled logic (ECL) are typically used. A novel biasing strategy called “Keep Alive” for CML topology is proposed to achieve improved performance in terms of speed when the circuit is biased at 10% to 30% of the peak f_T current. The proposed biasing scheme utilizes a regular bias that supports the normal CML operation and a small “keep alive” bias that keeps the upper level transistors in “ON” states for speed improvement.

The maximum speed of these circuits is limited by the RC open circuit time constants of the series gated latches and gates. It is therefore imperative to conduct a detailed study of delay through CML topology and develop techniques to extract its maximum performance. There are a few propagation delay models available in literature [2][3][4]. The model presented in [2] is derived using sensitivity analysis and the model presented in [4] is based on linearization of the device which are complex for use during pencil and paper design. We have used the model presented in [3] to evaluate the performance of

CML gate with “Keep Alive biasing” where the delay has been expressed as sum of RC time constants derived from the small signal model of the gate. While CMOS logic circuit still tends to dominate the field of digital integrated circuits, it is not suitable for high speed designs as the turn-on and turn-off times limit its maximum operation speed. Since the rail-to-rail CMOS voltage swing is large (from zero to V_{DD}), the time taken to charge and discharge capacitors is also large. Moreover, the rate of charge and discharge of capacitors in CMOS circuits is not constant. The power consumption of CMOS circuits increases with frequency. The digital switching noise associated with the CMOS logic circuit is also much larger than CML circuits that use constant current sources. A better option for high-speed circuit designs would be to use CML or ECL topologies. The main advantages of CML logic lie on its high operation speed, its constant power consumption independent of operation frequency. The CML voltage swing is small, suitable for high-speed and low noise applications. Since its operation is normally differential, CML circuits generate less noise and result in lower dynamic power dissipation. However the main disadvantage of CML circuits is the static power dissipation. ECL gates consist of differential amplifier, temperature and voltage compensated bias network, emitter follower output. The operation of ECL circuits is similar to that of CML circuits. The power consumption in ECL is larger than that of CML due to the presence of emitter followers at the input and output.

In this paper, we will focus on delay analysis and optimization of CML circuits for high-speed and low power applications.

2. SERIES GATED CURRENT MODE LOGIC

In this section, we model the delay time constants of a series gated CML D-latch, which is the common basic building block of many switching circuits. Figure 1a and figure 1b illustrate the circuit schematics of the D-latch and its small-signal (half-circuit) model. For worst-case propagation delay we set the upper level data inputs as

constant and provide a step input at lower level clock transistors[2][3]. The analysis of the half circuit is sufficient for differential operations.

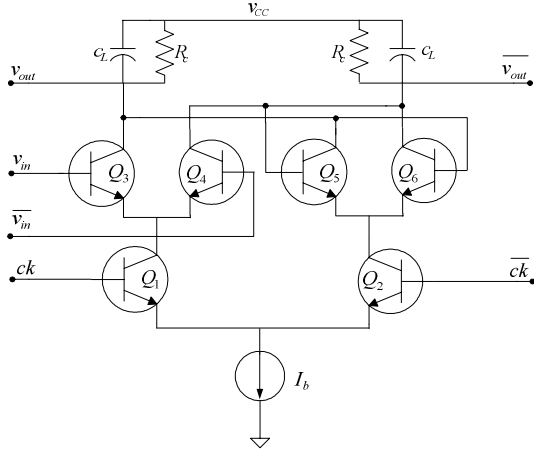


Fig. 1a. Schematic diagram of CML D-Latch.

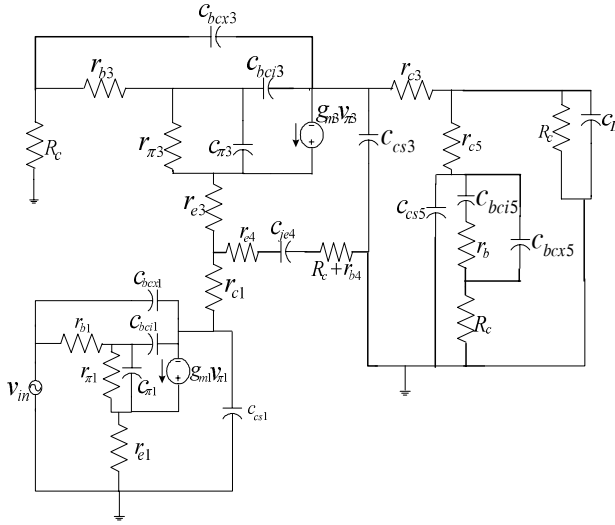


Fig. 1b. Small signal half circuit model of CML D-Latch.

The above figure is the small signal half circuit model of the CML D-Latch and the delay through the gate can be expressed as the sum of RC time constants, assuming dominant pole behavior[3]. The time constant associated with various capacitors can be derived from the equivalent circuit model shown in Fig. 1b. The time constants for lower transistors are given as

$$\tau_{\pi} = \frac{r_{el} + r_{bl}}{1 + g_{ml}r_{el} + \frac{r_{el} + r_{bl}}{r_{\pi}}} C_{\pi} \quad (1a)$$

$$\tau_{bcxl} = \left(r_{cl} + r_{eu} + \frac{r_{\mu} + r_{bu} + R_c}{\beta + 1} \right) C_{bcxl} \quad (1b)$$

$$\tau_{bcil} = \left[\left(r_{cl} + r_{eu} + \frac{r_{\mu} + r_{bu} + R_c}{\beta + 1} \right) + r_{bl} \left(1 + \frac{g_{ml} \left(r_{cl} + r_{eu} + \frac{r_{\mu} + r_{bu} + R_c}{\beta + 1} + r_{el} \right)}{1 + g_{ml}r_{el}} \right) \right] \cdot C_{bcil} \quad (1c)$$

$$\tau_{csl} = \left(r_{cl} + r_{eu} + \frac{r_{\mu} + r_{bu} + R_c}{\beta + 1} \right) \cdot C_{csl} \quad (1d)$$

The time constants for upper transistors are listed as

$$\tau_{\pi 3} = \frac{1}{\left(g_{m3} + \frac{1}{r_{\pi 3}} \right)} \cdot C_{\pi 3} \quad (2a)$$

$$\tau_{bc3} = (2R_c + r_{cu} + r_{bu}) \cdot C_{bc3} \quad (2b)$$

$$\tau_{bcx3} = (2R_c + r_{cu}) \cdot C_{bcx3} \quad (2c)$$

$$\tau_{bc5} = (2R_c + r_{cu} + r_{bu}) \cdot C_{bc5} \quad (2d)$$

$$\tau_{bcx5} = (2R_c + r_{cu}) \cdot C_{bcx5} \quad (2e)$$

$$\tau_{cs3} = (R_c + r_{cu}) \cdot C_{cs3} \quad (2f)$$

$$\tau_{cs5} = (R_c + r_{cu}) \cdot C_{cs5} \quad (2g)$$

$$\tau_{je4} = (R_c + r_{bu} + 2r_{eu}) \cdot C_{je4} \quad (2h)$$

$$\tau_{load} = R_c \cdot C_{load} \quad (2i)$$

where subscripts "u" and "l" denote upper and lower transistors and "c", "b", "e" and "s" means collect, base, emitter and substrate of the corresponding transistors, "π" denotes base-emitter junction, respectively. The delays associated with upper and lower transistors can be found out by summing all the delays in Eq. (1) and Eq.(2), respectively:

$$t_{lower} = \tau_{\pi} + \tau_{bcil} + \tau_{bc1} + \tau_{csl} \quad (3a)$$

$$t_{upper} = \tau_{\pi 3} + \tau_{bc3} + \tau_{bcx3} + \tau_{bc5} + \tau_{bcx5} + \tau_{cs3} + \tau_{cs5} + \tau_{je4} + \tau_{load} \quad (3b)$$

$$t_{total} = 0.69 \times (t_{lower} + t_{upper}) \quad (3c)$$

At the junction where voltages change rapidly by a large amount, those junction capacitances are modified from zero bias values by using coefficient K given by [1]

$$K = \left(\frac{\phi^m}{V_2 - V_1} \right) \left[\frac{(\phi - V_1)^{1-m}}{1-m} - \frac{(\phi - V_2)^{1-m}}{1-m} \right] \quad (4)$$

where ac voltage swing of $\pm 150mV_{pp}$ is considered.

The capacitances used in Eq. (1) and (2) are assumed to be constants when bias current varies, which is a good approximation at low bias current. At high bias current, this assumption results in about 10% discrepancy between the analytical model and the Cadence SPICE simulation.

3. OPTIMUM BIASING FOR CML CIRCUITS

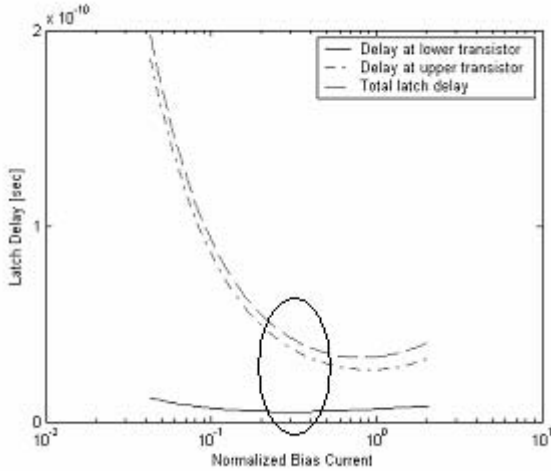


Fig. 2. CML D-Latch delay versus normalized bias current.

Fig.2 plots the gate propagation delay with respect to the bias current normalized to the peak f_T current using equations 3a,3b,3c. It comes as no surprise that the optimum biasing current to provide minimum delay is indeed the transistor peak f_T current.

According to Fig.2, it is obvious that there is not much speed improvement obtained by increasing the biasing current beyond 60% of the peak f_T current[3]. This fact has not been well adopted in the practical CML circuit designs. In fact, a lot of published CML circuits employed bias schemes that were more than 60% of the peak f_T current and the speed improvements were not very evident. Biasing the circuit close to the peak f_T current may cause the actual bias current go beyond the peak f_T current under temperature, supply and process variations, which leads to dramatic speed penalty as the result of current crowding and the conductivity modulation effects in the base region. Unless absolutely high speed of operation is required, it is a good practice, to bias the CML circuit with smaller than 60% of the peak f_T current to save unnecessary power consumption. Figure 2 shows that biasing the CML circuits at 40% of the peak f_T current (the circled region in the figure) can achieve about 80% of the maximum speed that corresponds to the peak f_T current. Also it can be seen from the figure that the optimum bias current to give minimum delay is not the same for both upper and lower level transistors. The lower transistors have minimum delay at a lower bias current than the upper transistors. This is evident from the fact that the upper transistors have more

time constants associated with it. Next, we will present a novel CML biasing technique. The proposed biasing scheme utilizes a regular bias that supports the normal CML operation and a small “keep alive” bias that keeps the upper level transistors in “ON” states for speed improvement when the circuit is biased at 10-30% of peak f_T current (the circled region in Fig.2)

4. “KEEP ALIVE” BIASING TECHNIQUE

The delay model developed in the previous sections can be used to optimize CML circuit to further improve circuit performance in terms of power consumption and speed.

A dependence of CML latch delays on bias current is illustrated in Fig. 3. It’s evident that the CML latch delay is dominated by the delay associated with the upper transistors. Note that the delay contributed by the upper level transistors decreases much faster than that contributed by the lower level transistors when the biasing current increases. In other words, increasing biasing current can dramatically reduce the delay at upper level transistors, yet not much effect for the delay at lower level transistors. Hence, reducing the delay due to upper level transistors is critical to improve CML switching speed.

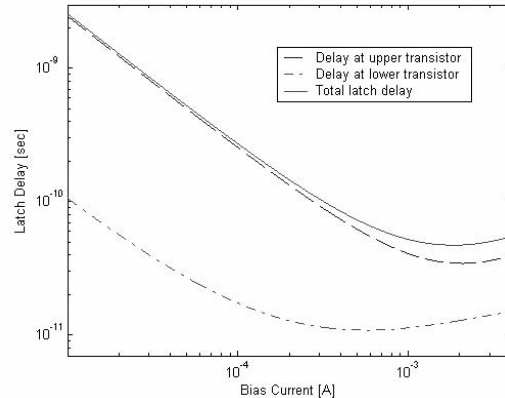


Fig. 3. CML latch delays versus bias current.

Based on the previous discussion, it’s intuitive that there will be a speed improvement if we bias the circuit in a manner such that after the clock signal arrives, the upper level transistors have slightly higher bias currents than the lower level transistors. The total bias current remains the same. The only difference from conventional CML biasing arrangement is that we are splitting the biasing currents such that the upper level transistors are biased at slightly higher current than the lower level ones. For instance, we may reduce the bias currents by about 20% for the lower level clock transistors and supply the extra current to the upper level data transistors. Fig. 4 shows a D-flip flop biased in such a manner. This biasing technique is named as “keep alive”, since there will always be a small amount

of bias current flowing through the upper level transistors, keeping them alive in slightly “turn-ON” states regardless of the clock and data. The main advantage of this type of biasing arrangement is that the data transistors are always slightly “ON” independent of clock signal. As a result, the capacitors associated with the upper level transistors, which are the dominant contributors to the CML propagation delay, will be charged to a certain level. When the clock signal arrives, it takes relatively less time for the capacitors to reach their steady state values. Moreover, optimization can also be performed in terms of transistor sizing for upper and lower transistors.

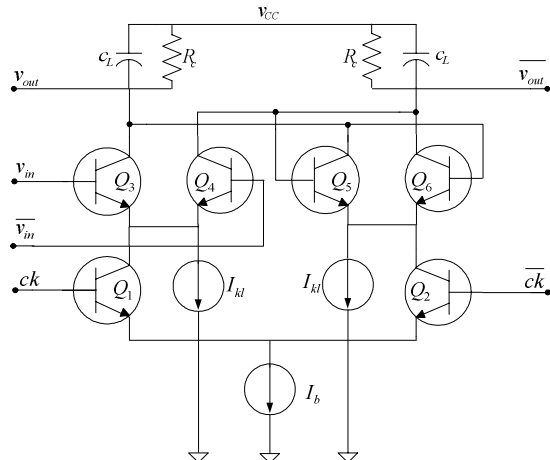


Fig. 4. “Keep alive” biasing technique for CML D-Latch.

5. SIMULATION RESULTS

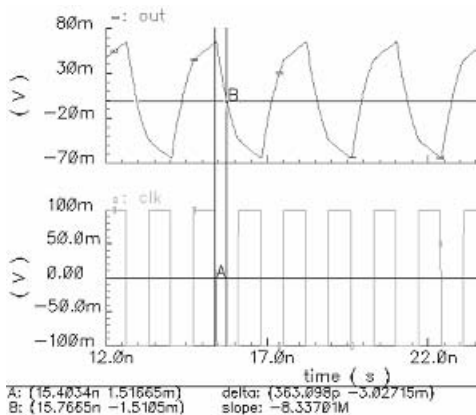


Fig. 5a. Propagation delay without “keep alive” biasing in a divided by two circuit.

We have implemented the CML circuits with the proposed “keep alive” biasing scheme in a 47GHz SiGe technology. A divided by two circuit is chosen to test the performance of the proposed CML D-latch. The propagation delay through a divide by two circuit without a “keep alive” is about 363ps, as shown in the Fig. 5a, and the propagation delay through the circuit with a “keep

alive” is about 313ps, as shown in Fig. 5b. Hence, a speed improvement of about 11% is achieved by using the proposed “keep alive” biasing scheme. The D-latch delay of 363ps is relatively large for bipolar CML circuit due to our low biasing current. The proposed “keep alive” biasing scheme does not increase the power consumption, yet the output noise margin (swing) is slightly reduced, i.e., we trade noise margin for circuit speed.

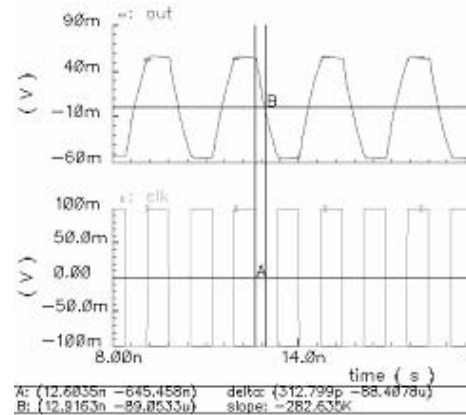


Fig. 5b. Propagation delay with “keep alive” biasing in the divided by two circuit.

6. CONCLUSION

The delay of a CML circuit is modeled in terms of its delay elements such as transistor junction capacitances. The contribution of these individual delay elements to the final propagation delay is analyzed to explore circuit and device optimization. Also studied are an optimal biasing and a novel “keep alive” biasing for CML circuits for high-speed and low power applications. The proposed biasing scheme increases the CML operation frequency without any extra power consumption.

7. REFERENCES

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