Process-Variation-Resistant Dynamic Power Optimization for VLSI Circuits

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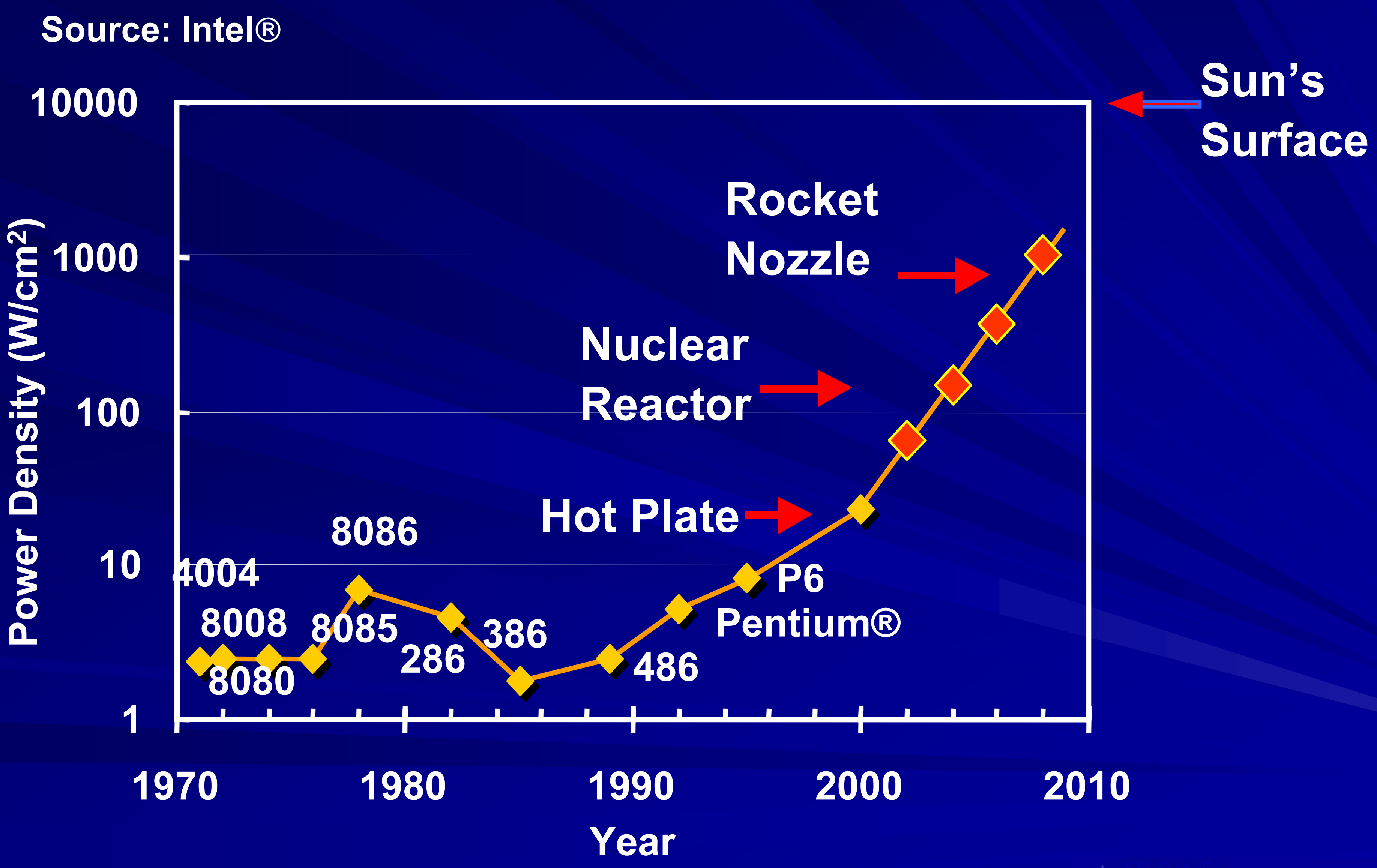
Outline

- Introduction
- Background
  - Dynamic power dissipation
  - Glitch reduction
  - Previous LP model
- Process-variation-resistant LP model
  - Process variation
  - Delay model
  - LP model based on worst-case timing
  - LP model based on statistical timing
- Input-specific optimization
  - Without process-variation
  - With process-variation
- Experimental results
- Conclusion

Introduction

- Power component for CMOS circuits
  - $P_{avg} = P_{static} + P_{dynamic}$
  - $P_{dynamic} \approx 1/2\, kC_L V_{dd}^2 f_{clk}$
- Power dissipation problem
  - For constant die size, total capacitance increases by 40% when transistor size is reduced by 70%
  - Clock frequency is scaled up faster than the minimum feature size (MFS)
  - Leakage power increases dramatically as MFS reduces into submicron region
  - Architecture trend is towards programmability and reusability – leads to more hunger for power

VLSI Chip Power Density



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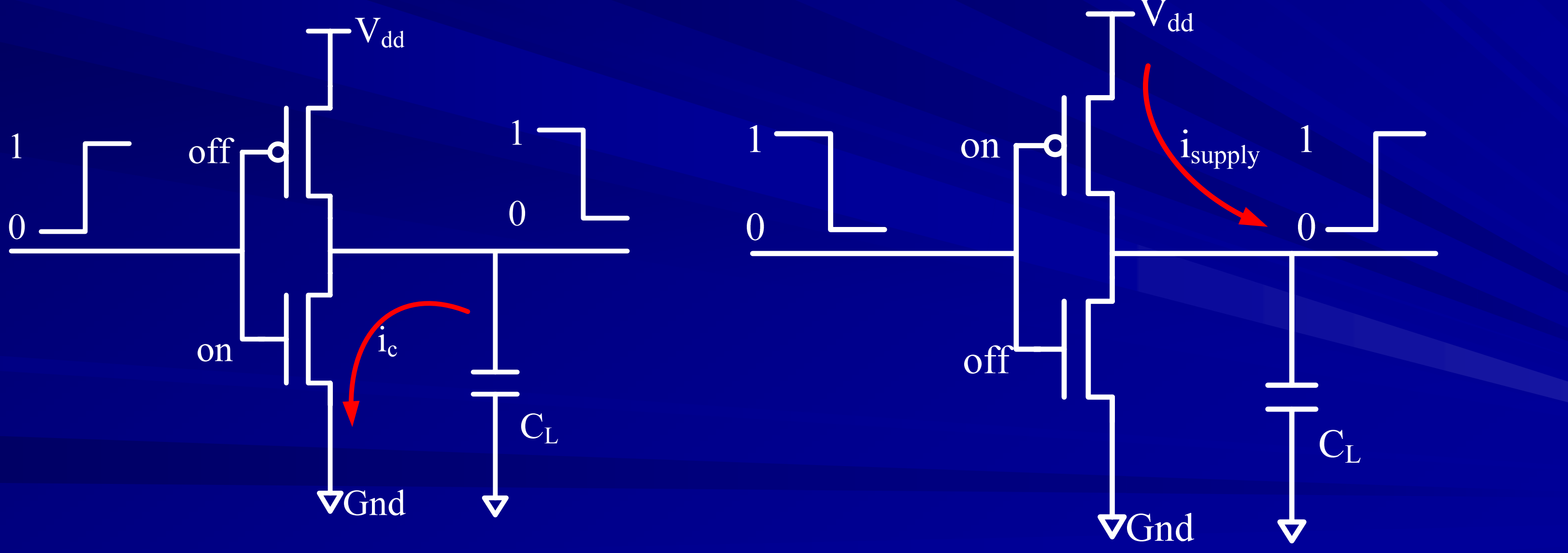
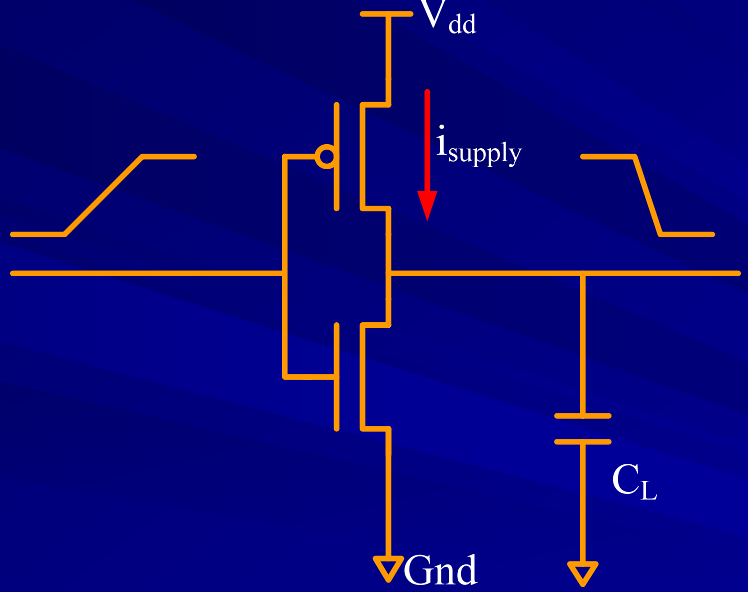
Background

- Dynamic power dissipation
  - $P_{dyn} = P_{switching} + P_{short\text{-}circuit}$
- Switching power dissipation
  - $P_{switching} = 1/2\ kC_L V_{dd}^2 f_{clk}$



Background

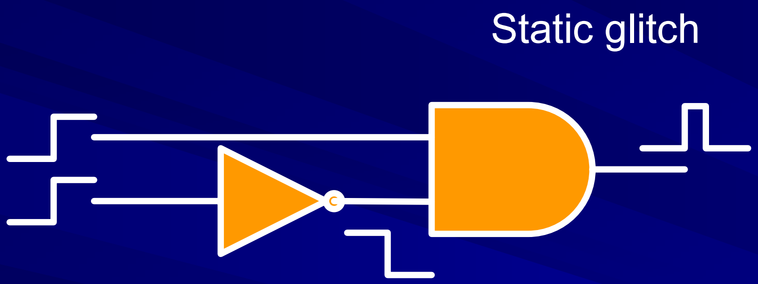
- Short-circuit power dissipation
  - Short-circuit current when both PMOS and NMOS are on
  - Very much affected by the rising and falling times of input signals

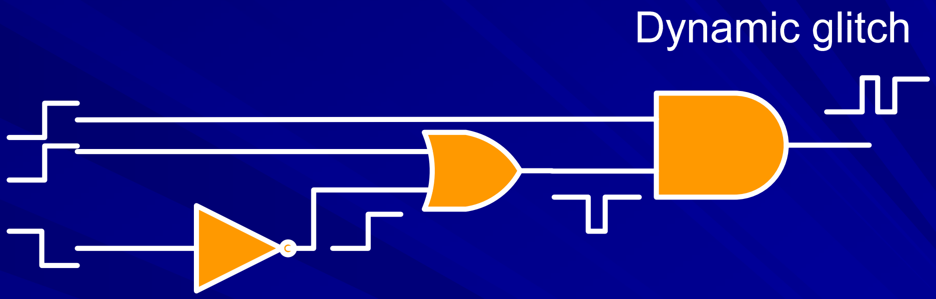


    - significant when input rise/fall time much longer than the output rise/fall time
  - Can be kept to a insignificant portion of P_{dyn}

Background

- Glitch reduction
  - A important dynamic power reduction technique

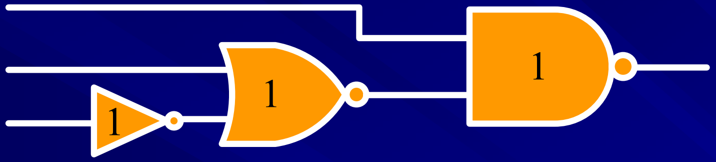




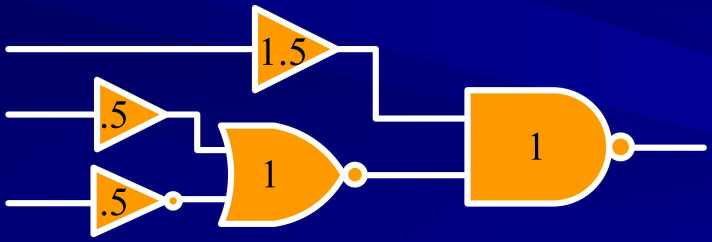
  - Glitch power consumes 30~70% P_{dyn} for typical circuits
  - Related techniques
    - Balanced delay
    - Hazard filtering
    - Transistor/Gate sizing
    - Linear Programming approach

Glitch reduction

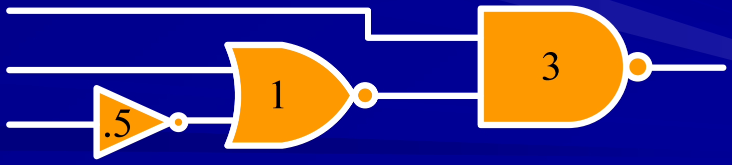
- Original circuit



- Balanced path/ path balancing
  - Equalize delays of all path incident on a gate
  - Balancing requires insertion of delay buffers.



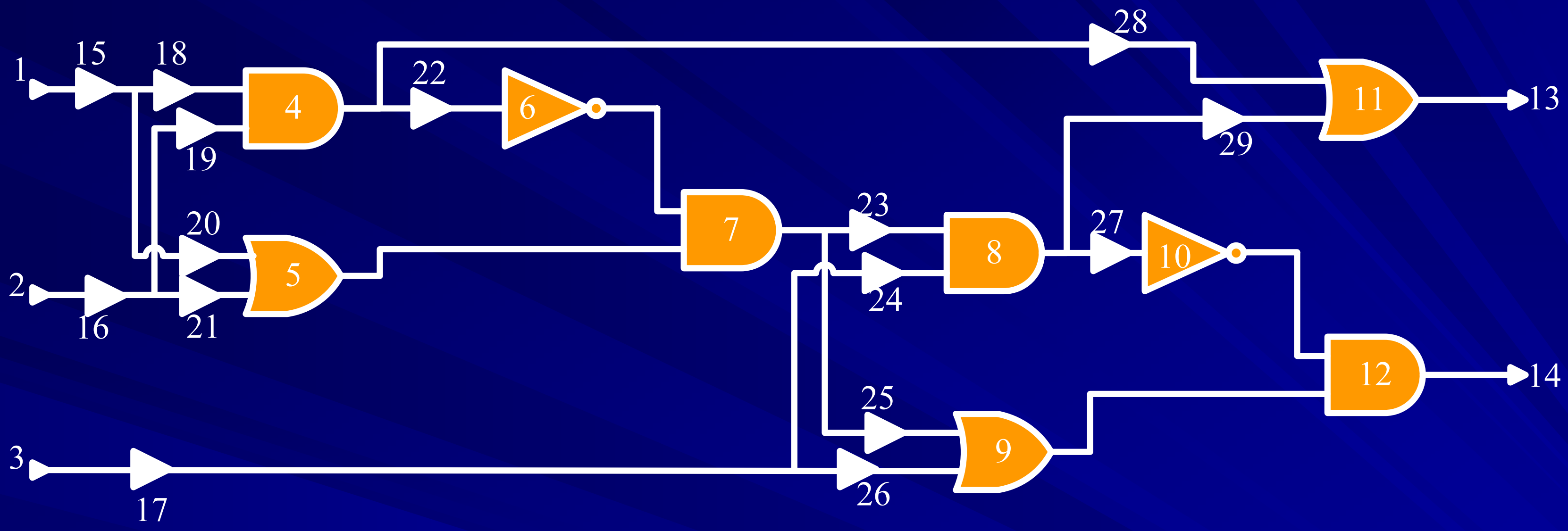
- Hazard/glitch filtering
  - Utilize glitch filtering effect of gate
  - Not necessary to insert buffer



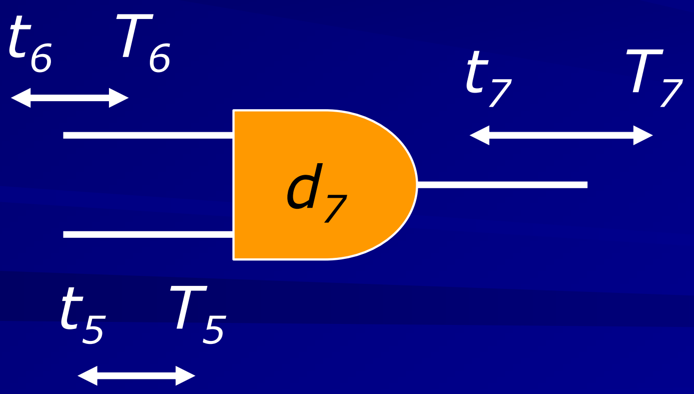
Glitch reduction

- Transistor/gate sizing
  - Find transistor sizes in the circuit to realize the delay
  - No need to insert buffer
  - Suffers from nonlinearity of delay model
  - large solution space, numeric convergence and global optimization not guaranteed
- Linear programming approach
  - Adopt both path balancing and hazard filtering
  - Find the optimal delay assignments of gates
  - Use technology mappings to map the gate delay assignments to transistor/gate dimensions.
  - Guaranteed optimal solution, a convenient way to solve a large scale optimization problem

Previous LP approach



Timing window *(t, T)*



Gate constraints:

$T_7 \geq T_5 + d_7$

$T_7 \geq T_6 + d_7$

$t_7 \leq t_5 + d_7$

$t_7 \leq t_6 + d_7$

$d_7 > T_7 - t_7$

Circuit delay constraints:

$T_{11} \leq maxdelay$

$T_{12} \leq maxdelay$

Objective:

Minimize sum of buffer delays

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Process-variation-resistant optimization

- Motivation
  - Gate delay assumed fixed in previous models
  - Variation of gate delay in real circuits
    - Environmental factors: temperature, V_{dd}
    - Physical factors: process variations
  - Effect of delay variation
    - Glitch filtering conditions corrupted
    - Power dissipation increases from the optimized value
    - Leakage variation possible, requires separate investigation
  - Our proposal
    - Consider delay variations in dynamic power optimization
    - Only consider process variations (major source of delay variation)

Process and delay variations

- Process variations
  - Variations due to semiconductor process
    - V_T, t_{ox}, L_{eff}, W_{wire}, TH_{wire}, etc.
  - Inter-die variation
    - Constant within a die, vary from one die to another die of a wafer or wafer lot
  - Intra-die variation
    - Variation within a die
    - Due to equipment limitations or statistical effects in the fabrication process, e.g., variation in doping concentration
    - Spatial correlations and deterministic variation due to CMP and optical proximity effect

Process and delay variations

- Delay variation
  - First order gate delay model

$$T_d = \frac{C_L \times V_{dd}}{I} = \frac{C_L \times V_{dd}}{\frac{\mu C_{ox}(W/L)}{2}(V_{dd} - V_t)^2}$$

  - Gate delay sensitive to process-variations
- Related previous work
  - Static timing analysis
    - Worst case timing analysis
    - Statistical timing analysis
  - Power optimization under process-variations
    - Voltage scaling, multi-V_{dd}/V_{th} considering critical delay variations
    - Gate sizing using statistical delay model
    - No work on glitch power optimization

Delay model and implications

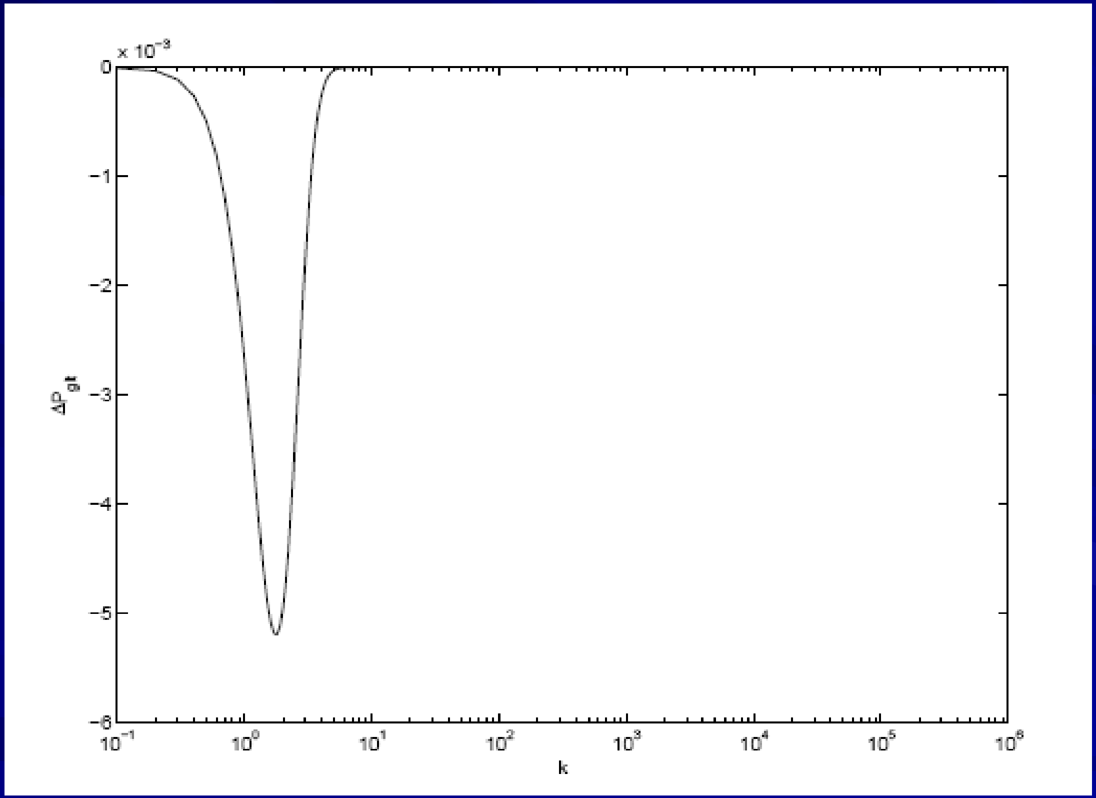
- Random gate delay model
  - $D_{total,i} = D_{nom,i} + \Delta D_{inter,i} + \Delta D_{intra,i}$
  - Truncated normal distribution
  - Assume independence
  - Variation in terms of $\sigma/D_{nom,i}$ ratio
- Effect of inter-die variations
  - Depends on its effect to switching activities
  - Definition of glitch-filtering probability $P_{glt} = P\{t_2 - t_1 < d\}$
    - Signal arrival time t_1, t_2
    - Gate inertial delay d
  - Theorem 1 states the change of P_{glt} due to inter-die variation

$$\Delta P_{glt} = \frac{1}{2}\left(\operatorname{erf}\left(\frac{-k}{\sqrt{2}}\right) - \operatorname{erf}\left(\frac{-k}{\sqrt{2+2(r \cdot k)^2}}\right) \right)$$

    - *erf()*, the error function
    - *k*, a path and gate dependent constant
    - *r*, $\sigma/D_{nom,i}$ ratio for inter-die variations

Delay model and implications

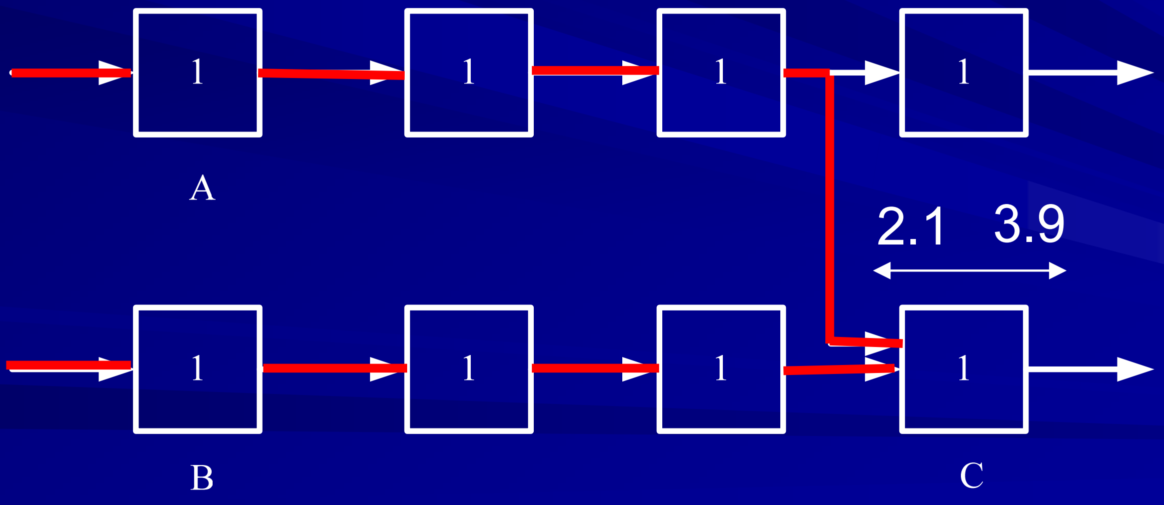
- Effect of inter-die variations
  - For a large inter-die variation, r = 0.15, $|\Delta P_{glt}| < 5.3 \times 10^{-3}$



  - Negligible effect on switching activity

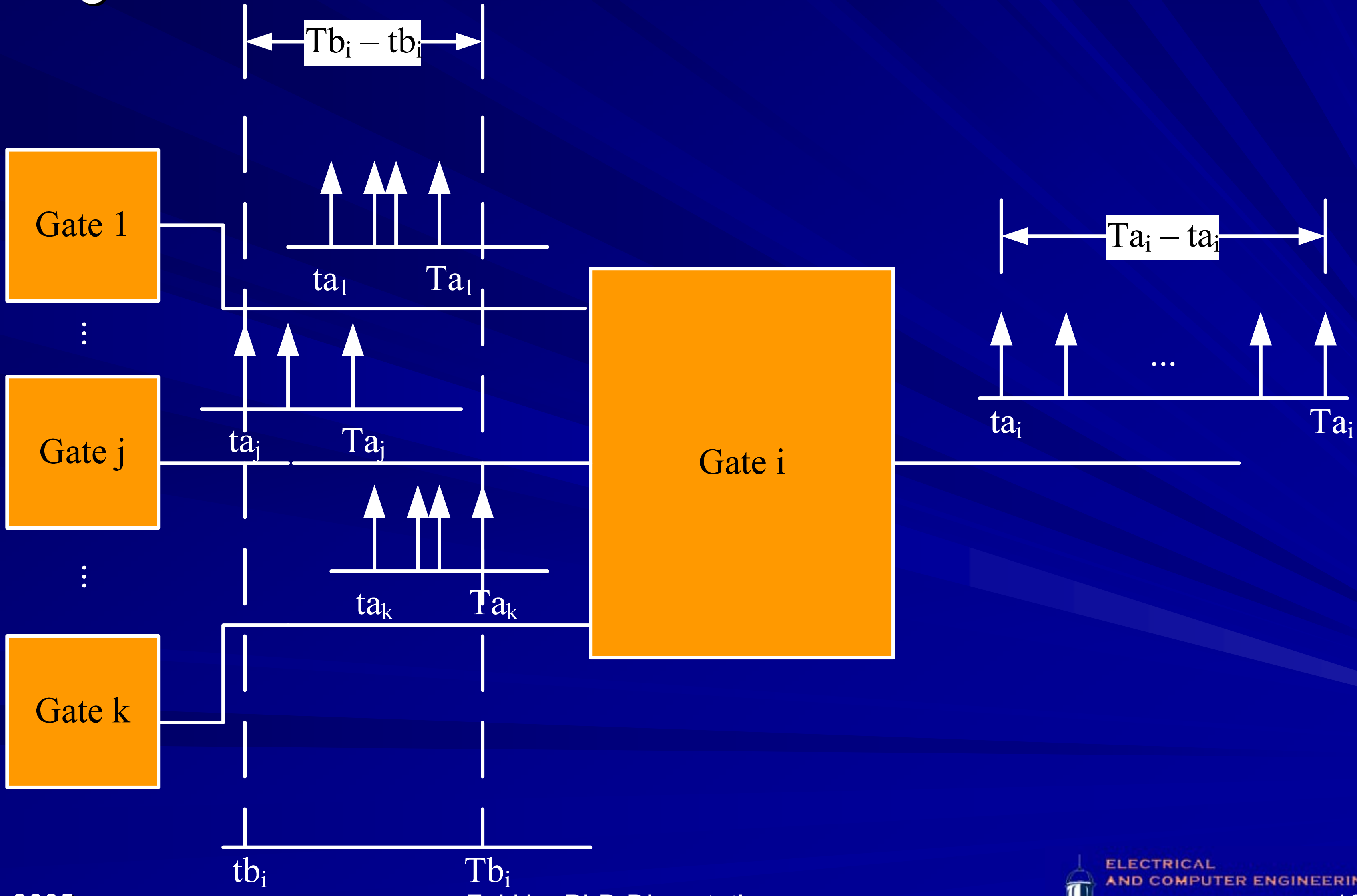
Delay model and implications

- Process-variation-resistant design
  - Can be achieved by path balancing and glitch filtering
  - Critical delay may increase
    - Theorem 2 states that a solution is guaranteed only if circuit delay is allowed to increase
    - Proved by example, assuming 10% variation



LP model based on worst-case timing

- Timing model



LP model based on worst-case timing

- Constraints
  - Gate constraints

$$Tb_i \geq Ta_1; \qquad tb_i \leq ta_1;$$

$$Tb_i \geq Ta_j; \qquad tb_i \leq ta_j; \qquad Ta_i = Tb_i + d_i \cdot (1 + 3r);$$

$$Tb_i \geq Ta_k; \qquad tb_i \leq ta_k; \qquad ta_i = tb_i + d_i \cdot (1 - 3r);$$

  - Glitch filtering constraints

$$Tb_i - tb_i < d_i \cdot (1 - 3r) \cdot \alpha \qquad \text{where } r < 0.33 \ (33\%)$$

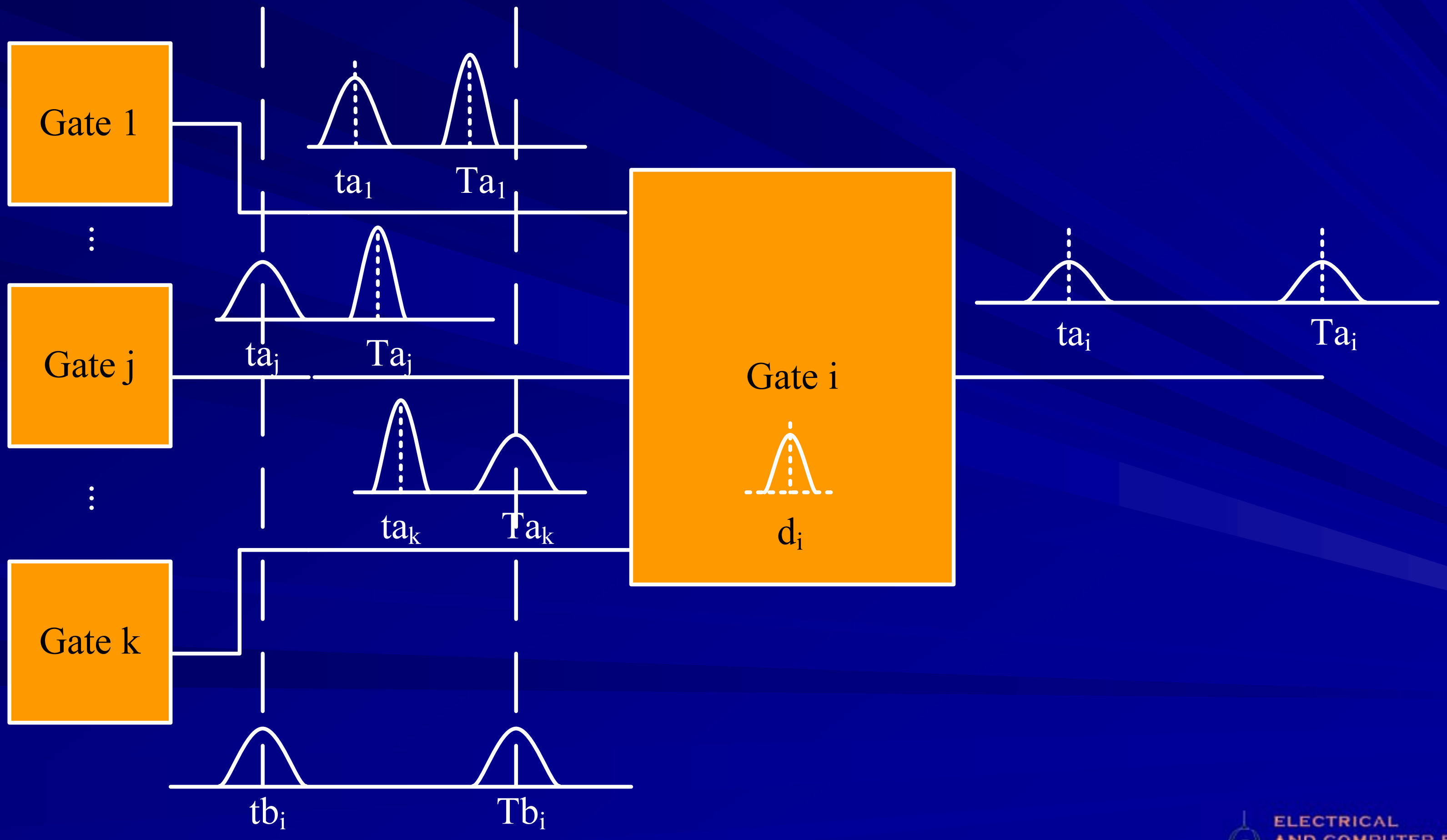
  - Delay constraints for POs

$$Ta_i \leq D_{max}$$

- Parameter
  - r, $\sigma / D_{nom,i}$ ratio
  - D_{max}, circuit delay parameter
  - α, optimism factor $\in$ [1,∞]; 1 ≡ all glitches filtered, ∞ ≡ no glitch filtered
- Objective
  - Minimize #buffer inserted – sum of buffer delays

LP model based on statistical timing

- Worst-case timing tends to be too pessimistic
- Statistical timing model with random variables



LP model based on statistical timing

- Minimum-maximum statistics
  - needed for tb_i, Tb_i

$$tb_i = \mathrm{Min}(ta_1, ta_j, ta_k);$$

$$Tb_i = \mathrm{Max}(Ta_1, Ta_j, Ta_k);$$

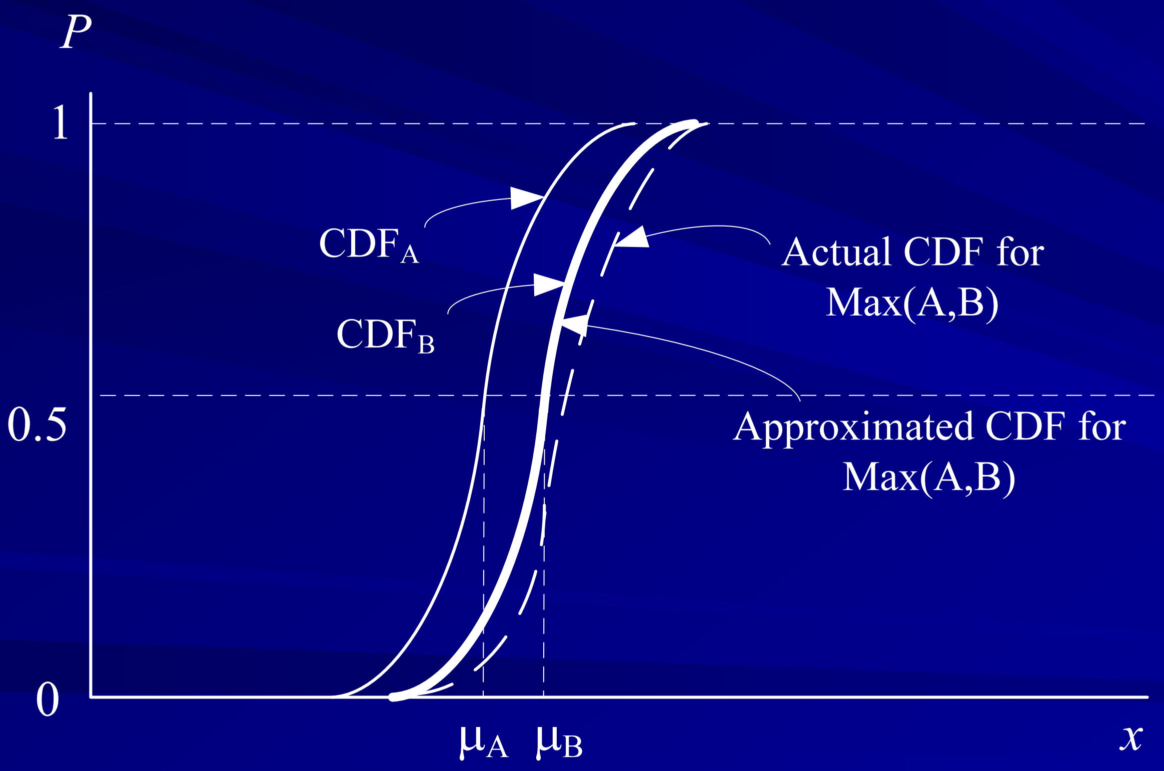
  - Previous works
    - Min, Max for two normal random variable not necessarily distributed as normal
    - Can be approximated with a normal distribution
    - Requiring complex operations, e.g., integration, exponentiation, etc.
  - Challenges for LP approach
    - Require simple approximation w/o nonlinear operations
    - Our approximation for *C*=Max(*A*,*B*), A, B, and C are Gaussian RVs

$$\mu_C = \mathrm{Max}(\mu_A, \mu_B)$$

$$\mu_C + 3\sigma_C = \mathrm{Max}(\mu_A + 3\sigma_A, \mu_B + 3\sigma_B)$$

LP model based on statistical timing

- Min-Max statistics approximation error
  - Negligible when $|\mu_A - \mu_B| > 3(\sigma_A + \sigma_B)$
  - Largest when $\mu_A = \mu_B$



$$\mu_C = \mathrm{Max}(\mu_A, \mu_B)$$

$$\sigma_C = \frac{1}{3}\left(\mathrm{Max}(\mu_A + 3\sigma_A, \mu_B + 3\sigma_B) - \mu_C\right)$$

LP model based on statistical timing

- Variables
  - Timing, delay variables with mean μ and std dev σ
  - Auxiliary variables, $T_{Tb_i}, t_{tb_i}, W_i = Tb_i - tb_i, \mu_{W_i}, \sigma_{W_i}$
- Constraints
  - Gate constraints
    - Timing window at the inputs for a two-input gate i

$$\mu_{Tb_i} \ge \mu_{Ta_1}; T_{Tb_i} \ge \mu_{Ta_1} + 3\sigma_{Ta_1}; \qquad \mu_{tb_i} \le \mu_{ta_1}; t_{tb_i} \le \mu_{ta_1} - 3\sigma_{Ta_1};$$

$$\mu_{Tb_i} \ge \mu_{Ta_2}; T_{Tb_i} \ge \mu_{Ta_2} + 3\sigma_{Ta_2}; \qquad \mu_{tb_i} \le \mu_{ta_2}; t_{tb_i} \le \mu_{ta_2} - 3\sigma_{Ta_2};$$

$$\sigma_{Tb_i} = (T_{Tb_i} - \mu_{Tb_i})/3; \qquad \sigma_{tb_i} = (\mu_{tb_i} - t_{tb_i})/3;$$

    - Timing window at outputs

$$\mu_{Ta_i} = \mu_{Tb_i} + \mu_{d_i}; \quad \sigma_{Ta_i} = k(\sigma_{Tb_i} + r \cdot \mu_{d_i});$$

$$\mu_{ta_i} = \mu_{tb_i} + \mu_{d_i}; \quad \sigma_{ta_i} = k(\sigma_{tb_i} + r \cdot \mu_{d_i});$$

LP model based on statistical timing

- Constraints
  - Gate constraint
    - Linear approximation

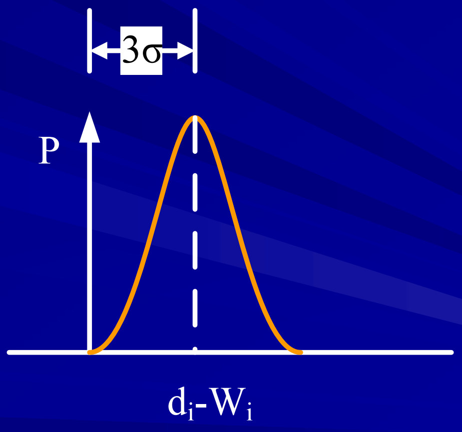
$$\sigma_{Ta_i} = \sqrt{\sigma_{Tb_i}^2 + (r \cdot \mu_{d_i})^2} \Leftrightarrow \sigma_{Ta_i} = k(\sigma_{Tb_i} + r \cdot \mu_{d_i})$$

  - k ∈ [0.707, 1]; choose k=0.85, since $\frac{A+B}{\sqrt{2}} \le \sqrt{A^2 + B^2} \le A + B;$
  - Glitch filtering constraints

$$\mu_{W_i} = \mu_{Tb_i} - \mu_{tb_i};$$

$$\sigma_{W_i} = k(\sigma_{Tb_i} + \sigma_{tb_i});$$

$$\mu_{d_i} - \mu_{W_i} > 3 \cdot k(\sigma_{W_i} + r \cdot \mu_{d_i});$$



  - Circuit delay constraint

$$\mu_{Ta_i} \cdot (1 + 3r) \le D_{max}$$

LP model based on statistical timing

- Parameter
  - r, $\sigma/D_{nom,i}$ ratio
  - D_{max}, circuit delay parameter
  - α, optimism factor

$$\mu_{d_i} - \mu_{W_i} > 3 \cdot k(\sigma_{W_i} + r \cdot \mu_{d_i}) \cdot \alpha;$$

  - $\alpha=1$, no relaxation
  - $\alpha<1$, optimistic about the actual glitch width
  - $\alpha=0$, reduce to previous model
- Objective
  - Minimize #buffer inserted – sum of buffer delays

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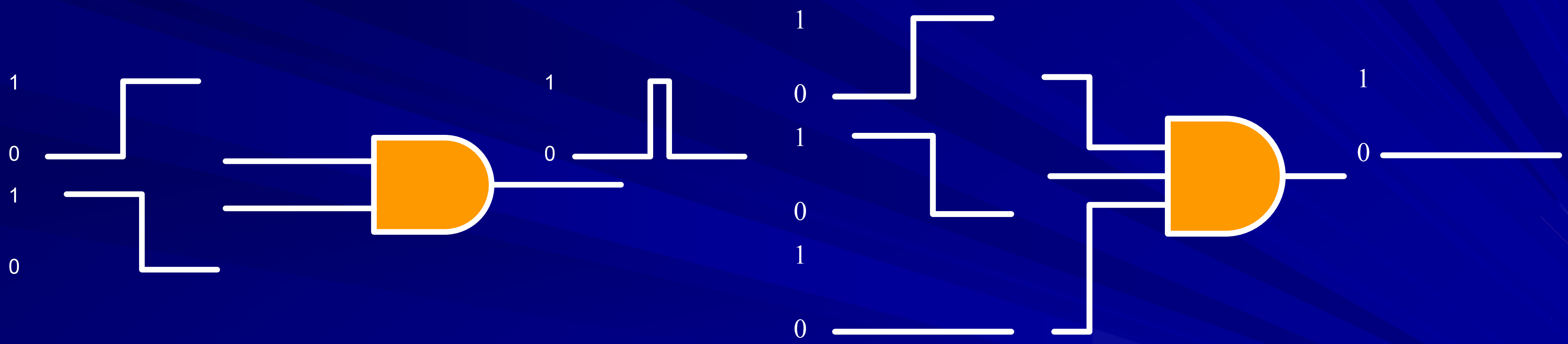
Input-specific optimization

- Motivation
  - Previous LP models guarantees glitch filtering for any input vector sequence
    - $T_i - t_i < d_i$ for all gates
  - Redundancy in optimization
    - Insertion of more buffers
    - Increased the overhead in power/area
  - In reality, circuit under embedded environments
    - Optimization for input vector sequence that is possible to the circuit, e.g., functional vectors
    - Same reduction in power dissipation w/ less trade-offs in overheads

Input-specific optimization

- Glitch generation pattern
  - Input vector pair that can potentially generate a glitch
  - AND gate example:



- Glitch generation probability $P_g[i]$
  - Probability glitch-generation pattern occurs at input of gate i
  - Steady state signal values match the pattern

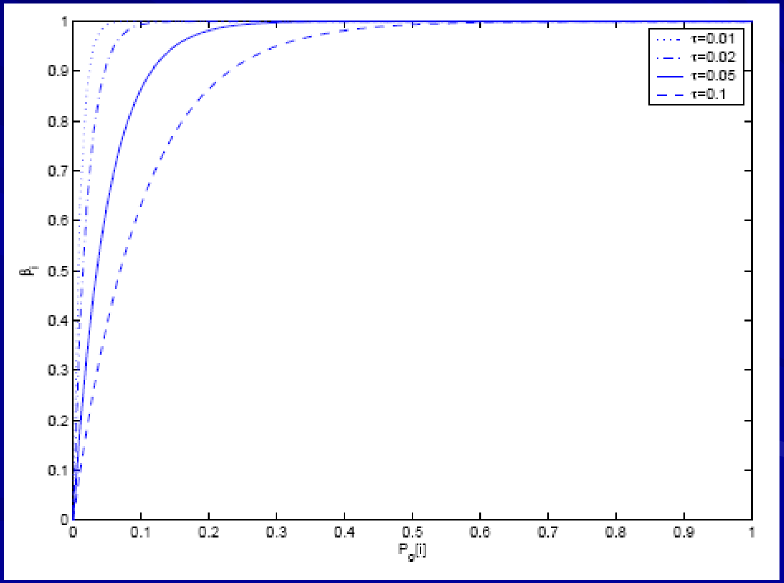
Input-specific optimization

- Application to Previous model w/o process-variation
  - Static optimization
    - Only static glitches/hazards considered
  - Relaxation of constraints
    - Relax glitch filtering constraints where glitches unlikely happen
    - $T_i - t_i < d_i$ => $(T_i - t_i) * \beta_i < d_i$
    - Selective relaxation

$$\beta_i = \begin{cases} 0 \text{ if } P_g[i] = 0 \\ 1 \text{ if } P_g[i] > 0 \end{cases}$$

    - Generalized relaxation

$$\beta_i = 1 - e^{-P_g[i]/\tau}$$



Input-specific optimization

- Application to process-variation-resistant LP model based on statistical timing
  - Static optimization
  - Relaxation of constraints

$$\mu_{d_i} > [\mu_{W_i} + 3 \cdot k(\sigma_{W_i} + r \cdot \mu_{d_i}) \cdot \alpha] \cdot \beta_i;$$

    - Selective relaxation
    - Generalized relaxation
  - Tuning factor
    - Original objective

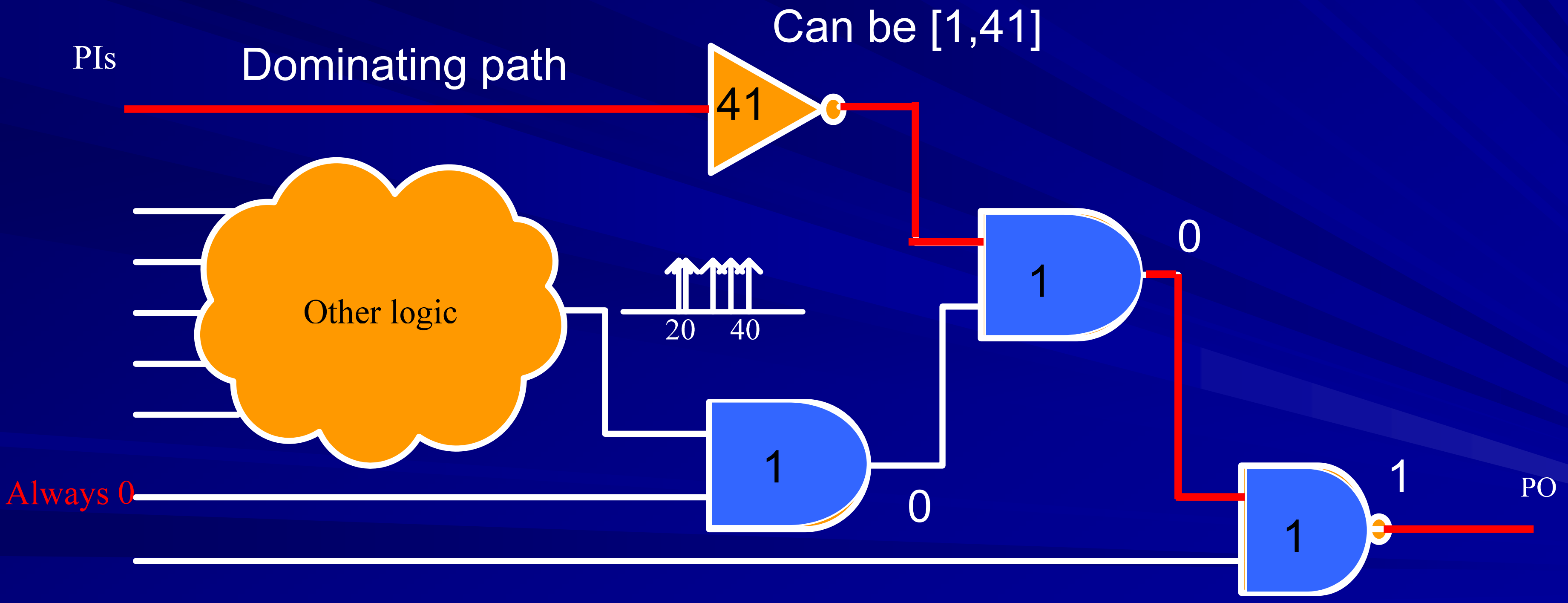
$$\text{Minimize } \sum_j d_j; \quad (j \in \text{ buffers})$$

    - Current objective

$$\text{Minimize } \sum_j d_j \; + \; TF \cdot (\frac{1}{N} \cdot \sum_i d_i); \quad (j \in \text{ buffers, } i \in \text{ other gates})$$

Input-specific optimization

- Why need a tuning factor
  - Dominating path affected critical delay distribution



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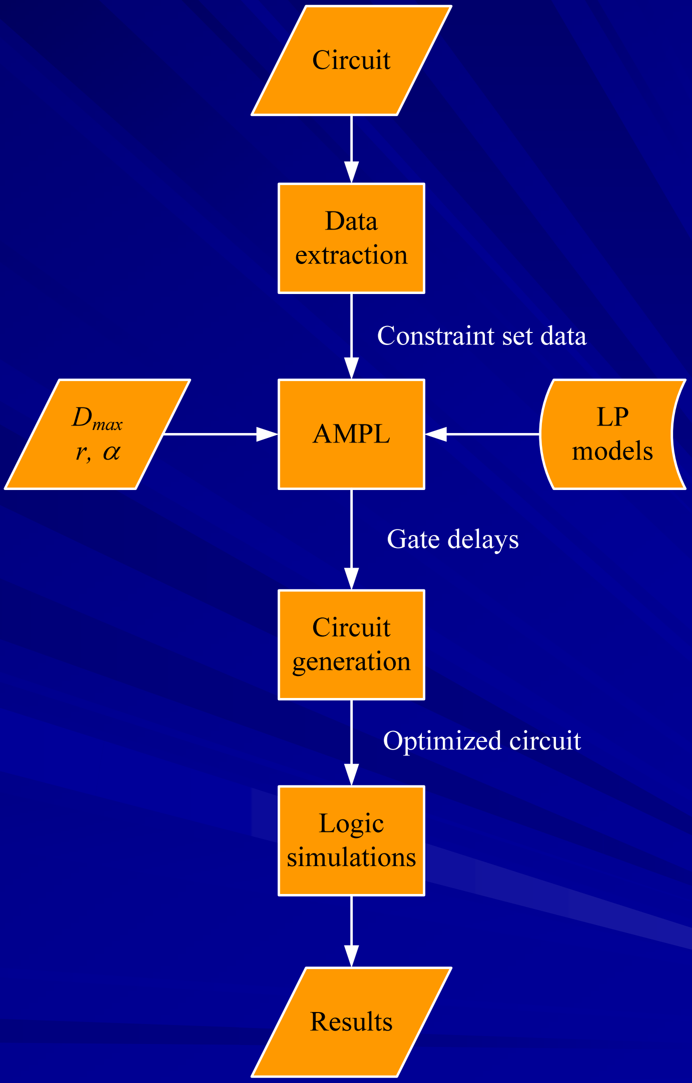
Experimental results

- Experimental procedure
  - Flow chart
  - Power estimation
    - Event driven logic simulation
    - Fanout weighted sum of switching activities
    - Variations of C_L and V_{dd} ignored
    - Monte-Carlo simulation with 1,000 samples of delays under process-variation
  - Results analysis
    - Un-Opt., unit-delay circuit
    - Opt, previous optimization
    - Opt1, Proc-var-rst optimization worst-case timing
    - Opt2, Proc-var-rst optimization statistical timing



Experimental results – small variation

- Power dissipation under no process variation

	UnOpt	Opt (w/o proc var.)			Opt1 (worst case proc)			Opt2 (statistical proc)		
	Pwr.	Pwr.	Buf.	maxdelay	Pwr.	Buf.	Dmax	Pwr.	Buf.	Dmax
c432	1.0	0.74	95	17	0.74	96	20	0.74	99	20
	1.0	0.74	66	34	0.74	91	40	0.74	91	40
c499	1.0	0.94	80	11	0.94	88	13	0.94	97	13
	1.0	0.94	48	22	0.94	88	26	0.94	129	26
c880	1.0	0.54	63	24	0.54	45	28	0.54	76	28
	1.0	0.54	29	72	0.54	37	83	0.54	37	83
c1355	1.0	0.93	224	24	0.93	296	28	0.93	305	28
	1.0	0.93	160	72	0.93	296	83	0.93	273	83
c1908	1.0	0.53	84	40	0.53	68	46	0.52	136	46
	1.0	0.55	54	120	0.53	92	138	0.52	198	138
c2670	1.0	0.74	157	32	0.79	244	37	0.73	313	37
	1.0	0.74	26	96	0.75	80	111	0.73	168	111
c3540	1.0	0.60	219	47	0.59	228	55	0.59	306	55
	1.0	0.59	103	141	0.61	152	163	0.59	303	163
c5315	1.0	0.56	281	49	0.62	228	57	0.55	401	57
	1.0	0.56	113	147	0.58	130	170	0.55	460	170
c6288	1.0	0.13	881	124	0.15	801	143	0.14	1685	143
	1.0	0.13	864	372	0.14	922	428	0.13	1213	428
c7552	1.0	0.52	369	43	0.64	180	50	0.52	464	50
	1.0	0.52	62	129	0.56	162	149	0.52	879	149

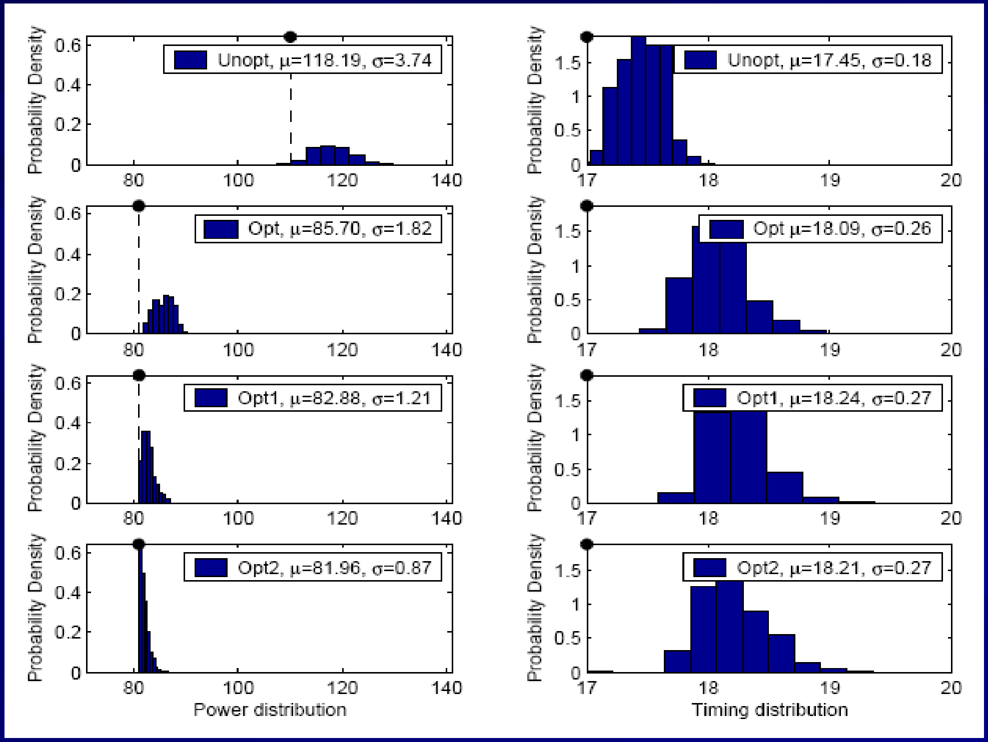
Experimental results – small variation

- Power distribution under 5% inter-die, 5% intra-die variation

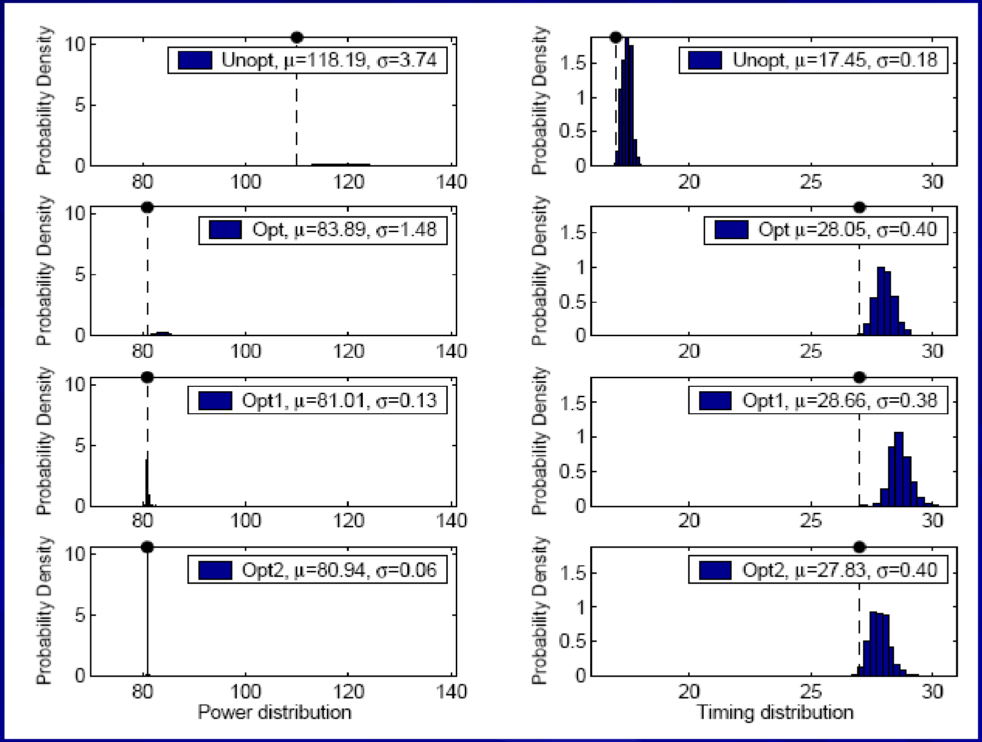
Circuit	Maxdelay	Un-Opt		Opt (w/o proc var.)		Opt1 (worst case proc)		Opt2 (statistical proc)	
		Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)
c432	17	1.08	17.5	0.78	12.8	0.75	7.0	0.75	4.5
	34	1.08	17.5	0.76	8.2	0.74	0.1	0.74	0.1
c499	11	1.06	12.9	1.00	12.6	0.95	0.7	0.95	0.7
	22	1.06	12.9	0.99	12.6	0.94	0.0	0.94	0.1
c880	24	1.03	7.1	0.62	23.1	0.58	13.9	0.55	7.5
	72	1.03	7.1	0.57	12.8	0.55	1.1	0.54	1.0
c1355	24	1.10	18.1	0.99	10.6	0.96	5.5	0.95	4.2
	72	1.10	18.1	0.98	8.8	0.93	0.3	0.93	0.1
c1908	40	1.15	21.0	0.64	28.6	0.62	22.8	0.58	21.6
	120	1.15	21.0	0.64	21.5	0.54	5.9	0.54	6.5
c2670	32	1.17	21.8	0.80	11.6	0.81	5.5	0.75	4.8
	96	1.17	21.8	0.77	6.1	0.78	5.2	0.74	1.8
c3540	47	1.15	18.9	0.66	15.2	0.65	12.9	0.63	9.7
	141	1.15	18.9	0.62	7.2	0.63	5.1	0.59	1.3
c5315	49	1.12	14.9	0.62	13.8	0.67	9.9	0.59	9.1
	147	1.12	14.9	0.60	10.3	0.61	6.8	0.56	3.7
c6288	124	1.46	49.9	0.27	131.6	0.28	105.9	0.24	93.6
	372	1.46	49.9	0.26	128.3	0.23	76.8	0.18	56.0
c7552	43	1.17	19.6	0.57	12.4	0.72	13.3	0.57	11.8
	129	1.17	19.6	0.56	9.3	0.58	5.1	0.53	3.5

Experimental results – small variation

- Power timing analysis
  - Example c432



maxdelay=17

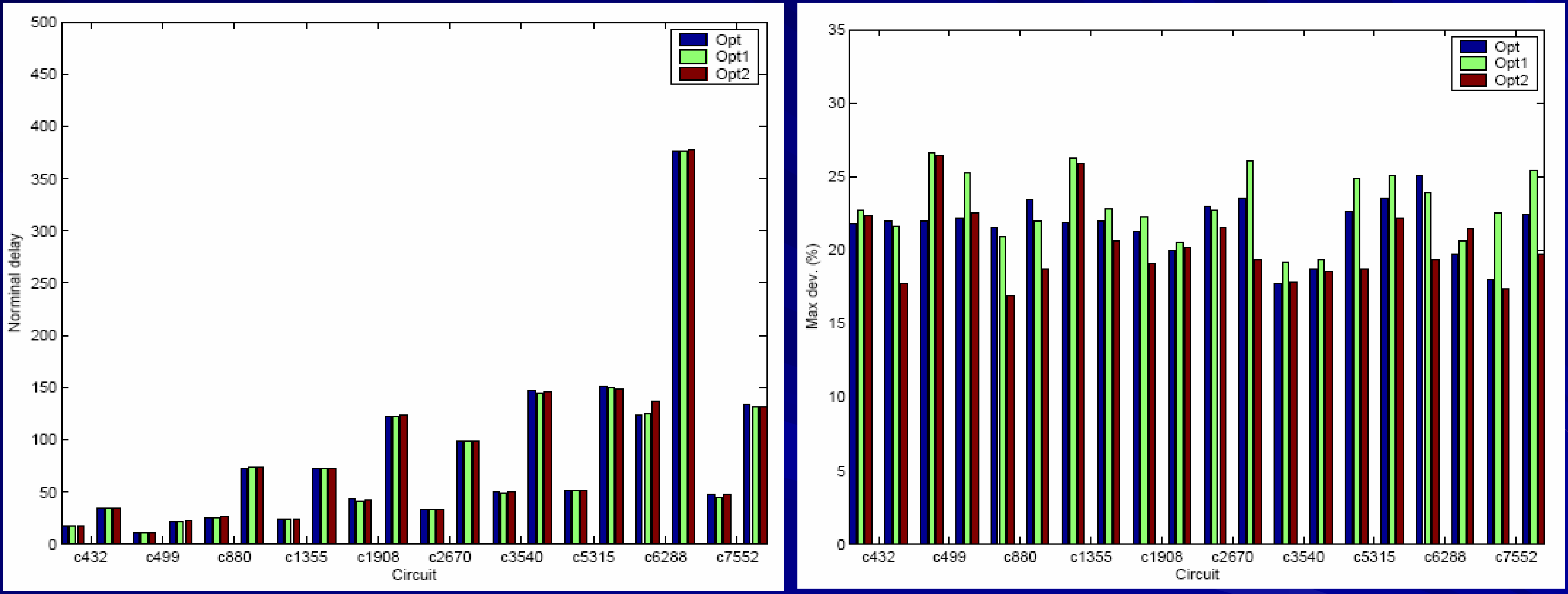


maxdelay=26

  - Complete suppression of power variation

Experimental results – small variation

- Critical delay distribution



Nominal delay

Max. Deviation

  - Similar nominal delay
  - Reduced variation by Opt2 for c880, c2670, c5315, c7552

Experimental results – large variation

- Power dissipation under no process-variation

	Un-opt.	Opt (w/o proc var.)			Opt1 (worst case proc)			Opt2 (statistical proc)		
	Pwr.	Pwr.	Buf.	maxdelay	Pwr.	Buf.	Dmax	Pwr.	Buf.	Dmax
c432	1.00	0.74	66	34	0.75	87	50	0.74	88	50
	1.00	0.74	58	68	0.74	81	99	0.74	106	99
c499	1.00	0.94	48	22	0.97	88	32	0.94	88	32
	1.00	0.94	0	33	0.97	0	48	0.94	129	48
c880	1.00	0.54	35	48	0.58	36	70	0.54	57	70
	1.00	0.54	30	120	0.59	29	174	0.54	62	174
c1355	1.00	0.93	192	48	0.95	264	70	0.93	305	70
	1.00	0.93	128	120	0.96	264	174	0.93	305	174
c1908	1.00	0.53	62	80	0.55	41	116	0.52	135	116
	1.00	0.54	34	200	0.56	12	290	0.52	190	290
c2670	1.00	0.74	34	64	0.80	39	93	0.74	249	93
	1.00	0.74	9	160	0.78	95	232	0.73	211	232
c3540	1.00	0.59	139	94	0.62	149	137	0.59	281	137
	1.00	0.59	78	235	0.65	52	341	0.59	311	341
c5313	1.00	0.56	167	98	0.66	93	143	0.55	399	143
	1.00	0.56	53	245	0.60	144	356	0.55	418	356
c6288	1.00	0.13	870	228	0.14	1303	331	0.13	1121	331
	1.00	0.13	857	620	0.13	939	899	0.13	1473	899
c7552	1.00	0.52	91	86	0.69	64	125	0.52	481	125
	1.00	0.52	44	215	0.60	622	312	0.52	645	312

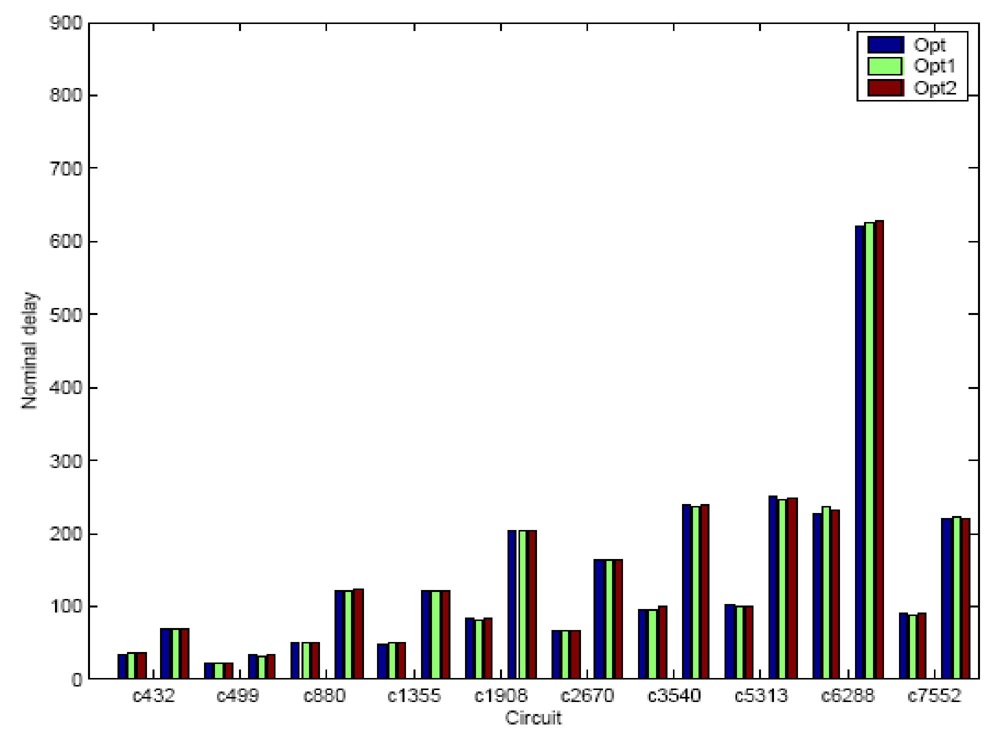
Experimental results – large variation

- Power distribution under 15% intra-die and 5% inter-die variation

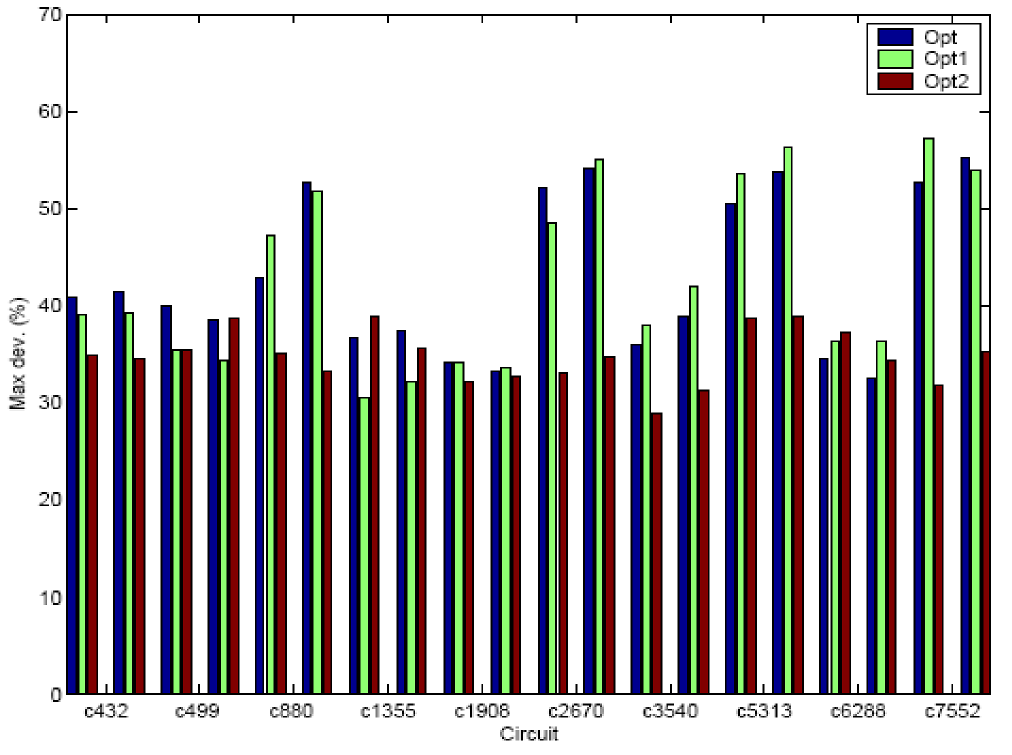
		Un-opt		Opt (w/o proc var.)		Opt1 (worst case proc)		Opt2 (statistical proc)	
Circuit	Max-delay	Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)	Mean Pwr.	Max. Dev. (%)
c432	34	1.09	19.8	0.78	12.6	0.78	12.1	0.76	11.1
	68	1.09	19.8	0.77	10.3	0.75	6.1	0.74	3.7
c499	22	1.07	14.0	1.02	15.3	0.98	1.7	0.95	2.0
	33	1.07	14.0	0.99	10.2	0.97	1.4	0.95	1.0
c880	48	1.04	8.0	0.62	26.5	0.63	15.7	0.59	18.2
	120	1.04	8.0	0.60	22.7	0.60	5.6	0.55	8.6
c1355	48	1.13	21.8	1.06	19.7	0.98	7.3	0.98	10.2
	120	1.13	21.8	1.05	18.8	0.97	1.7	0.94	3.0
c1908	80	1.16	23.1	0.72	49.6	0.66	30.1	0.64	35.8
	200	1.16	23.1	0.66	32.3	0.62	18.8	0.58	21.4
c2670	64	1.19	25.4	0.81	13.6	0.90	16.0	0.80	13.6
	160	1.19	25.4	0.80	11.2	0.82	8.6	0.76	6.2
c3540	94	1.16	20.7	0.67	19.5	0.69	16.9	0.66	17.8
	235	1.16	20.7	0.66	16.1	0.71	11.7	0.62	10.1
c5313	98	1.13	16.5	0.67	24.6	0.74	16.3	0.63	20.8
	245	1.13	16.5	0.64	19.0	0.66	13.9	0.60	13.4
c6288	228	1.45	52.2	0.43	274.3	0.36	193.4	0.38	223.8
	620	1.45	52.2	0.41	264.0	0.31	161.5	0.26	125.3
c7552	86	1.17	21.9	0.64	25.8	0.78	16.0	0.59	18.7
	215	1.17	21.9	0.60	20.2	0.65	11.2	0.56	11.8

Experimental results – large variation

- Critical delay distribution



Nominal delay



Max. Deviation (%)

  - Similar nominal delay
  - Reduced delay variation by Opt2

Experimental results – input-specific optimization

- Application to "Opt" under no process-variation, IS-Opt

		Un-Opt	Opt (w/o proc var.)			IS-Opt (input-specific w/o proc)		
	maxdelay	Pwr.	Pwr.	Delay	Buffers	Pwr.	Delay	Buffers
c432	34	1.0	0.74	34	66	0.74	35	66
	68	1.0	0.74	68	58	0.74	69	41
c499	22	1.0	0.94	22	48	0.94	22	33
	33	1.0	0.94	33	0	0.95	33	0
c880	48	1.0	0.54	51	35	0.54	49	32
	120	1.0	0.54	121	30	0.54	122	24
c1355	48	1.0	0.93	48	192	0.93	48	113
	120	1.0	0.93	121	128	0.93	120	25
c1908	80	1.0	0.53	82	62	0.54	86	52
	200	1.0	0.54	203	34	0.53	204	3
c2670	64	1.0	0.74	65	34	0.74	66	30
	160	1.0	0.74	163	9	0.74	162	1
c3540	94	1.0	0.59	95	139	0.59	101	122
	235	1.0	0.59	239	78	0.59	239	73
c5315	98	1.0	0.56	100	167	0.56	104	170
	245	1.0	0.56	249	53	0.56	250	52
c6288	228	1.0	0.13	226	870	0.13	228	870
	620	1.0	0.13	620	857	0.13	620	853
c7552	86	1.0	0.52	89	91	0.52	88	84
	215	1.0	0.52	220	44	0.52	221	38

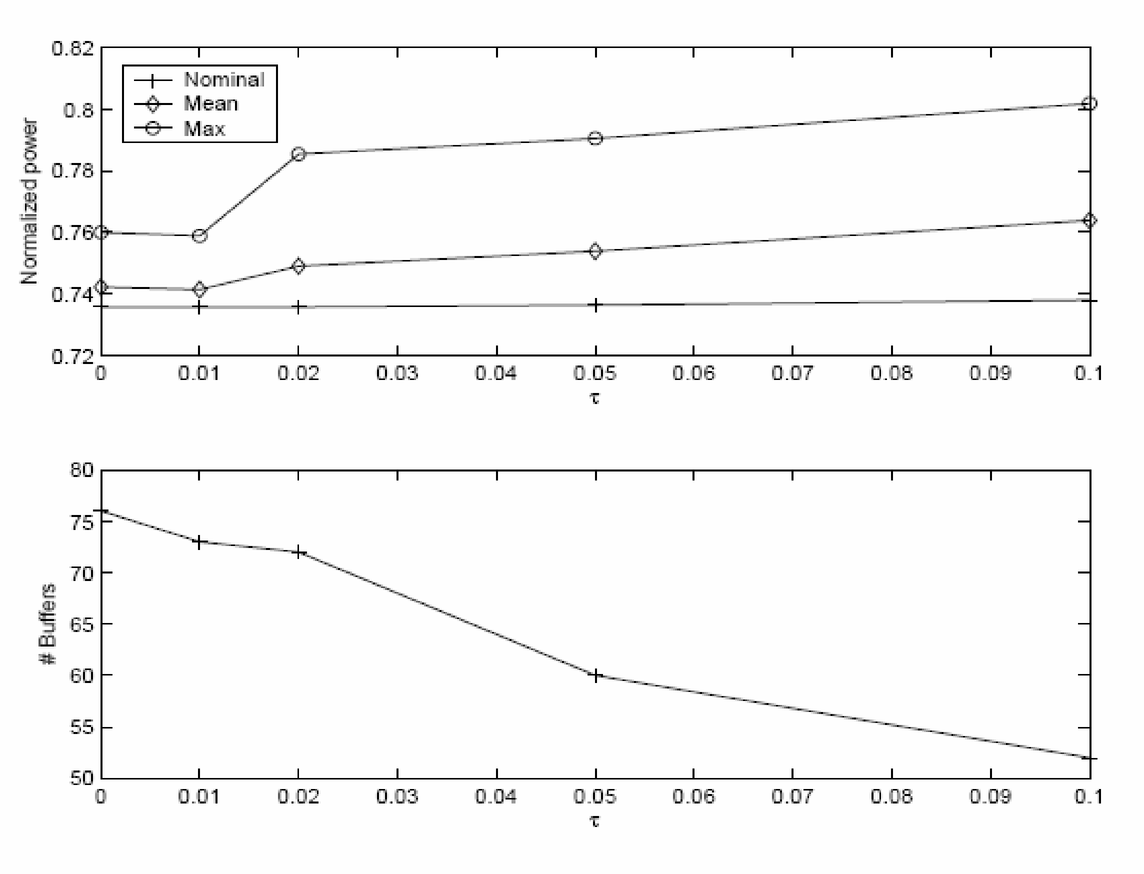
Experimental results – input-specific optimization

- Application to “Opt2” under process-variation, IS-Opt2 under 15% intra-die and 5% inter-die variation

		Un-opt.	Opt2 (statistical proc)				IS-Opt2 (input-specific statistical proc)			
Cir.	D_{Max}	Nom. Pwr.	Nom. Pwr.	Mean Pwr.	Max Dev. (%)	No. Buf.	Nom. Pwr.	Mean Pwr.	Max Dev. (%)	No. Buf.
c432	50	1.0	0.74	0.76	11.1	88	0.74	0.76	9.3	81
	99	1.0	0.74	0.74	3.7	106	0.74	0.74	3.3	76
c499	32	1.0	0.94	0.95	2.0	88	0.94	0.95	1.9	88
	48	1.0	0.94	0.95	1.0	129	0.94	0.95	1.8	58
c880	70	1.0	0.54	0.59	18.2	57	0.54	0.59	20.4	38
	174	1.0	0.54	0.55	8.6	62	0.54	0.56	9.0	38
c1355	70	1.0	0.93	0.98	10.2	305	0.93	1.01	13.1	253
	174	1.0	0.93	0.94	3.0	305	0.93	0.95	4.7	160
c1908	116	1.0	0.52	0.64	35.8	135	0.52	0.64	34.7	107
	290	1.0	0.52	0.58	21.4	190	0.52	0.57	18.4	104
c2670	93	1.0	0.74	0.80	13.6	249	0.73	0.79	11.3	186
	232	1.0	0.73	0.76	6.2	211	0.73	0.75	4.3	79
c3540	137	1.0	0.59	0.66	17.8	281	0.59	0.65	15.6	247
	341	1.0	0.59	0.62	10.1	311	0.59	0.61	7.4	188
c5315	143	1.0	0.55	0.63	20.8	399	0.55	0.63	21.0	389
	356	1.0	0.55	0.60	13.4	418	0.55	0.60	13.2	413
c6288	331	1.0	0.13	0.38	223.8	1121	0.13	0.38	225.2	1115
	899	1.0	0.13	0.26	125.3	1473	0.13	0.26	125.5	1243
c7552	125	1.0	0.52	0.59	18.7	481	0.52	0.58	18.1	389
	312	1.0	0.52	0.56	11.8	645	0.52	0.55	10.9	520

Experimental results – input-specific optimization

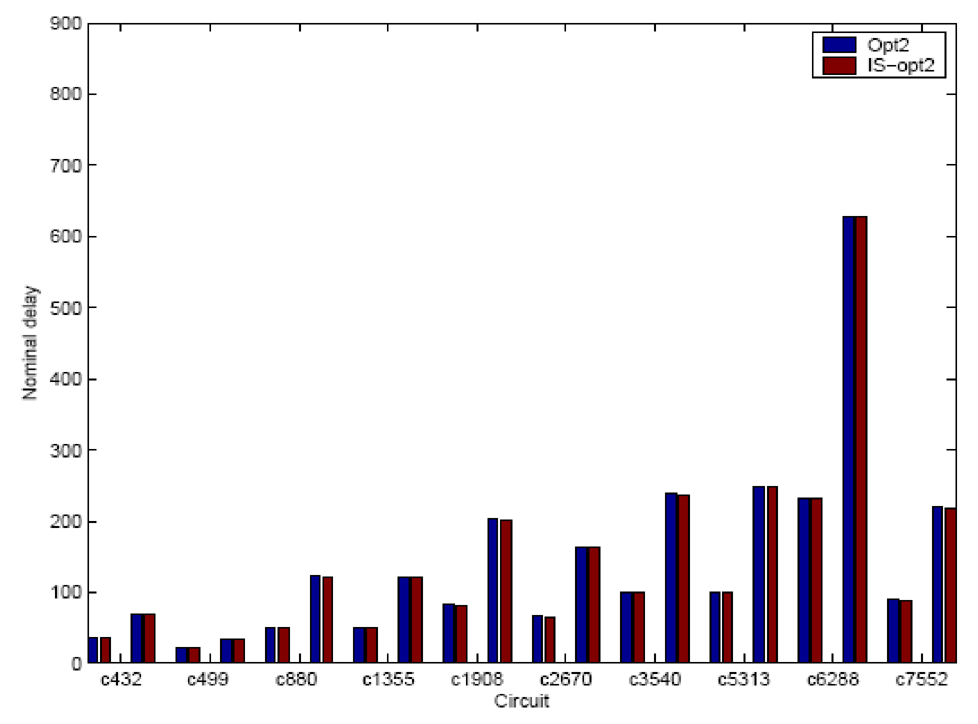
- Trade-off by generalized relaxation



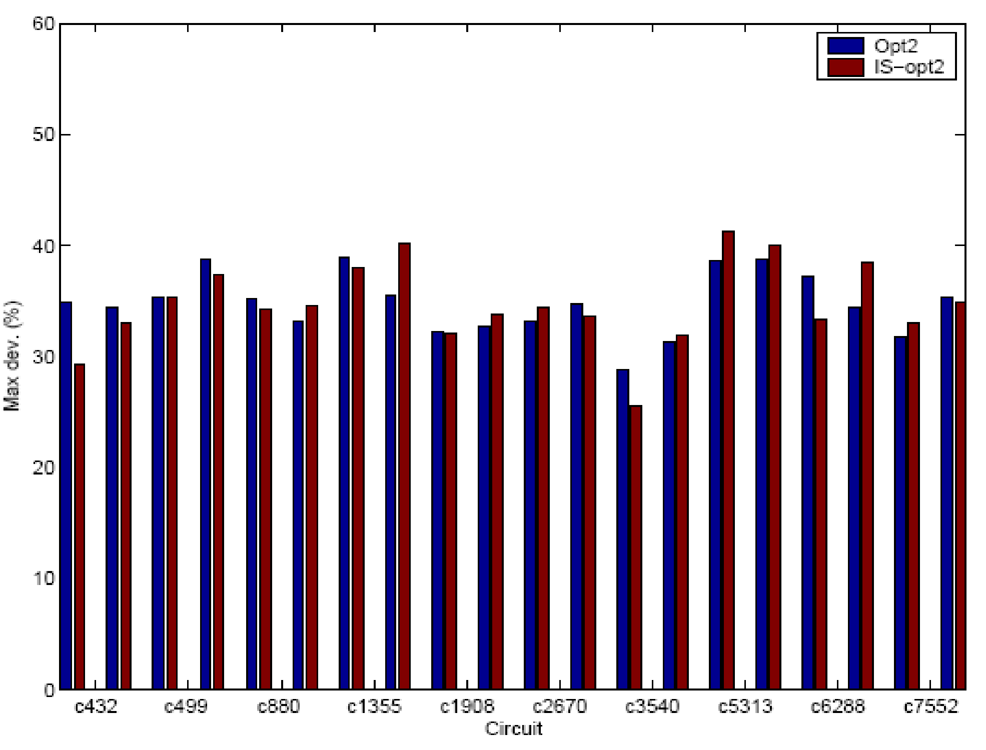
  - c432 circuit with varying τ value
  - Reduction of #buffers with degradation of power distribution

Experimental results – input-specific optimization

- Critical delay



Nominal delay



Max. deviation

  – Similar performance for “Opt2” and “IS-Opt2”

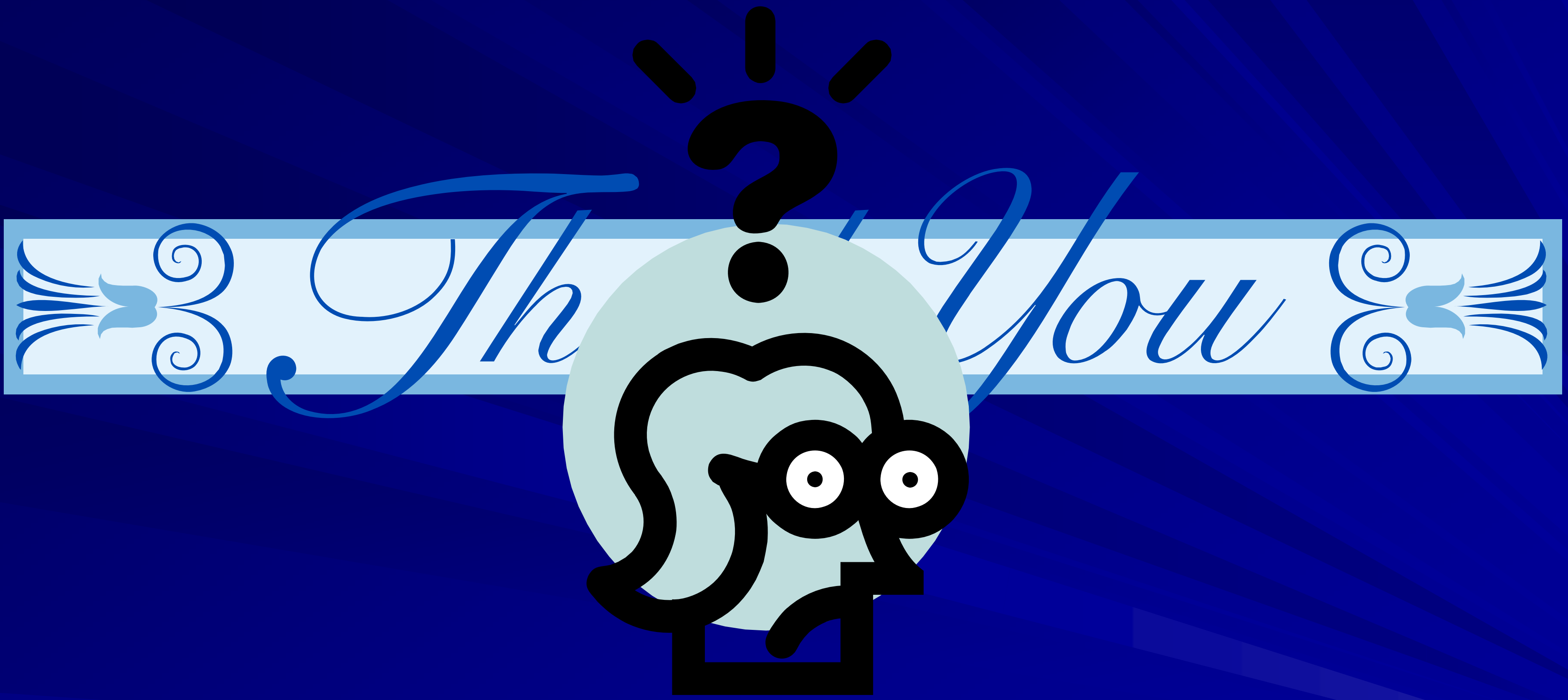
Outline

- Introduction
- Background
  - Dynamic power dissipation
  - Glitch reduction
  - Previous LP model
- Process-variation-resistant LP model
  - Process variation
  - Delay model
  - LP model based on worst-case timing
  - LP model based on statistical timing
- Input-specific optimization
  - Without process-variation
  - With process-variation
- Experimental results
- Conclusion

Conclusions

- Proposed a dynamic power optimization technique that is resistant to the process variation
- Consider process-variation in terms of the delay variations
  - inter-die and intra-die variations
  - Prove inter-die variation has negligible effect on switching activity and power
- Construct two new LP models
  - Worst case timing analysis
  - Statistical timing analysis
- Input-specific optimization to reduce number of buffers
  - Circuit optimized for certain input vector sequence
- Experimental results
  - Complete suppression of power variation for small circuit and variations
  - Significant reduction of power and delay variations for larger circuit and variations
    - 53% reduction in power deviation, 40% reduction in delay deviation under 15% intra-die and 5% inter-die variation
  - Input-specific optimization reduces trade-off (buffers) significantly w/ equivalent power and delay performance
    - IS-Opt2 vs. Opt2, Up to 63% reduction of buffer

Questions



- For more questions, contact me at hufei01@auburn.edu