# Built-In Test and Calibration of DAC/ADC Using A Low-Resolution Dithering DAC*

Wei Jiang and Vishwani D. Agrawal
Electrical and Computer Engineering, Auburn University, Auburn, AL 36849
wzj0003@auburn.edu, vagrawal@eng.auburn.edu

## Abstract

This paper presents a BIST scheme to test and calibrate on-chip DAC and ADC and to improve both linearity and resolution of converters using a built-in sigma-delta modulator. We use a dithering dynamic element matching (DEM) techniques. A first-order sigma-delta modulator is used to sample DAC outputs because of high linearity of its outputs with high oversampling rate (OSR). The scheme is capable of characterizing non-linearity of DAC/ADC by a polynomial-fitting algorithm to obtain calibration coefficients. A built-in low-cost low-resolution dithering DAC is employed to compensate analog outputs of the on-chip DAC for higher resolution and linearity. Simulation shows that using a 6-bit dithering DAC a 14-bit on-chip DAC could be calibrated with 2-bit ENOB gain. Calibration of the on-chip ADC is also discussed.

## 1 Introduction

Many modern mixed-signal integrated circuits (IC) include built-in digital-to-analog converters (DAC) or analog-to-digital converters (ADC). Linearity and resolution are critical measurements for DACs and ADCs of a mixed-signal system-on-chip (SoC). They determine overall performance of the device. With increasing requirements for high resolution DAC/ADC set by high speed DSP processors and digital circuitry, it becomes more challenging to test the on-chip converters, especially for system-on-chips (SoC). It also becomes more expensive and difficult to testing such high performance converters using external automated testing equipments (ATE). In mixed-signal systems, the DFT scheme used for digital components can be used to test the analog components [11, 12]. Built-in self-test (BIST) is a promising solution here because it provides an automatic internal test for the circuit under test (CUT) during and after fabrication. A typical BIST scheme needs a test stimuli generator and a response collector as well as a data analyzer to determine whether or not the CUT is working properly before notifying the result to outside.

Some BIST schemes have been studied for testing of embedded DAC/ADC in SoC. Huang and Cheng [3] employ a 1-bit sigma-delta modulator for BIST of mixed-signal circuits with on-chip stimulus generation and response analysis. Ong *et al.* [8] propose a $2^{nd}$-order sigma-delta modulator based BIST architecture which is capable of self characterizing, though with low resolution. Several authors [4, 6, 13] describe histogram based BIST architectures to perform test on DAC/ADC using low-cost low-precision converters. However, large amount of memory is required for these histogram approaches, especially for high resolution DAC/ADC, since results for all codes must be stored and compared with predefined reference values to determine the linearity of converters.

Another technique [1] using full digital stimuli for cheap but accurate testing of high resolution ADC has

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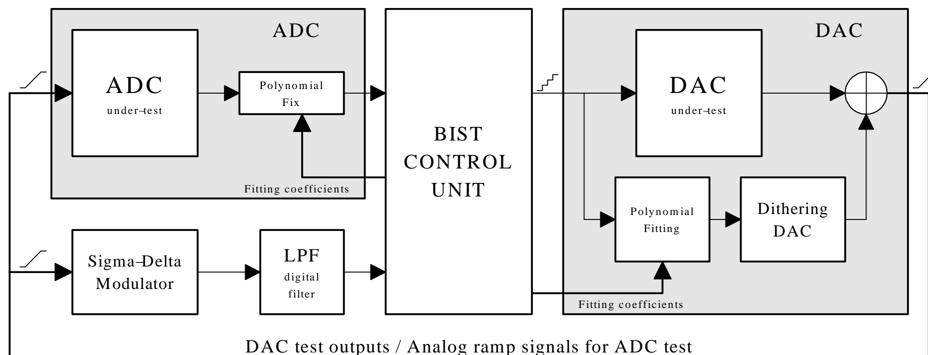


Figure 1: Proposed BIST scheme for testing and calibration of DAC/ADC.

been proposed. But the scheme is complex because pulse-width modulation (PWM) signals are used. Some papers [5, 14] also use dithering technique to obtain precise analog signals for high quality stimuli generation.

## 2 Testing and Calibration Scheme

In this paper, a novel BIST scheme, shown in Figure 1, is presented for test and calibration of DAC/ADC. A first-order 1-bit sigma-delta modulator samples DAC outputs and a low-precision dithering DAC compensates for quantization errors at the outputs for higher linearity and resolution in the normal operation. A DSP processor acting as BIST control unit is needed in this BIST scheme to generate sequential digital codes as test stimuli for CUT, to analyze sampled data from sigma-delta modulator, and to calibrate CUT outputs by characteristics calculated from data analysis results.

It is assumed that a mixed-signal IC with on-chip DAC/ADC, when powered up, initially completes a BIST procedure for digital components including a DSP processor. The proposed BIST scheme then starts the test and calibration of DAC/ADC. The BIST control unit first tests and characterizes DAC using a sigma-delta modulator and then calibrates it using a dithering DAC to eliminate quantization error and improve the linearity and quality of DAC output provided the quantization error is in the range of compensation. The calibrated DAC can be considered fault-free with higher resolution and therefore acts as an accurate analog ramp signal generator for ADC test in the final step of the BIST.

During ADC test, BIST control unit gives the same consecutive codes as DAC test to calibrated DAC to obtain a high quality ramp waveform, and then samples conversion data from ADC-under-test instead of the sigma-delta modulator. The quantization error from ADC-under-test is the main source of noise in the ADC test. Since we have calibrated DAC before testing ADC, we can test and characterize ADC using its outputs. An at-speed digital reverse-function generator is needed to make fixes to the ADC outputs in order to achieve high-linearity. It should be noted, however, that unlike DAC-under-test the resolution of ADC-under-test is not improved.

A sigma-delta modulator is chosen for sampling DAC output because of its simple structure and low cost. The modulator only works during initial calibration steps and is put into sleep mode once the calibration is completed.

In an actual implementation, to facilitate calculation and ensure that BIST takes on sampled digital data $\hat{k}$ corresponding to each digital code $k$ fed into CUT as test stimulus, $\Delta v_k = v_k - \hat{v}_k$ is used for analysis and calculation rather than the sampled code $\hat{k}$. The differential values actually represent the sum of quantization errors of DAC-under-test and sigma-delta modulator and, therefore, the generated polynomial curve fits integral non-linearity ($INL_k$) for each code. The maximum value of

$INL_k$ is considered as the extreme value of the quantization error and therefore the reference voltage for dithering DAC for calibration of on-chip DAC.

For an $N$-bit DAC working under a reference voltage $V_{ref}$, there are $2^N$ codes and the minimum unit voltage represented by the least significant bit (LSB) is $V_{ref}/2^N$. The maximum quantization error may not exceed 1 LSB, theoretically, but considering fault tolerance of the quantization error, a slightly larger reference voltage is used on the dithering DAC, typically 3 LSB for wide enough voltage range. Since the reference voltage of dithering DAC is much lower than that of DAC-under-test, the analog signals generated by dithering DAC can be fine tuned to compensate for most of DAC quantization error and achieve higher linearity and resolution. In this case a 6-bit dithering DAC is used for compensation with reference voltage of 3 LSB for an on-chip 14-bit DAC. Thus, the voltages of 1 LSB and 3 LSB are

$$V_{1LSB} = \frac{V_{ref}}{2^{14}} \quad (1)$$

$$V_{3LSB} = \frac{V_{ref}}{2^{11}} \quad (2)$$

Using 3 LSB as the reference voltage of 6-bit dithering DAC, we get

$$V'_{ref} = V_{3LSB} = \frac{V_{ref}}{2^{11}} \quad (3)$$

$$V'_{1LSB} = \frac{V'_{ref}}{2^6} = \frac{V_{ref}}{2^{17}} \quad (4)$$

Hence, there is no need for a high quality dithering DAC in this BIST scheme and we may easily obtain a high resolution calibrated DAC using a low cost and low quality dithering DAC. A dithering DAC with up to 2 LSB quantization error is sufficient to obtain a calibrated DAC whose effective number of bits (ENOB) is 16.

## 2.1 Test Stimuli

Test stimuli are a series of consecutive codes generated by BIST control unit as inputs to the DAC-under-test. These range from the least value (all zeros) to the most value (all ones). For these consecutive code inputs the DAC outputs an analog signal, a ramp waveform, from which INL parameters can be calculated. Because of the non-linearity introduced by the DAC during conversion of digital codes into the analog waveform the ramp may not be purely linear. According to a previous study [10] the non-linear part is nearly $3^{rd}$-order and therefore can be represented through a fitted curve using a polynomial function.

## 2.2 Polynomial-Fitting Algorithm

A simplified polynomial-fitting algorithm [9, 10] can be employed for characterizing DAC/ADC by four coefficients that form a best fit $3^{rd}$-order polynomial curve for the transfer function of the converters. By dividing the input code range of the DAC into four equal segments. For all segments, $S_0$, $S_1$, $S_2$ and $S_3$ are the sums of outputs corresponding the included codes. Syndromes, $B_0$, $B_1$, $B_2$ and $B_3$, are then obtained as specific linear combinations of the sums, and these allow the computation of four coefficients, $b_0$, $b_1$, $b_2$ and $b_3$, for a least mean-square fit of a third-order polynomial:

$$y(x) = b_0 + b_1 x + b_2 x^2 + b_3 x^3 \quad (5)$$

where $x$ is the input code and $y(x)$ is the analog output of DAC.

This algorithm [9, 10] eliminates the requirement for massive amount memory to store individual sampled data as some schemes using histogram algorithms do. In Section 3, we apply this kind of third-order mean-square fit to the integral nonlinearity (INL) calculated as the difference between the actual DAC output and the ideal output for all input codes. The proposed best fit polynomial algorithm is then used to check the functionality of DAC, as well as to control the dithering DAC to produce proper analog compensation signal for each code.

## 2.3 Sigma-Delta Modulator and Digital Filter

The digital BIST circuitry cannot process the analog ramp signals directly, so we employ a first-order 1-bit sigma-delta modulator to sample DAC output and to convert each analog signal $k$ to corresponding digital code $\hat{k}$.

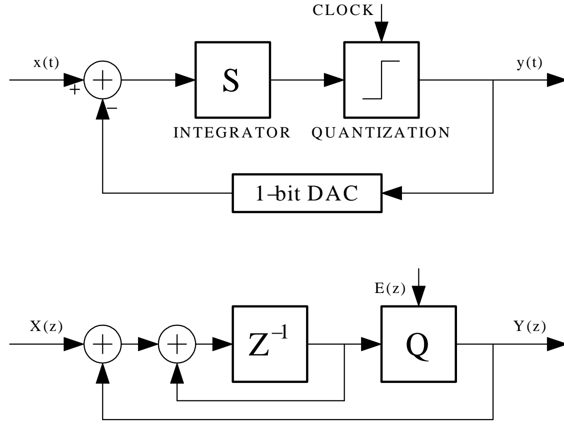


Figure 2: Sigma-Delta modulator and its transfer function in $z$-domain.

The proposed sigma-delta modulator includes an integrator, an 1-bit quantizer, and an 1-bit DAC. With oversampling and noise-shaping techniques sigma-delta DAC is simple to design and implement for achieving high linearity without strict requirements for high quality components. By oversampling the quantization noise of sigma-delta ADC is uniformly distributed over a wider band up to half of sampling frequency (Nyquist frequency) and therefore the overall noise figure is reduced. Because the signal to noise ratio (SNR) of simple oversampling increases by 3dB for each doubled sampling rate, the oversampling rate (OSR) must be quadrupled for each ENOB of resolution gain. The feedback loop (consisting of a quantizer and a 1-bit DAC) acts as a low-pass filter for input analog signals and high-pass filter for internal quantization error. So the quantization noise is removed from the lower band and is concentrated in the high-frequency end of the Nyquist band. Therefore, the noise is shaped to higher band than input signals.

More than one integration and loop stages could be used to build high-order sigma-delta modulators for better quantization noise-shaping and ENOB gain for a given OSR. However, a high-order sigma-delta modulator is not as stable and linear as a first-order modulator [7], which is our choice in this application. Testing time of the first-order 1-bit sigma-delta modulator is not an issue since the testing and calibration procedure is executed only during chip powering up and therefore modulator will not affect the performance of the normal operation.

Figure 2 shows the circuit of first-order 1-bit sigma-delta modulator. The transfer function of the modulator is

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{6}$$

where $E(z)$ is the quantization error introduced by the sigma-delta modulator.

Assuming oversampling rate of a sigma-delta modulator is $M$, each analog signal output by DAC-under-test for code $k$ must have $M$ samples by the modulator. The SNR of sigma-delta modulator with an oversampling rate $M$ is

$$M = \frac{f_s}{f_0} \tag{7}$$

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}\left(\frac{1}{M}\right)^{3/2} \tag{8}$$

$$SNR = \frac{1}{n_0 \cdot 2\sqrt{2}} \tag{9}$$

$$\approx \frac{\sqrt{3}M^{3/2}}{2\sqrt{2}\pi} \tag{10}$$

where $f_s$ is the sampling frequency of sigma-delta modulator and $f_0$ is the operational frequency of the DAC.

Assuming $e_{rms} = 1$, the input signal RMS value is $1/2\sqrt{2}$ and SNR for the first-order sigma-delta modulator can be obtained. Generally, we can get higher SNR using larger oversampling rate at the cost of longer measuring time for each code, but this would apply only to BIST stage and does not affect DAC/ADC performance during normal operations.

The reference voltage of the modulator must be same as that for the DAC-under-test in order to make sure that the conversion result is precise and any difference between results and stimuli is only quantization error introduced by the DUT itself.

The accuracy of modulator must be higher than that of DUT, which means that the resolution of the modulator is higher than that of DUT, in order to measure the DUT outputs. Furthermore, delta-sigma modulator may have to be accurate enough to calibrate DUT for several more bits

of resolution. We estimate the required number of bits of the modulator from the following equation:

$$ENOB_{\Sigma\Delta} = N_{DUT} + N'_{d-DAC} - \log_2 \alpha \qquad (11)$$

where we have $N$-bit resolution for DAC-under-test, $N'$-bit resolution for dithering DAC, and $\alpha$ as a scaling factor for INL range of fault tolerance. Taking a large value for $\alpha$, the scheme becomes more capable of fixing the nonlinearity error of DUT but the final calibrated resolution becomes lower. On the other hand, a small $\alpha$ can be used for better calibration result with a reduced range of nonlinearity error tolerance. Suppose, we choose $\alpha = 8$, giving 3 LSB range of fault tolerance. The ENOB of the modulator must be larger than $\hat{N} = N + N' - 3$ for the desired INL voltage range. Thus, the SNR of the sigma-delta modulator is [2]

$$SNR = 6.02\hat{N} + 1.76 \qquad (12)$$

where $\hat{N}$ is ENOB of the modulator calculated above for given DUT and dithering DAC.

The output of sigma-delta modulator is a bit stream of '0' or '1' which contains high-frequency noise and cannot be directly processed by BIST control unit. A low-pass digital filter (LPF) is required to filter out the noise. We use a simple integrator at the output of sigma-delta modulator as LPF. It has been shown [6] that the $z$-domain transfer function of a modulator and integrator is given by,

$$Y(z) = \frac{z^{-1}}{1 - z^{-1}} X(z) + E(z) \qquad (13)$$

where $X(z)$ is sigma-delta input, $Y(z)$ is the integrator output and $E(z)$ is quantization error. Thus, the input signal is recovered and quantization error is not accumulated, improving the overall SNR. The final LPF output is then converted to usual digital code $\hat{k}$, corresponding to input stimulus $k$ plus quantization error from both DAC-under-test and sigma-delta modulator.

Since the reference voltage is only about 3 LSB of DAC-under-test, the quantization error of sigma-delta modulator is much less than that of DAC-under-test and therefore can be ignored.

## 2.4 Calibration with Dithering DAC

We apply the polynomial-fitting algorithm mentioned in Section 2.2 [9, 10] to emulate the curve of DAC quantization error

$$\Delta v_k = v_k - \hat{v}_k \qquad (14)$$

for each test stimulus code $k$, where $v_k$ is the ideal DAC output and $\hat{v}_k$ is the actual output of DAC-under-test. Four coefficients of a $3^{rd}$-order polynomial function are calculated from the sums obtained from four equally-divided segments. $\Delta k$ is the $N'$-bit code of calculated voltage value $\Delta v_k$ by $N$-bit code $k$ and $\hat{N}$-bit code $\hat{k}$. $\Delta k$ will be used by digital BIST control unit for actual calculation to obtain coefficients. These four coefficients will be used to recover $N'$-bit code $\Delta k$, to generate compensation signal for DAC output during ADC BIST in next step, and in the normal operation until the power is finally turned off.

An $N'$-bit dithering DAC using a dynamic element matching (DEM) technique is used for accurate compensation with high-tolerance mismatches among the current sources of the DAC. Assuming DEM iteration factor $p$, meaning $N'$-bit dithering DAC generates $p$ outputs for each input code $\Delta k$, we get DEM elements distance factor $q$ so that $p \cdot q = 2^{N'}$. After eliminating spurious data by an LPF, the performance of dithering DEM DAC is comparable to an ideal DAC with $N' + \log_2 p$ ENOB as discussed in a previous paper [4]. A typical implementation of dithering DEM DAC contains $2^{N'}$ current sources which are divided into $p$ segments with element distance of $q$. For any code $k$, $k$ consecutive current sources from $(d-1)q+1$ through $(d-1)q+k$ are turned on at $d^{th}$ iteration $(1 \leq p)$.

## 2.5 Testing and Calibration of ADC

The implementation of BIST circuitry and algorithm to test ADC-under-test is quite similar to the techniques used for DAC-under-test. BIST control unit generates exactly the same consecutive codes as digital test stimuli for the on-chip DAC, which then outputs an analog ramp signal. BIST reads the digital conversion output of ADC-under-test whose input is the ramp signal. Since testing and calibration of DAC has been completed in the previous step

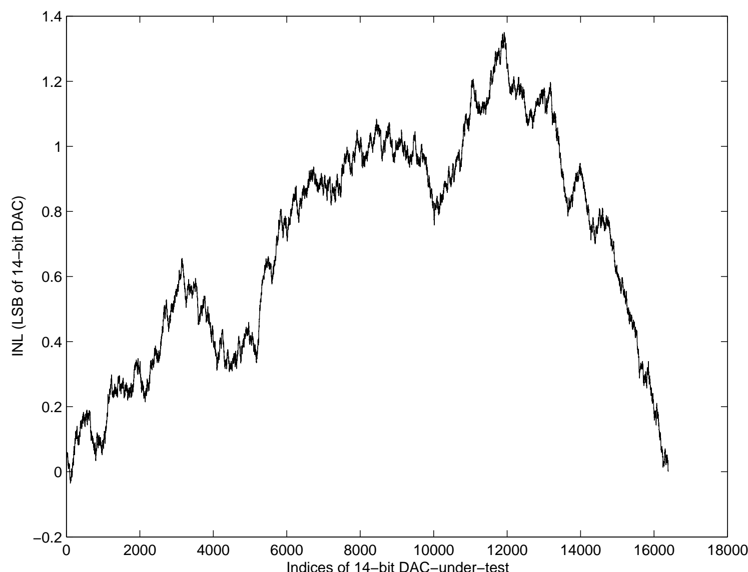


Figure 3: INL of simulated 14-bit DAC-under-test.

and the resolution and linearity is improved, the quantization error of DAC may be ignored now.

Four coefficients of a third-order best-fitting polynomial function are obtained from the output of ADC in a similar fashion as was done for the sigma-delta modulator in the previous step. The calibration of ADC is simple,

$$k = k' + \Delta k \tag{15}$$

where $k'$ is $N'$-bit ADC output, $\Delta k$ is calculated from polynomial function, and $k$ is calibrated result. We should point out that this procedure only makes limited compensation to the linearity and does not improve the resolution of ADC-under-test.

# 3 Simulation Results

The proposed test and calibration approach is verified by simulation in Matlab for 14-bit on-chip DAC and ADC model on various quantization noise level. A 6-bit low-cost dithering DAC model is used in the simulation to generate compensating analog signal for DAC calibration.

Table 1: Third-order polynomial fit for INL of Figure 3.

| $i$ | Sum, $S_i$ | Syndrome, $B_i$ | Coefficient, $b_i$ |
|---|---|---|---|
| 0 | $2.5437E3$ | $-0.1959E4$ | 0.93 |
| 1 | $1.9997E3$ | $-1.1045E4$ | $9.2746E5$ |
| 2 | $-3.3732E3$ | $-2.8564E3$ | $-1.0391E8$ |
| 3 | $3.1289E3$ | $-2.3792E3$ | $-1.4088E12$ |

The reference voltage for the dithering DAC is 3 LSB of on-chip DAC considering fault tolerance of its resolution. However, this is enough to calibrate the on-chip DAC with 3 more ENOB.

Figure 3 depicts INL of a 14-bit DAC with maximum 1.4 LSB quantization error from a Matlab simulation in which random noise was introduced. The maximum INL magnitude is within a predefined range, e.g., 3 LSB in this case, so that this on-chip DAC could be calibrated. If $INL_k$ for any code $k$ falls outside the specified range, the on-chip DAC would fail the test.

By dividing the INL data of Figure 3 into four equal code segments, we get sums $S_0$, $S_1$, $S_2$ and $S_3$, syndromes

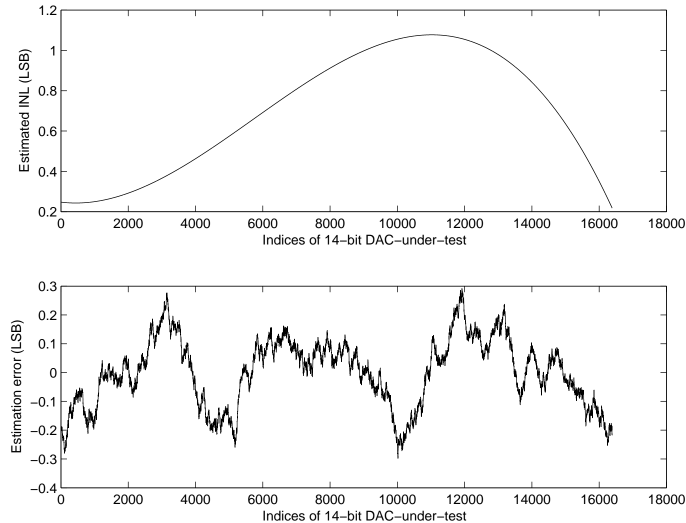


Figure 4: Least mean-square fit third-order polynomial (top) and estimation error (bottom) for DAC-under-test INL data of Figure 3.

$B_0$, $B_1$, $B_2$, and $B_4$, and polynomial fit coefficients $b_0$, $b_1$, $b_2$, and $b_3$ shown in Table 1. These were obtained by the method of Section 2.2 [9, 10]. Figure 4 shows the best mean-square third-order polynomial fit and the estimation error by the fitting algorithm. The average per code error is about $-39.3dB$.

Similar results for a low-quality 6-bit dithering DAC are shown in Figure 5. The reference voltage of the DAC is typically 3 LSBs of the DAC-under-test. Using a reference voltage higher than 3 LSB will provide a larger range of calibration and hence better fault-tolerance but will lower the calibrating precision and worsen linearity. On the other hand, using less than 3 LSB will provide better calibration precision and linear outputs but worsen the fault-tolerance of the DAC.

The final calibrated output of the 14-bit DAC-under-test using the 6-bit dithering DAC is shown in Figure 6. The calibrated is not exactly as ideal as shown in Figure 4 and the average per code estimation error is about $-38.0dB$. However, the INL of the calibrated DAC is not large than 0.25 LSB, which is comparable to the ideal DAC so that the DAC-under-test is improved by 2-bit resolution.

# 4 Conclusion

A BIST scheme for testing and calibration of on-chip DAC/ADC with low-cost sigma-delta modulation and dithering DEM DAC is presented in this paper. A sigma-delta modulator is used to sample the DAC outputs and a third-order polynomial least mean-square fitting algorithm is employed to characterize the DAC. The analog output of DAC is calibrated for higher linearity and resolution by compensation signals from dithering DAC. Similar algorithm is also proposed for test and calibration of ADC for improved linearity. The calibration method has been verified by simulation in which a 6-bit dithering DAC is used for improving the linearity of a 14-bit on-chip DAC.

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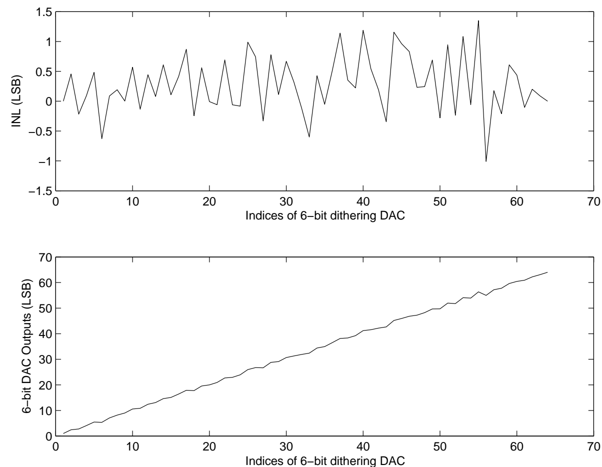


Figure 5: INL (top) of simulated 6-bit dithering DAC, and DAC outputs (bottom).

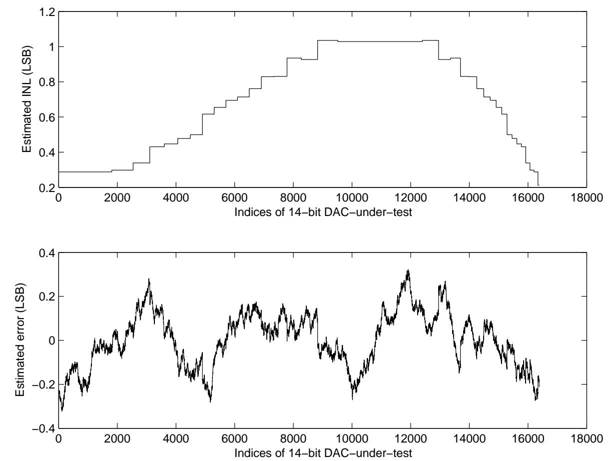


Figure 6: INL (top) of calibrated 14-bit DAC-under-test using 6-bit dithering DAC, and corresponding INL error (bottom).


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