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Career Objective

Be a strong contributor to the profession of computer engineering and be counted among the **top ten** professionals in my area of expertise – **electronic testing**. Conduct leading edge and innovative research to advance the state of the art of semiconductor products. Most recent research includes original inventions of *a hazard-free low-power design, a high-speed testing method, a combinational ATPG method for partial-scan circuits, and spectral testing methods*. **University teaching**, developed curricula, courses and text-books: have taught undergraduate and graduate courses, most recently voluntarily, co-authored a text-book, directed PhD and Master's research, served as co-PI on NSF grants, and served on the ECE Advisory Boards of three universities. Other interests are general computing systems, parallel and distributed computing, and neural network based algorithms.

Personal

Born February 7, 1943, married, two children, permanent resident of the United States.

Education

PhD 1971, University of Illinois at Urbana-Champaign, Thesis: *Mutual Coupling in Phased Arrays of Randomly Spaced Antennas*, Advisor: Y. T. Lo.

ME (With Distinction) 1966, Indian Institute of Science, Bangalore, India, Thesis: *Reactance Modulation of Dielectric Rod Surface Wave Structure*, Advisor: S. K. Chatterjee.

BE (Honours) 1964, University of Roorkee, Roorkee, India, Thesis: *Design and Construction of Directional Loudspeaker for S.W.P. Hanger*, Advisor: P. V. Indiresan.

Employment History

Since December 2003, Auburn University, Auburn, Alabama: James J. Danaher Professor of Electrical and Computer Engineering.

1991-2003, Rutgers University, Piscataway, New Jersey: *Visiting Professor, ECE Dept. (Honorary position)*, teaching VLSI testing course and supervising masters and doctoral research with Professors Michael Bushnell and Michael Hsiao (now with Virginia Tech).

2001-2002, Agere Systems, Murray Hill, New Jersey: *Distinguished Member of Technical Staff*, Circuits and Systems Research Lab, leading research on new techniques for VLSI test generation, design for testability, low-power design, and topics relevant to VLSI architectures, design and test.

- 1990-2000, Bell Labs, Murray Hill, New Jersey:** *Distinguished Member of Technical Staff*, Computing Sciences Research Center, job function same as above.
- 1986-1990, AT&T Bell Laboratories, Murray Hill, New Jersey:** *Member of Technical Staff*, Computing Sciences Research Center, job function same as present.
- 1982-1986, AT&T Bell Laboratories, Murray Hill, New Jersey:** *Supervisor, VLSI Test and Design Verification Group*, responsible for invention of test methods and development of computer-aided design (CAD) tools (including company-wide user training and counseling): TITUS (testability implementation and test generation using scan), SCOAP testability analysis system, STAFAN (statistical fault analysis), CRITIC (critical timing analysis of ICs), ALERT (a logic expert for reviewing testability), MISL (Motis input stimulus language), and HASTEN (hardware accelerated simulation and test environment). Initiated work on functional fault simulation and expert system for logic verification. Served on a task force (May-December 1984) to assess Company's CAE needs and strategy for tool development. During 1985-86, chaired a task force for development of built-in self-test (BIST) in AT&T.
- 1978-1982, Bell Laboratories, Murray Hill, New Jersey:** *Member of Technical Staff*, developed Bell Labs' first static timing analyzer and scan design system for VLSI; was part of a team that produced one of the world's first mixed-mode simulator; developed simulation, analysis and test tools for VLSI design and conducted research on topics related to design, verification, testing and design for testability.
- 1975-1978, TRW Defense & Space Systems Group, Redondo Beach, California:** *Member of Technical Staff*, designed and prototyped spacecraft (TDRSS) antennas (reflectors, arrays and omnidirectional) and designed and implemented company's most modern computer-based antenna test facility; conducted research on multifrequency reflector antenna and received the IEEE Antennas & Propagation Transactions' **Best Applications Paper Award**.
- 1972-1975, Indian Institute of Technology, New Delhi, India:** *Assistant Professor*, developed phase shifters and phased array antennas for radar, taught undergraduate and graduate courses, and directed research in electrical engineering.
- 1971-1972, EG&G, Inc., Albuquerque, New Mexico:** *Senior Scientist*, developed electromagnetic pulse (EMP) simulators for the United States Air Force.
- 1970-1971, Automation Technology, Inc., Champaign, Illinois:** *Research Engineer*, developed automated methods of logic testing for the ILLIAC IV computer project; published a paper describing the idea of combining random and algorithmic test generation techniques.
- 1967-1970, University of Illinois, Urbana, Illinois:** *Research and Teaching Assistant*, conducted research on phased array antennas and taught electrical engineering courses.
- 1966-1967, Indian Institute of Technology, New Delhi, India:** *Associate Lecturer*, taught undergraduate and graduate courses in electrical engineering.

Professional Society Memberships

- Fellow** Institute of Electrical and Electronics Engineers (IEEE), elected 1986.
- Fellow** Association for Computing Machinery (ACM), elected 2003.
- Fellow** Institution of Electronics and Telecommunications Engineers (IETE, India), elected 1983.
- Member** VLSI Society of India (VSI)

Patents

1. **U.S. Patent 6,131,181** *Method and System for Identifying Tested Path Delay Faults*, October 10, 2000.
2. **U.S. Patent 5,983,007** *Low Power Circuits Through Hazard Pulse Suppression*, November 9, 1999.
3. **U.S. Patent 5,657,240** *Testing and Removal of Redundancies in VLSI Circuits with Non-Boolean Primitives*, August 12, 1997.
4. **U.S. Patent 5,606,567** *Delay Testing of High-Performance Digital Components by a Slow-Speed Tester*, February 25, 1997.
5. **U.S. Patent 5,590,13** *Testing a Sequential Circuit*, December 31, 1996.
6. **U.S. Patent 5,499,249** *Method and Apparatus for Test Generation and Fault Simulation for Sequential Circuits with Embedded Random Access Memories (RAMs)*, March 12, 1996.
7. **U.S. Patent 5,461,573** *VLSI Circuits Designed for Testability and Methods for Producing Them*, October 24, 1995.
8. **U.S. Patent 5,377,201** *A Transitive Closure Based Process for Generating Test Vectors for VLSI Circuits*, December 27, 1994.
9. **U.S. Patent 5,365,528** *Method for Testing Delay Faults in Non-Scan Sequential Circuits*, November 15, 1994.
10. **U.S. Patent 5,257,268** *Cost-function Directed Search Method for Generating Tests for Sequential Logic Circuits*, October 26, 1993.
11. **U.S. Patent 5,228,040** *Testable Implementations of Finite State Machines and Methods for Producing Them*, July 13, 1993.
12. **U.S. Patent 5,043,986** *Method and Integrated Circuit Adapted for Partial Scan Testability*, August 27, 1991.
13. **U.S. Patent 4,493,077** *Scan Testable Integrated Circuit*, January 8, 1985.

Awards – General

1. **Lifetime Achievement Award** 2006, VLSI Society of India, *in recognition of contributions to the area of VLSI test and for founding and steering the International Conference on VLSI Design in India.*
2. **ACM Fellow Award** 2003, *for contributions to testing of digital electronic circuits.*
3. **Certificate of Appreciation** 2000, IEEE Computer Society, *for dedicated service to the Asian Test Symposium and Asian activities of the TTTC.*
4. **Harry H. Goode Memorial Award** 1998, IEEE Computer Society, *for innovative contributions to the field of electronic testing.*
5. **Golden Core Member Citation** 1996, IEEE Computer Society, *for leadership and service.*
6. **Certificate of Appreciation** 1996, IEEE Circuits and Systems Society, *for contribution to the organization of the Eighth International Conference on VLSI Design.*
7. **Distinguished Alumnus Award** 1993, University of Illinois at Urbana-Champaign.

8. **Meritorious Service Award** 1989, IEEE Computer Society, *for contributions to the International Test Conference.*
9. **Outstanding Contribution Award** 1988, IEEE Computer Society, *for contributions to the Design & Test of Computers magazine as its Editor-in-Chief.*
10. **IEEE Fellow Award** 1986, *for contributions to probabilistic testing techniques for large integrated circuits.*
11. **University Prize** 1964, University of Roorkee, India, *for graduating at the top of the Bachelor of Engineering (Telecommunication) class.*
12. **General MacLagan Silver Medals (two)** 1964, University of Roorkee, India, *for obtaining the highest undergraduate class ranks in Line Communications and Radio Engineering.*

Awards – Papers

1. **Honorable Mention Award** 2007, *20th International Conference on VLSI Design*, for the paper, “Spectral RTL Test Generation for Microprocessors,” co-authored with N. Yogi (PhD student at Auburn University.)
2. **Best Student Paper Award** 2006, *15th IEEE North Atlantic Workshop*, for the paper, “High-Level Test Generation for Gate-Level Fault Coverage,” co-authored with Nitin Yogi (PhD student at Auburn University.)
3. **Best Student Paper Award** 2002, *11th IEEE North Atlantic Workshop*, for the paper, “New Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss,” co-authored with Lan Rao (PhD student at Rutgers University) and M. L. Bushnell (Rutgers University.)
4. **Best Student Paper Award** 2000, *14th International Conference on VLSI Design*, for the paper, “Combinational Test Generation for Acyclic Sequential Circuits using a Balanced ATPG Model,” co-authored with Y. C. Kim (PhD student at University of Wisconsin-Madison) and K. K. Saluja (University of Wisconsin-Madison.)
5. **Honorable Mention Award** 1992, *5th International Conference on VLSI Design*, for the paper, “A New Method for Generating Tests for Delay Faults in Non-Scan Circuits,” co-authored with P. Agrawal (Telcordia) and S. C. Seth (University of Nebraska-Lincoln.)
6. **Best Paper Award** 1988, *IEEE International Conference on Computer Design*, for the paper, “Test Generation by Fault Sampling,” co-authored with H. Farhat (University of Nebraska-Omaha) and S. C. Seth (University of Nebraska-Lincoln.)
7. **Best Paper Award** 1987, *AT&T Conference on Electronic Testing*, for the paper, “Use of a Concurrent Fault Simulator for Test Generation,” co-authored with K.-T. Cheng (UCSB) and P. Agrawal (Telcordia.)
8. **Best Presentation Award in the Design & Test Category** 1985, *IEEE International Conference on Computer Design*, for the paper, “Probabilistic Testability,” co-authored with S. C. Seth (University of Nebraska.)
9. **Best Paper Award** 1982, *International Test Conference*, for the paper, “Testability Measures – What Do They Tell Us?” co-authored with M. R. Mercer (Texas A&M University.)
10. **Best Applications Paper Award** 1979, *IEEE Transactions on Antennas and Propagation*, for the paper, “Design of a Dichroic Cassegrain Subreflector,” co-authored with W. A. Imbriale (JPL).

Publications – Books

1. M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Boston: Kluwer Academic Publishers, 2000.
2. E. G. Ulrich, V. D. Agrawal, and J. H. Arabian, *Concurrent and Comparative Discrete Event Simulation*. Boston: Kluwer Academic Publishers, 1994.
3. S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, *Neural Models and Algorithms for Digital Testing*. Boston: Kluwer Academic Publishers, 1991.
4. K. T. Cheng and V. D. Agrawal, *Unified Methods for VLSI Simulation and Test Generation*. Boston: Kluwer Academic Publishers, 1989.
5. V. D. Agrawal and S. C. Seth, *Test Generation for VLSI Chips*. Los Alamitos, CA: IEEE Computer Society Press, 1988.

Publications – Book Chapters

1. S. T. Chakradhar and V. D. Agrawal, “VLSI Design,” in *Encyclopedia of Microcomputers* (A. Kent and J. G. Williams, eds.), pp. 97–111, New York: Marcel Dekker, Inc., 1997. Volume 20.
2. V. D. Agrawal and S. M. Reddy, “Fault modeling and test generation,” in *VLSI Handbook* (J. DiGiacomo, ed.), Chapter 8, New York: McGraw-Hill, 1989.
3. S. C. Seth and V. D. Agrawal, “On the probability of fault occurrence,” in *Defect and Fault Tolerance in VLSI Systems* (I. Koren, ed.), pp. 47–52, Plenum Publishing Corp., 1989.
4. V. D. Agrawal and K. T. Cheng, “Threshold-value simulation and test generation,” in *Testing and Diagnosis of VLSI and ULSI* (F. Lombardi and M. Sami, eds.), pp. 311–323, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1988.
5. V. D. Agrawal, “Statistical testing,” in *Testing and Diagnosis of VLSI and ULSI* (F. Lombardi and M. Sami, eds.), pp. 33–47, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1988.

Publications – Refereed Journals

1. K. Kim and V. D. Agrawal, “Minimum Energy CMOS Design with Dual Subthreshold Supply and Multiple Logic-Level Gates,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2011 (in revision).
2. M. A. Shukoor and V. D. Agrawal, “Diagnostic test Set Minimization and Full-Response Fault Dictionary,” *Journal of Electronic Testing: Theory and Applications*, vol. 27, 2011 (in revision).
3. K. Kim and V. D. Agrawal, “Ultra Low Energy CMOS Logic Using Below-Threshold Dual-Voltage Supply,” *Jour. Low Power Electronics*, vol. 7, no. 4, pp. 460-470, Dec. 2011.
4. T. Raja, V. D. Agrawal, and M. L. Bushnell, “Variable Input Delay CMOS Logic for Low Power Design,” *IEEE Trans. on VLSI Systems*, vol. 17, no. 10, pp. 1534-1545, October 2009.
5. L. Rao, M. L. Bushnell and V. D. Agrawal, “Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss,” *IEEE Trans. VLSI Systems*, vol. 15, no. 11, pp. 1256-1255, November 2007.
6. Y. Lu and V. D. Agrawal, “CMOS Leakage and Glitch Minimization for Power-Performance Tradeoff,” *Jour. Low Power Electronics*, vol. 2, no. 3, pp. 378-387, December 2006.

7. T. Raja, V. D. Agrawal, and M. L. Bushnell, "Transistor Sizing of Logic Gates to Maximize Input Delay Variability," *Jour. Low Power Electronics*, vol. 2, no. 1, pp. 121-128, April 2006.
8. Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "Combinational Automatic Test Pattern Generation for Acyclic Sequential Circuits," *IEEE Trans. CAD*, vol. 24, no. 6, pp. 948-956, June 2005.
9. S. Majumder, B. B. Bhattacharya, V. D. Agrawal, and M. L. Bushnell, "New Classification of Path-Delay Fault Testability in Terms of Stuck-at Faults," *Journal of Computer Science and Technology (Academia Sinica)*, vol. 19, no. 6, pp. 955-964, Nov. 2004.
10. P. A. Thaker, V. D. Agrawal, and M. E. Zaghoul, "A Test Evaluation Technique for VLSI Circuits using Register-Transfer Level Fault Modeling," *IEEE Trans. CAD*, vol. 22, no. 8, pp. 1104-1113, Aug. 2003.
11. A. Giani, S. Sheng, M. Hsiao, and V. D. Agrawal, "Compaction-Based Test Generation Using State and Fault Information," *J. Electronic Testing: Theory and Applic.*, vol. 18, no. 1, pp. 63-72, Feb. 2002.
12. T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Improving path delay testability of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 8, pp. 736-741, Dec. 2000.
13. M. A. Gharaybeh, V. D. Agrawal, M. L. Bushnell, and C. G. Parodi, "False-path removal using delay fault simulation," *J. Electronic Testing: Theory and Applic.*, vol. 16, pp. 463-476, Oct. 2000.
14. A. K. Majhi, V. D. Agrawal, J. Jacob, and L. M. Patnaik, "Line coverage of path delay faults," *IEEE Trans. VLSI Systems*, vol. 8, pp. 610-614, Oct. 2000.
15. T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Path delay fault simulation of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 8, pp. 223-228, Apr. 2000.
16. V. D. Agrawal, "Design of mixed-signal systems for testability," *INTEGRATION, The VLSI J.*, vol. 26, pp. 141-150, 1998.
17. M. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "A parallel-vector concurrent-fault simulator and generation of single-input-change tests for path-delay faults," *IEEE Trans. CAD*, vol. 17, pp. 873-876, Sept. 1998.
18. S. Bose, P. Agrawal, and V. D. Agrawal, "Deriving logic systems for path delay test generation," *IEEE Trans. Computers*, vol. 47, pp. 829-846, Aug. 1998.
19. V. D. Agrawal, D. Lee, and H. Woźniakowski, "Numerical computation of characteristic polynomials of Boolean functions and its applications," *Numerical Algorithms*, vol. 17, pp. 261-278, 1998.
20. L. Pappu, M. L. Bushnell, V. D. Agrawal, and S. Mandyam-Komar, "Statistical delay fault coverage estimation for synchronous sequential circuits," *J. Electronic Testing: Theory and Applications*, vol. 12, pp. 239-254, June 1998.
21. S. Bose, P. Agrawal, and V. D. Agrawal, "A rated-clock test method for path delay faults," *IEEE Trans. VLSI Systems*, vol. 6, pp. 323-331, June 1998.
22. M. A. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "The path-status graph with application to delay fault simulation," *IEEE Trans. CAD*, vol. 17, pp. 324-332, Apr. 1998.
23. S. T. Chakradhar, S. G. Rothweiler, and V. D. Agrawal, "Redundancy removal and test generation for circuits with non-Boolean primitives," *IEEE Trans. CAD*, vol. 16, pp. 1370-1377, Nov. 1997.
24. T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "On variable clock methods for path delay testing of sequential circuits," *IEEE Trans. CAD*, vol. 16, pp. 1237-1249, Nov. 1997.

25. M. A. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "Classification and test generation for path-delay faults using single stuck-at fault tests," *J. Electronic Testing: Theory and Applications*, vol. 11, pp. 55–67, Aug. 1997.
26. K. Heragu, V. D. Agrawal, M. L. Bushnell, and J. H. Patel, "Improving a nonenumerative method to estimate path delay fault coverage," *IEEE Trans. CAD*, vol. 16, pp. 759–762, July 1997.
27. R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling tests for VLSI systems under power constraints," *IEEE Trans. VLSI Systems*, vol. 5, pp. 175–185, June 1997.
28. M. K. Srinivas, J. Jacob, and V. D. Agrawal, "Functional test generation for synchronous sequential circuits," *IEEE Trans. on CAD*, vol. 15, pp. 831–843, July 1996.
29. S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "A partition and resynthesis approach to testable design of large circuits," *IEEE Trans. CAD*, vol. 14, pp. 1268–1276, Oct. 1995.
30. V. D. Agrawal and S. T. Chakradhar, "Combinational ATPG theorems for identifying untestable faults in sequential circuits," *IEEE Trans. CAD*, vol. 14, pp. 1155–1160, Sept. 1995.
31. S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "Test function embedding algorithms with application to interconnected finite state machines," *IEEE Trans. CAD*, vol. 14, pp. 1115–1127, Sept. 1995.
32. S. T. Chakradhar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops," *J. Electronic Testing: Theory and Applic.*, vol. 7, pp. 83–93, Aug. 1995.
33. S. T. Chakradhar, M. Iyer, and V. D. Agrawal, "Energy models for delay testing," *IEEE Trans. CAD*, vol. 14, pp. 728–739, June 1995.
34. K. Heragu, V. D. Agrawal, and M. L. Bushnell, "Fault coverage estimation by test vector sampling," *IEEE Trans. CAD*, vol. 14, pp. 590–596, May 1995. Correction, August 1995, p. 1037.
35. D. Bhattacharya, P. Agrawal, and V. D. Agrawal, "Test generation for path delay faults using binary decision diagrams," *IEEE Trans. Computers*, vol. 44, pp. 434–447, Mar. 1995.
36. V. D. Agrawal, "A tale of two designs: the cheapest and the most economic," *J. Electronic Testing: Theory and Applic.*, vol. 5, pp. 131–135, May 1994.
37. V. D. Agrawal, C. J. Lin, P. Rutkowski, S. Wu, and Y. Zorian, "Built-in self-test for digital integrated circuits," *AT&T Tech. Jour.*, vol. 73, pp. 30–39, Mar. 1994.
38. S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Energy minimization and design for testability," *J. Electronic Testing: Theory and Applic.*, vol. 5, pp. 55–64, Feb. 1994.
39. D. Das, S. C. Seth, and V. D. Agrawal, "Accurate computation of field reject ratio based on fault latency," *IEEE Trans. VLSI Systems*, vol. 1, pp. 537–545, Dec. 1993.
40. S. Bose, P. Agrawal, and V. D. Agrawal, "Path delay fault simulation of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 1, pp. 453–461, Dec. 1993.
41. S. Bose, P. Agrawal, and V. D. Agrawal, "The optimistic update theorem for path delay testing of sequential circuits," *J. Electronic Testing: Theory and Applic.*, vol. 4, pp. 285–290, Aug. 1993.
42. S. T. Chakradhar, V. D. Agrawal, and S. G. Rothweiler, "A transitive closure algorithm for test generation," *IEEE Trans. CAD*, vol. 12, pp. 1015–1028, July 1993.
43. V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A tutorial on built-in self-test, part 2: Applications," *IEEE Design & Test of Computers*, vol. 10, pp. 69–77, June 1993.

44. V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A tutorial on built-in self-test, part 1: Principles," *IEEE Design & Test of Computers*, vol. 10, pp. 73–82, Mar. 1993.
45. P. Agrawal, V. D. Agrawal, and S. C. Seth, "Generating tests for delay faults in nonscan circuits," *IEEE Design & Test of Computers*, vol. 10, pp. 20–28, Mar. 1993.
46. S. T. Chakradhar, S. Kanjilal, and V. D. Agrawal, "Finite state machine synthesis with fault tolerant test function," *J. Electronic Testing: Theory and Applic.*, vol. 4, pp. 57–69, Feb. 1993.
47. V. D. Agrawal and S. T. Chakradhar, "Performance analysis of synchronized iterative algorithms on multiprocessor systems," *IEEE Trans. Parallel and Distr. Syst.*, vol. 3, pp. 739–746, Nov. 1992.
48. J. Jacob and V. D. Agrawal, "Multiple fault detection in two-level multi-output circuits," *J. Electronic Testing: Theory and Applic. (JETTA)*, vol. 3, pp. 171–173, May 1992.
49. E. Ulrich, K. P. Lentz, J. Arabian, M. Gustin, V. D. Agrawal, and P. L. Montessoro, "The comparative and concurrent simulation of discrete-event experiments," *J. Electronic Testing: Theory and Applic. (JETTA)*, vol. 3, pp. 107–118, May 1992.
50. K. T. Cheng and V. D. Agrawal, "Initializability considerations in sequential machine synthesis," *IEEE Trans. Comput.*, vol. 41, pp. 374–379, Mar. 1992.
51. K. T. Cheng and V. D. Agrawal, "State assignment for testable design," *Int. J. Computer Aided VLSI Design*, vol. 3, pp. 291–307, 1991.
52. S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "On test generation using neural computers," *Intl. J. Computer Aided VLSI Design*, vol. 3, pp. 241–257, 1991.
53. K. T. Cheng and V. D. Agrawal, "Methods for synthesizing testable sequential circuits," *AT&T Technical Journal*, vol. 70, pp. 64–86, Jan. 1991.
54. K. T. Cheng, V. D. Agrawal, and E. S. Kuh, "A simulation-based method for generating tests for sequential circuits," *IEEE Trans. on Computers*, vol. 39, pp. 1456–1463, Dec. 1990.
55. V. D. Agrawal and K. T. Cheng, "Finite state machine synthesis with embedded test function," *J. Electronic Testing: Theory and Applications (JETTA)*, vol. 1, no. 3, pp. 221–228, 1990.
56. S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Neural net and boolean satisfiability models of logic circuits," *IEEE Design & Test of Computers*, vol. 7, pp. 54–57, Oct. 1990.
57. S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Toward massively parallel automatic test generation," *IEEE Trans. CAD*, vol. 9, pp. 981–994, Sept. 1990.
58. V. D. Agrawal and H. Kato, "Fault sampling revisited," *IEEE Design & Test of Computers*, vol. 7, pp. 32–35, Aug. 1990.
59. S. C. Seth, V. D. Agrawal, and H. Farhat, "A statistical theory of digital circuit testability," *IEEE Trans. Comput.*, vol. 39, pp. 582–586, Apr. 1990.
60. K. T. Cheng and V. D. Agrawal, "A partial scan method for sequential circuits with feedback," *IEEE Trans. Comput.*, vol. 39, pp. 544–548, Apr. 1990.
61. S. C. Seth and V. D. Agrawal, "A new model for computation of probabilistic testability in combinational circuits," *INTEGRATION, The VLSI Journal*, vol. 7, pp. 49–75, 1989.
62. V. D. Agrawal, K. T. Cheng, and P. Agrawal, "A directed search method for test generation using a concurrent simulator," *IEEE Trans. on Computer-Aided Design*, vol. 8, pp. 131–138, Feb. 1989.

63. V. D. Agrawal, K. T. Cheng, D. D. Johnson, and T. Lin, "Designing circuits with partial scan," *IEEE Design & Test of Computers*, vol. 5, pp. 8–15, Apr. 1988.
64. N. C. E. Srinivas and V. D. Agrawal, "Formal verification of digital circuits using hybrid simulation," *Circuits and Devices*, vol. 4, pp. 19–27, Jan. 1988.
65. S. C. Seth and V. D. Agrawal, "A review of testing of VLSI devices," *IETE Tech. Review*, vol. 1, pp. 363–374, Nov. 1985.
66. S. K. Jain and V. D. Agrawal, "Clarifying statistical fault analysis - authors' reply," *IEEE Design & Test of Computers*, vol. 2, pp. 7–8, Aug. 1985.
67. S. K. Jain and V. D. Agrawal, "Modeling and test generation algorithms for MOS circuits," *IEEE Trans. Comput.*, vol. C-34, pp. 426–433, May 1985.
68. S. C. Seth and V. D. Agrawal, "Cutting chip testing costs," *IEEE Spectrum*, vol. 22, pp. 38–45, Apr. 1985.
69. S. K. Jain and V. D. Agrawal, "Statistical fault analysis," *IEEE Design & Test of Computers*, vol. 2, pp. 38–44, Feb. 1985.
70. M. R. Mercer and V. D. Agrawal, "A novel clocking technique for VLSI circuit testability," *IEEE J. Sol. St. Circ.*, vol. SC-19, pp. 207–212, Apr. 1984.
71. S. C. Seth and V. D. Agrawal, "Characterizing the LSI yield equation from wafer test data," *IEEE Trans. CAD*, vol. CAD-3, pp. 123–126, Apr. 1994.
72. V. D. Agrawal, S. C. Seth, and P. Agrawal, "Fault coverage requirements in production testing of LSI circuits," *IEEE J. Sol. St. Circ.*, vol. SC-17, pp. 57–61, Feb. 1982.
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74. S. C. Seth and V. D. Agrawal, "Forecasting reject rate of tested LSI chips," *IEEE Electron Device Letters*, vol. EDL-2, pp. 286–287, Nov. 1981.
75. V. D. Agrawal, "Sampling techniques for determining fault coverage in LSI circuits," *J. Digital Syst.*, vol. V, pp. 189–202, Fall 1981.
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Publications – Technical Reports

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2. V. D. Agrawal and W. A. Imbriale, "Dichroic subreflector," Tech. Rep. 76-7323.A4-72, TRW Defense and Space Systems Group, Redondo Beach, California, Sept. 1976.
3. D. T. Shahani and V. D. Agrawal, "An experimental phased array antenna," Tech. Rep. SRS-75-1, School of Radar Studies, Indian Institute of Technology, New Delhi, Jan. 1975.
4. V. D. Agrawal and D. R. Barkhurst, "Vertically polarized dipole evaluation – Final report," Tech. Rep. AL-685, EG&G, Inc., Albuquerque, New Mexico, March 1, 1972.
5. V. D. Agrawal and Y. T. Lo, "Mutual coupling in phased arrays of randomly spaced antennas," Antenna Lab. Report No. 71-1, University of Illinois, Urbana, Illinois, 1971.

Publications – Book Reviews and Forewords

1. Foreword in the book, *Soft Errors in Modern Electronic Systems*, First edition, M. Nicolaidis (Editor), Springer, 2011.
2. Foreword in the book, *Advances in Electronic Testing: Challenges and Methodologies*, D. Gizopoulos (Editor), Springer, 2006.

3. Preface in the book, *Analog and Mixed-Signal Boundary-Scan, A Guide to the IEEE 1149.4 Test Standard*, A. Osseiran (Editor), Kluwer Academic Publishers, Boston, 1999.
4. Foreword in the book, *Delay Fault Testing for VLSI Circuits*, A. Krstić and K.-T. Cheng, Kluwer Academic Publishers, Boston, 1998.
5. Foreword in the book, *On-Line Testing for VLSI*, M. Nicolaidis, Y. Zorian and D. K. Pradhan (editors), Kluwer Academic Publishers, Boston, 1998.
6. Foreword in the book, *Defect Oriented Testing for CMOS Analog and Digital Circuits*, M. Sachdev, Kluwer Academic Publishers, Boston, 1998.
7. Foreword in the book, *Multi-Chip Module Test Strategies*, Y. Zorian, Kluwer Academic Publishers, Boston, 1997.
8. Foreword in the text-book, *Testing and Testable Design of High-Density Random-Access Memories*, P. Mazumder and K. Chakraborty, Kluwer Academic Publishers, Boston, 1996.
9. Foreword in the book, *From Contamination to Defects, Faults and Yield Loss*, J. Khare and W. Maly, Kluwer Academic Publishers, Boston, 1996.
10. Foreword in the book, *Efficient Branch and Bound Search with Application to Computer-Aided Design*, X. Chen and M. L. Bushnell, Kluwer Academic Publishers, Boston, 1996.
11. Preface in the book, *Test Economics and Design for Testability*, C. Dislis, J. Dick, I. D. Dear and A. P. Ambler, Ellis Horwood, UK, 1994.
12. Foreword in the book, *Economics of Electronic Design, Manufacture and Test*, M. Abadir and T. Ambler, Kluwer Academic Publishers, Boston, 1994.
13. Foreword in the book, *IDDQ Testing of VLSI Circuits*, R. K. Gulati and C. F. Hawkins, Kluwer Academic Publishers, Boston, 1993.
14. Book Review: *Introduction to Adaptive Arrays*, R. A. Monzingo and T. W. Miller, New York: Wiley-Interscience, 1980, 543 pages, reviewed for *IEEE Antennas and Propagation Society Newsletter*, Vol. 23, pp. 37-38, August 1981.

Invited Talks – Keynote and Plenary

1. “Testing for Faults, Looking for Defects,” *Keynote Talk, Twelfth IEEE Latin-American Test Workshop*, Porto de Galinhas, Brazil, March 28, 2011.
2. “Interdisciplinary Computer Engineering Curriculum,” *Keynote Address, Sixth VLSI Design and Test Workshops, Education Day*, Bangalore, India, August 29, 2002.
3. “Testing in the Fourth Dimension,” *Keynote Address, Ninth Asian Test Symp.*, Taipei, Taiwan, December 4-6, 2000.
4. “Core Testing and the Core of Testing,” *Plenary Talk, International Test Conference*, Washington, D.C., October 1998.
5. “Science, Technology and the Indian Society,” *Keynote Address, 8th International Conference on VLSI Design*, New Delhi, India, January 1995.
6. “A Tale of Two Designs – the Cheapest and the Most Economical,” *Keynote Address, Second International Workshop on Design, Test and Manufacturing*, Austin, TX, May 1993.

7. "Technology Forecast and Weather Prediction," *Keynote Address, Second Great Lakes Symp. on VLSI*, Kalamazoo, Michigan, February 1992.
8. "Design and Test – The Two Sides of a Coin," *Design & Test Plenary Talk, International Conf. on Computer Design*, Boston, October 1991.
9. "Testability and Productivity – The Merging of the Two Goals," *Design & Test Keynote, TECH-CON'88 SRC Conf.*, Dallas, Texas, October 1988.

Invited Talks – Universities

1. New York University - Abu Dhabi, April 15, 2011, Title: *Testing for Faults, Looking for Defects*.
2. Virginia Tech, June 2, 2009, Title: *Diagnostic Test Generation*.
3. Rutgers University, ECE Distinguished Lecture Series, March 30, 2005, Title: *Implication Graphs and Logic Testing*.
4. Pennsylvania State University, June 20, 2003, Title: *Minimum Dynamic Power CMOS Circuits*.
5. City College of City University of New York, May 28, 2003, Title: *Minimum Dynamic Power CMOS Circuits*.
6. University of New Mexico, April 10, 2003, Title: *Minimum Dynamic Power CMOS Circuits*.
7. University of Illinois at Urbana-Champaign, April 3, 2003, Title: *Hierarchical Fault Collapsing – Functional Equivalences and Dominances*.
8. Temple University, February 12, 2003, Title: *Minimum Dynamic Power CMOS Circuits*.
9. University of Maryland Baltimore County, December 11, 2002, Title: *Minimum Dynamic Power CMOS Circuits*.
10. Yale University, Dec 4, 2002, Title: *Minimum Dynamic Power CMOS Circuits*.
11. Rutgers University, Dept. of ECE, Oct. 5, 2001, Title: *Partial Scan Design with Guaranteed Combinational ATPG*.
12. New Jersey Institute of Technology, Dept. of ECE, Sep. 26, 2001, Title: *Stratified Sampling for Fault Coverage of VLSI Systems*.
13. Carnegie Mellon University, Dept. of ECE, Feb. 27, 2001, Title: *Digital Circuit Design for Minimum Transient Energy*.
14. University of Southern California, Dept. of EE - Systems, Feb. 20, 2001, Title: *Digital Circuit Design for Minimum Transient Energy*.
15. National Tsing Hua University (Hsinchu, Taiwan), Dec. 7, 2000, Titles: *High-Level Fault Modeling and Gate-Level Coverage Estimation* and *Path-Delay Fault Simulation and False Path Removal*.
16. Stanford University, Nov. 29, 2000, Title: *High-Level Fault Modeling and Gate-Level Coverage Estimation*.
17. University of California, Berkeley, Dept. of EE&CS, Nov. 28, 2000, Title: *Digital Circuit Design for Minimum Transient Energy*.
18. Princeton University, Dept. of EE, Oct. 30, 2000, Title: *Digital Circuit Design for Minimum Transient Energy*.

19. Indian Institute of Science (Bangalore, India), Jan. 6, 1999, Title: *A Linear Programming Method for Minimum Transient Energy Digital Circuit Design.*
20. Rutgers University (ECE Dept. Seminar), Nov. 6, 1998, Title: *Digital Circuit Design for Minimum Transient Energy and a Linear Programming Method.*
21. University of California, Santa Barbara, May 1996, Title: *A Randomized Algorithm for Verification of Combinational Circuits.*
22. National Chiao Tung University (Hsinchu, Taiwan), Aug. 5-9, 1991, *A Series of Talks on Advanced VLSI Testing Techniques.*
23. Rutgers University, CS Dept., Apr. 1990, Title: *Synthesis for Testability.*
24. Yale University, Nov. 1989, Title: *Synthesis for Testability.*
25. University of Illinois at Urbana-Champaign, April 1988, Title: *Directed Search Leads to New Directions in VLSI Testing.*
26. University of Massachusetts, April 1988, Title: *Directed Search Leads to New Directions in VLSI Testing.*
27. University of California, Berkeley, Dept. of EE&CS, Nov. 1986, Title: *The Joys of Very Large Scale Testing.*
28. University of Nebraska, Dept. of CSE, Nov. 1986, Title: *The Joys of Very Large Scale Testing.*
29. University of Iowa, Dept. of ECE, Apr. 1984, Title: *VLSI Design Verification.*
30. Duke University, Dept. of CS, Mar. 1984, Title: *VLSI Design Verification.*
31. McGill University, Dept. of EE, Nov. 1983, Title: *VLSI Design Verification Through Simulation.*
32. Indian Institute of Technology, New Delhi (India), Aug. 1983, Title: *Computer-Aided Verification of VLSI Designs.*
33. Indian Institute of Technology, Madras (India), Aug. 1983, Title: *Computer-Aided Verification of VLSI Designs.*
34. Indian Institute of Science (Bangalore, India), Aug. 1983, Title: *Computer-Aided Verification of VLSI Designs.*

Invited Talks – Industry and Research Organizations

1. Bangalore, India, Texas Instruments, Jan 12, 2005 and Intel Corp., Jan 13, 2005, Title: *Minimum Dynamic Power Design Using Variable Input Delay CMOS Logic.*
2. Seventeenth International Conference on VLSI Design, January 2004, Title: *A Tutorial on the Emerging Nanotechnology Devices.*
3. IEEE Bangalore Section, August 23, 2002, Titles: 1. *Delay Testing of Digital Circuits*, 2. *High-Speed VLSI Testing with Slow Test Equipment.*
4. Three invited talks: 1. Fault Sampling, 2. Test Generation by Fault Sampling, and 3. VLSI Product Quality and Fault Coverage, delivered at Compaq, Shrewsbury, Massachusetts, September 8, 1998.
5. “Future of Fault Modeling,” Intel Corporation, Folsom, California. *Invited external speech in company’s seminar on electronics manufacturing.* November 1994.

6. "Testing Techniques," invited one-week EKF Seminar at Oslo, Norway, March 1990.
7. "Statistical Testing," NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI, Como, Italy, June-July, 1987.
8. "Threshold-Value Simulation for Guided Test Generation," NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI, Como, Italy, June-July, 1987.
9. "Design For Testability," Hudson Technical Seminar Series, Digital Equipment Corporation, Hudson, MA, May 7, 1985.
10. "TITUS – Testability Implementation and Test-generation Using Scan," Distinguished Speaker Seminar Series, Microelectronics Center of North Carolina, Research Triangle Park, N.C., November 20, 1984.

Professional Activities – Editorial

1. **Associate Editor (2003 – 2008)**, *IEEE Transactions on VLSI Systems*.
2. **Founder (1990) and Editor-in-Chief (1990 – present)**, *Journal of Electronic Testing: Theory and Applications (JETTA)*. *JETTA is the only peer-reviewed archival journal devoted to the theory and techniques in the area of electronic testing.*
3. **Founder and Consulting Editor (1993 – present)**, *Frontiers in Electronic Testing Book Series*, Kluwer Academic Publishers, Boston. *Series publishes state-of-the-art books on electronic testing. Currently, the series has forty-three volumes including two text-books.*
4. **Editor-in-Chief (1995 – 1997)**, *IEEE Design & Test of Computers*. *A leading IEEE publication in the field of computer hardware; publishes peer-reviewed articles.*
5. **Editor (1984 – 1985)** *Design for Testability, IEEE Design & Test of Computers.*

Professional Activities – Conferences

1. **Program Committee Member**, *Design Automation and Test in Europe (DATE 04)*, Paris, February 16-20, 2004.
2. **Program Committee Member**, *Electronic Design, Test & Applications (DELTA 2004)*, Perth, Australia, January 28-30, 2004.
3. **Program Committee Member**, *IEEE VLSI Test Symposium (VTS)*, 2004.
4. **Program Committee Member**, *7th IEEE VLSI Design & Test Workshops (VDAT'03)*, Bangalore, August 28-30, 2003.
5. **Founder (1985) and Steering Committee Chair (1992 – present)**, *International Conference on VLSI Design*. Now in its sixteenth year, this conference has become a major forum for industry and academia in India. In January 2001, the conference attracted 1,000 attendees. Student fellowship program, that derives funds from the industry and government, is a unique feature of this conference.
6. **Program Chair**, *4th IEEE Asian Test Symposium*, Bangalore, India, November 23-24, 1995.
7. **Publications Chair**, *6th International Conference on VLSI Design*, Bombay, India, January 1993.
8. **General Co-Chair**, *4th CSI/IEEE International Conf. on VLSI Design*, New Delhi, India, January 1991.

9. **Program Committee Member**, *First European Design Automation Conference*, Glasgow, UK, March 1990.
10. **Program Committee Member**, *IFIP WG10.2 Working Conference on the CAD Systems using AI Techniques*, Tokyo, Japan, June 6-7, 1989.
11. **Program Committee Member**, *ACM/IEEE 25th Design Automation Conference*, 1988 and 1989.
12. **Program Committee Member**, *International Test Conference*, 1983, 1984, 1985, 1988 and 1989.
13. **Program Committee Member**, *IEEE Built-In Self Test Workshop*, 1984 and 1985.
14. **Program Committee Member**, *IEEE Design for Testability Workshop*, 1984 and 1985.
15. **Program Committee Member**, *14th Fault Tolerant Computing Symposium*, 1984.

Professional Activities – Committees

1. **ECE Department Advisory Board**, City College of New York, 2003 – present.
2. **Technical Advisory Board**, Center for Embedded System-on-a-Chip Design (CSED), A New Jersey State funded joint research group of NJIT, Princeton and Rutgers, 2000 – present.
3. **Technical Advisory Board**, LogicVision, Inc., San Jose, California (a built-in self-test specialty company), 1999 – present.
4. **ECE Alumni Association**, University of Illinois at Urbana-Champaign, Advisory Board, 2005 – , Board of Directors, 1999 – 2005, Vice-Chair, Eastern Region, 2002 – 2003.
5. **ECE Industrial Advisory Board**, New Jersey Institute of Technology, 1997 – 2001.
6. **IEEE Fellow Selection Committee Chair**, IEEE Computer Society, 1994.
7. **IEEE Fellow Selection Committee**, IEEE Computer Society, 1993.
8. **Board of Governors**, IEEE Computer Society, 1989 and 1990.
9. **Scientific Advisory Board**, Gateway Design Automation Corp., Westford, Massachusetts (a leading electronic simulation and test CAD company that was acquired by Cadence in 1990), 1988 – 1990.
10. **Publications Board**, IEEE Computer Society, 1985 – 1987.
11. **Magazine Advisory Committee**, IEEE Computer Society, 1985 – 1987.
12. **Vice-Chair, Steering Committee**, IEEE Design Automation Standards Subcommittee on Hardware Description Languages, 1984 – 1986.

Professional Activities – Consultation

1. **NSF Design Automation Panel**, Evaluation of research grant proposals on test, Washington, D.C., February 5, 1999.
2. **NSF Workshop** (by invitation), Future Research Directions in Testing of Electronic Circuits and Systems, Santa Barbara, California, May 12-13, 1998.
3. **Reviewer**, New CE Bachelor of Science Degree Program, University of Wisconsin – Madison, 1998.
4. **Consultant Evaluator**, New PhD Program in Computer Engineering, New Jersey Institute of Technology, 1996-1997.

5. **Research Mentor** for Dr. James Jacob of Indian Institute of Science under the United Nations Development Program (UNDP), November 1990 through June 1991.
6. **Consultant**, Central Electronic Engineering Research Institute (CEERI), Pilani (India), and the Indian Telephone Industries, Bangalore, India, under the TOKTEN Program of the United Nations. Three weeks in December 1987.
7. **External Reviewer**, Rapid Prototyping of Electronic Systems Project, Electronics Research Center, GE Corporate R&D Center, Schenectady, NY, July 1989.
8. **Panel of Judges**, SEMMY Award, Semiconductor Equipment and Materials Institute, Inc., 1983.
9. **Referee**, E. W. R. Steacie Fellowship for the Natural Sciences and Engineering Research Council of Canada.

Professional Activities – Teaching

1. **19th IEEE VLSI Test Symposium**: Taught a one-day tutorial on “Essentials of Electronic Testing” jointly with M. L. Bushnell (Rutgers University), Apr. 2001.
2. **Rutgers University**: Taught an “Advanced Electronic Testing Course” (senior and graduate level) in the ECE Dept. jointly with M. L. Bushnell for the past 10 years. 1992 – 2001.
3. **Test Technology Technical Council Educational Program**: Taught a one-day tutorial on “Essentials of Electronic Testing” at Marina-del-Rey, California, with M. L. Bushnell of Rutgers. April 2001.
4. **JN Center for Advanced Scientific Research, Bangalore, India**: Taught a one-week course on “Test Generation and Design for Test of VLSI” to university professors and industry engineers, jointly with J. Jacob (Indian Institute of Science) and S. M. Reddy (University of Iowa.) January 13-17, 1992.
5. **University of Wisconsin-Madison (Extension)**: Taught two-day courses on “Design for Testability and Built-In Self-Test of VLSI Systems” at Stuttgart and Munich, jointly with C. R. Kime and K. K. Saluja. 1987, 1988 and 1990.
6. **IEEE Custom Integrated Circuits Conference Educational Sessions**: Taught a half-day course on “Design for Testability and Advances in Testing.” Boston, 1990.
7. **International Test Conference**: Taught one-day tutorials on “Test Generation for VLSI Chips” jointly with S. C. Seth (University of Nebraska.) 1987 – 1990.
8. **Third International Conference on VLSI Design**: Taught a half-day course on “VLSI Testing and Design for Testability.” Bangalore, India, January 1990.
9. **26th ACM/IEEE Design Automation Conference**: Taught a one-day tutorials on “Introduction to Testing for VLSI Designers” jointly with S. C. Seth. 1989.
10. **First European Test Conference**: Taught a one-day tutorials on “ASIC Test Techniques for Chips and Boards” jointly with S. C. Seth and R. G. Bennetts. Paris, April 1989.
11. **Information Processing Society of Japan**: Taught a one-day tutorials on “AI Applications to CAD” jointly with R. Joobbani and T. J. Kowalski. Tokyo, 1989.

Professional Activities – Research

I have collaborated on master's and doctoral research at various universities. Only the PhD dissertations, indicating my involvement as a member of the *thesis committee* or as a *co-advisor*, are listed below.

1. P. Venkataramani, (in progress), Auburn University, *advisor*.
2. V. B. Sheshadri, (in progress), Auburn University, *co-advisor*.
3. J. Yao, (in progress), Auburn University, *advisor*.
4. S. Sindia, December 2012 (expected), Auburn University, *advisor*.
5. Y. Zhang, December 2011 (expected), Auburn University, *advisor*.
6. Y. Hao, December 2011 (expected), Auburn University, *thesis committee*, advisor: B. Wilamowski.
7. K. Kim, May 2011, Auburn University, *advisor*.
8. W. Jiang, May 2011, Auburn University, *advisor*.
9. L. Lan, May 2011, Auburn University, *thesis committee*, advisor: G. Niu.
10. Q. Jie, December 2010, Auburn University, *thesis committee*, advisors: F. Dai and C. E. Stroud.
11. R. McPherson, December 2010, Auburn University, *thesis committee*, advisor: R. Dean.
12. N. Yogi, August 2009, Auburn University, *advisor*.
13. Y. Lu, August 2007, Auburn University, *advisor*.
14. F. Hu, May 2006, Auburn University, *advisor*.
15. T. Raja, 2004, Rutgers University, *co-advisor*, faculty advisor: M. L. Bushnell.
16. K. N. Dwarakanath, 2003, Carnegie Mellon University, *thesis committee*, faculty advisor: R. D. Blanton.
17. S. Sheng, "Testing and Verification by Exploring Circuit Properties," Rutgers University, 2003, *thesis committee*, faculty advisor: M. S. Hsiao.
18. L. Rao, 2003, Rutgers University, *co-advisor*, faculty advisor: M. L. Bushnell.
19. Y.C. Kim, 2002, University of Wisconsin-Madison, *co-advisor*, faculty advisor: K. K. Saluja.
20. P. Thaker, 2000, George Washington University, *co-advisor*, faculty advisor: M. E. Zaghloul.
21. K. Heragu, 1998, University of Illinois at Urbana-Champaign, *co-advisor*, faculty advisor: J. H. Patel.
22. M. Sivaraman, 1997, Carnegie Mellon University, *thesis committee*, faculty advisor: A. J. Strojwas.
23. A. K. Majhi, 1996, Indian Institute of Science, *co-advisor*, faculty advisors: J. Jacob and L. M. Patnaik.
24. I. P. Shaik, 1996, Rutgers University, *thesis committee*, faculty advisor: M. L. Bushnell.
25. M. A. Gharaybeh, 1996, Rutgers University, *co-advisor*, faculty advisor: M. L. Bushnell.
26. A. Balakrishnan, 1996, Rutgers University, *thesis committee*, advisors: E. Boros (Rutgers-RUTCOR) and S. T. Chakradhar (NEC).
27. S. Bose, 1995, Carnegie Mellon University, *co-advisor*, faculty advisor: W. Maly.

28. M. K. Srinivas, 1994, Indian Institute of Science, *co-advisor*, faculty advisors: J. Jacob and V. Rajaraman.
29. S. Naik, 1994, Carnegie Mellon University, *thesis committee*, faculty advisor: W. Maly.
30. T. J. Chakraborty, 1993, Rutgers University, *co-advisor*, faculty advisor: M. L. Bushnell.
31. S. Kanjilal, 1993, Rutgers University, *co-advisor*, other advisors: M. Murdocca (Rutgers-CS) and S. T. Chakradhar (NEC).
32. X. Chen, 1993, Rutgers University, *thesis committee*, faculty advisor: M. L. Bushnell.
33. S. H. Robinson, 1992, Carnegie Mellon University, *thesis committee*, faculty advisor: J. Shen.
34. D. V. Das, 1992, University of Nebraska, *co-advisor*, faculty advisor: S. C. Seth.
35. J. Giraldi, 1990, Rutgers University, *thesis committee*, faculty advisor: M. L. Bushnell.
36. S. T. Chakradhar, 1990, Rutgers University, *co-advisor*, faculty advisor: M. L. Bushnell.
37. V. G. Karkare, 1989, University of Poona (India), *thesis committee*, faculty advisor: S. K. David.
38. H. A. Farhat, 1988, University of Nebraska, *co-advisor*, faculty advisor: S. C. Seth.
39. K.-T. Cheng, 1988, University of California, Berkeley, *co-advisor*, faculty advisor: E. S. Kuh.
40. R. Sivaswamy, 1979, Indian Institute of Science, *thesis committee*, faculty advisor: N. S. Nagaraja.

Technology Transfer

During the last thirty years my research has been on VLSI testing. Those who have used my work can be grouped in three categories:

1. **My Company:** Algorithms for built-in self-test, delay testing, partial-scan, scan design optimization, and timing analysis have been implemented into CAD tools that support VLSI design in the company. Recently, the method of path-status graph was used in a unique program (perhaps the only one in the industry today) to simulate path delay faults in non-scan sequential circuits.
2. **Industry:** The method of VLSI product quality (defect level) assessment from fault coverage has been studied by semiconductor manufacturers like Intel and Conexant, and board makers like Western Digital. The paper on fault sampling is widely used by many companies. The statistical fault analysis (STAFAN) algorithm has been implemented and used by companies like IBM. The cycle-breaking algorithm for partial-scan is used in CAD products of Sunrise and other companies. NEC has implemented the transitive closure method into a very efficient test generation program.
3. **Universities:** The idea of directed-search to enhance test generation was used by university researchers at Illinois and Torino in their work on genetic algorithms. Motivated by the cycle-breaking method of partial-scan, papers have been published by researchers from Illinois, Iowa, Technion and Yale on efficient minimum feedback vertex set (MFVS) solutions. Extensions of research on “hazard elimination for low-power” and “spectral analysis for test” have been funded at Rutgers by the National Science Foundation.

Funded Research

1. **Low-Power System-on-a-Chip Design for Minimum Transient Energy**, M. L. Bushnell and V. D. Agrawal, NSF Award #9988239, Sep. 1, 2000 through Aug 31, 2003, \$131,776.
2. **Digital Spectral Analysis for Mixed-Signal System-on-a-Chip Testing**, M. L. Bushnell, V. D. Agrawal and M. S. Hsiao, NSF Award #0098304, April 1, 2001 through March 31, 2004, \$513,522.
3. **Spectral Built-In Self-Testing for Mixed-Signal Systems-in-a-Package (SIP)**, M. L. Bushnell and V. D. Agrawal, NSF Award #0429743, Sep. 1, 2004 through Aug 31, 2007, \$300,000.
4. **Gift from NEC Corp. to support my research**, October 2004, \$30,000.
5. **Gift from Intel Corp. for research on “High-Level Fault Coverage Evaluation,”** One student supported for three years starting October 2004.
6. **Collaborative Research: CRI: IAD: Electronic Testing Education, Research and Training Infrastructure**, NSF-CNS-0708962, Oct 1, 2007 through Sep 30, 2010, extended to Sep 30, 2011, \$1,099,896 (Auburn \$599,995, UAH \$157,141, UA \$173,677, Tuskegee \$169,083).
7. **Collaborative Research: CRI: IAD: Electronic Testing Education, Research and Training Infrastructure**, NSF-CNS-0708962, REU Supplement, Oct 1, 2009 through Sep 30, 2010, extended to Sep 30, 2011, \$43,000.
8. **I/UCRC: Wireless Research Center for Cross-Layer Optimization of Coexisting Systems**, NSF-IIP-0738088, Aug 1, 2007 through July 31, 2012, \$734,959.
9. **SHF: Small: Methods for Diagnosis of Non-Classical Faults in Digital Circuits**, NSF-CCF-1116213, Aug 1, 2011 through July 31, 2014, \$299,999.
10. **CRI-II-NEW: Collaborative Research: Radio Frequency Test Education and Research**, NSF-CNS-1205429, submitted Oct 25, \$892,570 (Auburn \$646,941, Alabama \$245,629).
11. **SHF: Small: Adaptive Methods for Power Constrained Testing**, NSF-CCF-1219018, submitted Dec 19, 2011, \$274,201.