

# List of Publications

Vishwani D. Agrawal

October 3, 2009

- [1] V. K. Jain and V. D. Agrawal, "Directional loudspeaker system for a big hall," *J.I.T.E. (India)*, vol. 12, pp. 29–35, Jan. 1966.
- [2] S. K. Chatterjee, V. D. Agrawal, and R. Chatterjee, "Reactance modulated dielectric rod waveguide," *J.I.E. (India)*, vol. 43, Part ET2, pp. 103–114, 1968.
- [3] Y. T. Lo and V. D. Agrawal, "Removal of blindness in phased arrays," *Proc. IEEE*, vol. 56, pp. 1586–1588, Sept. 1968.
- [4] V. D. Agrawal and Y. T. Lo, "Distribution of sidelobe level in random arrays," *Proc. IEEE*, vol. 57, pp. 1764–1765, Oct. 1969.
- [5] Y. T. Lo, V. D. Agrawal, and A. R. Panicali, "A review of the theory of random arrays with some recent results," in *Proc. 4th Colloquium on Microwave Communication*, (Budapest, Hungary), Apr. 1970.
- [6] V. D. Agrawal and D. R. Barkhurst, "Vertically polarized dipole evaluation – Final report," Tech. Rep. AL-685, EG&G, Inc., Albuquerque, New Mexico, March 1, 1972.
- [7] V. D. Agrawal and Y. T. Lo, "Mutual coupling in phased arrays of randomly spaced antennas," *IEEE Trans. Antennas and Propagation*, vol. AP-20, pp. 288–295, May 1972. Also Antenna Lab. Report No. 71-1, University of Illinois, Urbana, Illinois.
- [8] V. D. Agrawal and Y. T. Lo, "Anomalies of dielectric coated gratings," *Applied Optics*, vol. 11, pp. 1946–1951, Sept. 1972.
- [9] V. D. Agrawal and P. Agrawal, "An automatic test generation system for Illiac IV logic boards," *IEEE Trans. Comput.*, vol. C-21, pp. 1015–1017, Sept. 1972.
- [10] V. D. Agrawal, "A novel technique of electronic scanning," in *Proc. Symposium on Sonar Systems and Ultrasonics*, Indian Institute of Technology, New Delhi, May 3-5, 1973.

- [11] V. D. Agrawal and R. K. Arora, "Scanning transients in phased array antennas," *Proc. IEEE*, vol. 62, pp. 850–851, June 1974.
- [12] R. K. Arora and V. D. Agrawal, "Frequency-spread associated with fast electronic scanning," *Proc. IEEE*, vol. 62, pp. 1175–1176, Aug. 1974.
- [13] V. D. Agrawal, "Comments on beamwidth of phased arrays," *IEEE Trans. Ant. Prop.*, vol. AP-22, pp. 841–842, Nov. 1974.
- [14] D. T. Shahani and V. D. Agrawal, "An experimental phased array antenna," Tech. Rep. SRS-75-1, School of Radar Studies, Indian Institute of Technology, New Delhi, Jan. 1975.
- [15] P. Agrawal and V. D. Agrawal, "On improving the efficiency of monte carlo test generation," in *Digest of Fifth Int. Fault Tolerant Computing Symposium*, (Paris, France), pp. 205–209, June 18-20, 1975.
- [16] P. Agrawal and V. D. Agrawal, "Probabilistic analysis of random test generation method for irredundant combinational networks," *IEEE Trans. Comput.*, vol. C-24, pp. 691–695, July 1975.
- [17] P. Agrawal and V. D. Agrawal, "On monte carlo testing of logic tree networks," *IEEE Trans. Comput.*, vol. C-25, pp. 664–667, June 1976.
- [18] V. D. Agrawal and W. A. Imbriale, "Dichroic subreflector," Tech. Rep. 76-7323.A4-72, TRW Defense and Space Systems Group, Redondo Beach, California, Sept. 1976.
- [19] V. D. Agrawal and W. A. Imbriale, "Experimental and theoretical design of dichroic surface for a spacecraft antenna," in *Proc. IEEE Int. AP-S Symp.*, (Amherst, MA), pp. 105–108, Oct. 1976.
- [20] V. D. Agrawal and W. A. Imbriale, "Analysis of frequency selective surfaces printed on dielectric sheet," in *Proc. IEEE Int. AP-S Symp.*, (Palo Alto, CA), June 1977.
- [21] V. D. Agrawal and G. G. Wong, "Helix antenna for multiple access array of TDRSS spacecraft," Tech. Rep. TDRSS-77-331-107, TRW Defense and Space Systems Group, Redondo Beach, California, Dec. 1977.
- [22] V. D. Agrawal, "Grating lobe suppression in phased arrays by subarray rotation," *Proc. IEEE*, vol. 66, pp. 347–349, Mar. 1978.
- [23] V. D. Agrawal and T. C. Tong, "Grating lobe suppression in multiple access array of TDRSS spacecraft," in *IEEE Int. AP-S Symp. Digest*, (Washington, D.C.), pp. 178–181, May 1978.
- [24] V. D. Agrawal, "Selection of element for a scanned array antenna," *Archiv fur Elektronik und Ubertragungstechnik (AEU)*, vol. 32, pp. 493–495, Nov. 1978.

- [25] V. D. Agrawal, "When to use random testing," *IEEE Trans. Comput.*, vol. C-27, pp. 1054–1055, Nov. 1978.
- [26] V. D. Agrawal, "Electrostatic analog for finding nonintersecting paths," *IETE Student's Journal (India)*, vol. 20, pp. 3–7, Jan. 1979.
- [27] V. D. Agrawal and G. G. Wong, "A high performance helical element for multiple access array on TDRSS spacecraft," in *IEEE Int. AP-S Symp. Digest*, (Seattle, Washington), pp. 481–484, June 1979.
- [28] V. D. Agrawal and W. A. Imbriale, "Design of a dichroic cassegrain sub-reflector," *IEEE Trans. Ant. Prop.*, vol. AP-27, pp. 466–473, July 1979.
- [29] V. D. Agrawal, "Authors reply to comments on when to use random testing," *IEEE Trans. Comput.*, vol. C-28, p. 581, Aug. 1979.
- [30] V. D. Agrawal, "Comments on an approach to highly integrated, computer maintained cellular arrays," *IEEE Trans. Comput.*, vol. C-28, pp. 691–693, Sept. 1979.
- [31] V. D. Agrawal, A. K. Bose, P. Kozak, H. N. Nham, and E. Pacas-Skewes, "A mixed-mode simulator," in *Proc. 17th Des. Auto. Conf.*, (Minneapolis, Minnesota), pp. 618–625, June 23–25, 1980.
- [32] V. D. Agrawal, "Information theory in digital testing – A new approach to functional test pattern generation," in *Proc. Int. Conf. Cir. Comput.*, (Port Chester, N.Y.), pp. 928–931, October 1–3, 1980.
- [33] V. D. Agrawal, "Random test generation – A tutorial," in *Proc. Bell Syst. Conf. on Electronic Testing*, (Princeton, N.J.), pp. 9–11, October 14–16, 1980.
- [34] V. D. Agrawal and Y. T. Lo, "Comments on characterization of the random array peak sidelobes," *IEEE Trans. Ant. Prop.*, vol. AP-28, pp. 946–948, Nov. 1980.
- [35] V. D. Agrawal, S. C. Seth, and P. Agrawal, "LSI product quality and fault coverage," in *Proc. 18th Des. Auto. Conf.*, (Nashville, TN), pp. 196–203, June 29–July 1, 1981.
- [36] V. D. Agrawal, "An information theoretic approach to digital testing," *IEEE Trans. Comput.*, vol. C-30, pp. 582–587, Aug. 1981.
- [37] M. R. Mercer, V. D. Agrawal, and C. M. Roman, "An LSI chip designed for testability," in *Proc. Bell System Conference on Electronic Testing*, (Princeton, N.J.), Sept. 1981.
- [38] V. D. Agrawal, "Sampling techniques for determining fault coverage in LSI circuits," *J. Digital Syst.*, vol. V, pp. 189–202, Fall 1981.

- [39] V. D. Agrawal, "Emerging roles of VLSI testing," in *Proc. SEMI-CON/Southwest*, (Dallas, Texas), October 13-14, 1981.
- [40] M. R. Mercer, V. D. Agrawal, and C. M. Roman, "Test generation for highly sequential scan-testable circuits through logic transformation,," in *Proc. International Test Conference*, (Philadelphia, PA), pp. 561-565, October 27-29, 1981.
- [41] S. C. Seth and V. D. Agrawal, "Forecasting reject rate of tested LSI chips," *IEEE Electron Device Letters*, vol. EDL-2, pp. 286-287, Nov. 1981.
- [42] V. D. Agrawal, A. K. Bose, P. Kozak, H. N. Nham, and E. Pacas-Skewes, "Mixed-mode simulation in the MOTIS system," *J. Digital Syst.*, vol. V, pp. 383-400, Winter 1981.
- [43] V. D. Agrawal, S. C. Seth, and P. Agrawal, "Fault coverage requirements in production testing of LSI circuits," *IEEE J. Sol. St. Circ.*, vol. SC-17, pp. 57-61, Feb. 1982.
- [44] M. R. Mercer and V. D. Agrawal, "Testability strategies for custom polycell designs," in *Computer Elements Workshop*, (New York, N.Y.), May 21-22 1982.
- [45] V. D. Agrawal, "Synchronous path analysis in MOS circuit simulator," in *Proc. 19th Des. Auto. Conf.*, (Las Vegas, Nevada), pp. 629-635, June 14-16, 1982.
- [46] S. C. Seth and V. D. Agrawal, "Statistical design verification," *12th Int. Fault Tolerant Computing Symp.*, June 22-24, 1982. Digest of Papers pp. 393-399.
- [47] M. R. Mercer and V. D. Agrawal, "Applications of testability measures in VLSI design," in *Proc. Bell System Conference on Electronic Testing*, (Princeton, N.J.), pp. 52-58, October 5-7 1982.
- [48] V. D. Agrawal and M. R. Mercer, "Testability measures - What do they tell us?," *Proc. Int. Test Conf.*, pp. 391-396, November 16-18, 1982.
- [49] S. K. Jain and V. D. Agrawal, "Statistical fault analysis - A technique for estimating fault coverage through good circuit simulation," in *IEEE Design for Testability Workshop*, (Vail, CO), April 12-14 1983.
- [50] S. K. Jain and V. D. Agrawal, "Test generation for MOS circuits using D-algorithm," in *Proc. 20th Des. Auto. Conf.*, (Miami Beach, Florida), pp. 64-70, June 1983.
- [51] V. D. Agrawal, S. K. Jain, and D. M. Singer, "Design for testability - Tutorial," in *Proc. Bell Syst. Conf. on Electronic Testing*, (Princeton, N.J.), Oct. 1983.

- [52] S. C. Seth and V. D. Agrawal, "Characterizing the LSI yield equation from chip test data," in *Proc. Int. Conf. Circ. Comp.*, (New York, N.Y.), pp. 556–559, Sept. 28-Oct. 1, 1982. Also *IEEE Trans. CAD* Vol. CAD-3, pp. 123-126, April 1984.
- [53] M. R. Mercer and V. D. Agrawal, "A novel clocking technique for VLSI circuit testability," *IEEE J. Sol. St. Circ.*, vol. SC-19, pp. 207–212, Apr. 1984.
- [54] S. K. Jain, M. Weisel, and V. D. Agrawal, "Scan overhead optimization in standard cell design," in *IEEE Design for Testability Workshop*, (Vail, CO), April 24-26 1984.
- [55] V. D. Agrawal, S. K. Jain, and D. M. Singer, "Automation in design for testability," in *Custom Integrated Circuits Conf.*, (Rochester, N.Y.), pp. 159–163, May 21-23, 1984.
- [56] S. M. Reddy, M. K. Reddy, and V. D. Agrawal, "Robust tests for stuck-open faults in CMOS combinational logic circuits," in *Proc. 14th Int. Fault Tolerant Comp. Symp.*, (Kissimmee, Florida), pp. 44–49, June 20-22, 1984.
- [57] S. K. Jain and V. D. Agrawal, "STAFAN: An alternative to fault simulation," in *Proc. ACM IEEE 21st Des. Auto. Conf.*, (Albuquerque, N.M.), pp. 18–23, June 25-27, 1984.
- [58] A. E. Dunlop, V. D. Agrawal, D. N. Deutsch, M. F. Jukl, P. Kozak, and M. Wiesel, "Chip layout optimization using critical path weighting," in *Proc. ACM IEEE 21st Des. Auto. Conf.*, (Albuquerque, N.M.), pp. 133–136, June 25-27, 1984.
- [59] S. M. Reddy, V. D. Agrawal, and S. K. Jain, "A gate level model for CMOS combinational logic circuits with application to fault detection," in *Proc. ACM IEEE 21st Des. Auto. Conf.*, (Albuquerque, N.M.), pp. 504–509, June 25-27, 1984.
- [60] V. D. Agrawal, S. K. Jain, and D. M. Singer, "A CAD system for design for testability," *VLSI Design*, vol. V, pp. 46–54, Oct. 1984.
- [61] V. D. Agrawal, "Will testability analysis replace fault simulation - A panel discussion," in *Proc. Int. Test Conf.*, (Philadelphia, PA), Oct. 1984.
- [62] V. D. Agrawal, "Computer-aids in VLSI design," in *Proc. IEEE Int. Conf. on Computers, Systems and Signal Processing*, (Bangalore, India), December 10-12, 1984.
- [63] S. K. Jain and V. D. Agrawal, "Statistical fault analysis," *IEEE Design & Test of Computers*, vol. 2, pp. 38–44, Feb. 1985.
- [64] V. D. Agrawal and S. H. C. Poon, "VLSI design process," in *Proc. ACM Computer Science Conference*, (New Orleans, Louisiana), pp. 74–78, March 12-14, 1985.

- [65] S. C. Seth and V. D. Agrawal, "Cutting chip testing costs," *IEEE Spectrum*, vol. 22, pp. 38–45, Apr. 1985.
- [66] S. K. Jain and V. D. Agrawal, "Modeling and test generation algorithms for MOS circuits," *IEEE Trans. Comput.*, vol. C-34, pp. 426–433, May 1985.
- [67] V. D. Agrawal, S. C. Seth, and C. C. Chuang, "Probabilistically guided test generation," in *Proc. Int. Symp. on Circuits and Systems*, (Kyoto, Japan), pp. 687–690, June 1985.
- [68] S. C. Seth, L. Pan, and V. D. Agrawal, "PREDICT - probabilistic estimation of digital circuit testability," in *Proc. Fault Tolerant Computing Symposium*, (Ann Arbor, Michigan), pp. 220–225, June 19–21, 1985.
- [69] P. Agrawal, V. D. Agrawal, and N. N. Biswas, "Multiple output minimization," in *Proc. 22nd Design Automation Conference*, (Las Vegas, Nevada), pp. 674–680, June 24–26, 1985.
- [70] S. K. Jain and V. D. Agrawal, "Clarifying statistical fault analysis – Authors' reply," *IEEE Design & Test of Computers*, vol. 2, pp. 7–8, Aug. 1985.
- [71] V. D. Agrawal and S. C. Seth, "Probabilistic testability," in *Proc. Int. Conf. on Computer Design*, (Port Chester, NY), pp. 562–565, Oct. 1985.
- [72] V. D. Agrawal, "Stafan takes a middle course (position statement)," in *Proc. International Test Conference*, (Philadelphia, PA), Nov. 1985.
- [73] S. C. Seth and V. D. Agrawal, "A review of testing of VLSI devices," *IETE Tech. Review*, vol. 1, pp. 363–374, Nov. 1985.
- [74] V. D. Agrawal, "VLSI testing," in *Proc. First International Workshop on VLSI Design*, (Madras, India), December 18–26 1985.
- [75] S. C. Seth, B. B. Bhattacharya, and V. D. Agrawal, "An exact analysis for efficient computation of random-pattern testability in combinational circuits," in *Proc. Fault Tolerant Computing Symposium*, (Vienna, Austria), pp. 318–323, July 1–3, 1986.
- [76] T. Lin and V. D. Agrawal, "A test generator for scan-design VLSI circuits," in *Proc. AT&T Conference on Electronic Testing*, (Jamesburg, NJ), pp. 23.1–23.7, Sept. 1986.
- [77] V. D. Agrawal and D. D. Johnson, "Logic modeling of PLA faults," in *Proc. Int. Conf. on Computer Design*, (Port Chester, NY), pp. 86–88, Oct. 1986.
- [78] N. C. E. Srinivas and V. D. Agrawal, "PROVE: Prolog based verifier," in *Proc. Int. Conf. on Computer-Aided Design*, (Santa Clara, CA), pp. 306–309, Nov. 1986.

- [79] V. D. Agrawal, K. T. Cheng, D. D. Johnson, and T. Lin, "A complete solution to the partial scan problem," in *Proc. Int. Test Conference*, (Washington, D.C.), pp. 44–51, Sept. 1987.
- [80] V. D. Agrawal and K. T. Cheng, "A simulation-based directed search method for test generation," in *Proc. Int. Conf. on Computer Design (ICCD)*, (Port Chester, NY), pp. 48–51, Oct. 1987.
- [81] V. D. Agrawal, K. T. Cheng, and P. Agrawal, "Use of a concurrent fault simulator for test vector generation," in *Proc. AT&T Conf. on Electronic Testing*, (Princeton, NJ), pp. 23–28, Oct. 1987.
- [82] N. C. E. Srinivas and V. D. Agrawal, "Formal verification of digital circuits using hybrid simulation," *Circuits and Devices*, vol. 4, pp. 19–27, Jan. 1988.
- [83] V. D. Agrawal, K. T. Cheng, D. D. Johnson, and T. Lin, "Designing circuits with partial scan," *IEEE Design & Test of Computers*, vol. 5, pp. 8–15, Apr. 1988.
- [84] V. D. Agrawal, "Statistical testing," in *Testing and Diagnosis of VLSI and ULSI* (F. Lombardi and M. Sami, eds.), pp. 33–47, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1988.
- [85] V. D. Agrawal and K. T. Cheng, "Threshold-value simulation and test generation," in *Testing and Diagnosis of VLSI and ULSI* (F. Lombardi and M. Sami, eds.), pp. 311–323, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1988.
- [86] V. D. Agrawal, K. T. Cheng, and P. Agrawal, "CONTEST: A concurrent test generator for sequential circuits," in *Proc. Des. Auto. Conf.*, (Anaheim, CA), pp. 84–89, June 1988.
- [87] K. T. Cheng, V. D. Agrawal, and E. S. Kuh, "A sequential circuit test generator using threshold-value simulation," in *Digest of Papers, Fault-Tolerant Computing Symposium (FTCS-18)*, (Tokyo, Japan), pp. 24–29, June 1988.
- [88] V. D. Agrawal and S. C. Seth, *Test Generation for VLSI Chips*. Los Alamitos, CA: IEEE Computer Society Press, 1988.
- [89] V. D. Agrawal, H. Farhat, and S. C. Seth, "Test generation by fault sampling," in *Proc. Int. Conf. on Computer Design (ICCD-88)*, (Rye Brook, NY), pp. 58–61, Oct. 1988.
- [90] V. D. Agrawal, "Testability and productivity - the merging of the two goals," in *Proc. TECHCON'88 (An SRC Conference)*, (Dallas, TX), pp. 137–140, Oct. 1988.

- [91] V. D. Agrawal and S. C. Seth, "On a relationship between fault coverage and circuit testability," in *Proc. AT&T Conf. Electronic Testing*, (Princeton, NJ), pp. 16.1–16.6, Oct. 1988.
- [92] P. Agrawal, V. D. Agrawal, and K. T. Cheng, "Fault simulation in MARS," in *Proc. AT&T Conf. Electronic Testing*, (Princeton, NJ), pp. 40.1–40.9, Oct. 1988.
- [93] S. T. Chakradhar, M. L. Bushnell, and V. D. Agrawal, "Automatic test generation using neural networks," in *Proc. Int. Conf. on Computer-Aided Design (ICCAD-88)*, (Santa Clara, CA), pp. 416–419, Nov. 1988.
- [94] S. C. Seth and V. D. Agrawal, "On the probability of fault occurrence," in *Defect and Fault Tolerance in VLSI Systems* (I. Koren, ed.), pp. 47–52, Plenum Publishing Corp., 1989.
- [95] V. D. Agrawal and S. M. Reddy, "Fault modeling and test generation," in *VLSI Handbook* (J. DiGiacomo, ed.), p. Chapter 8, New York: McGraw-Hill, 1989.
- [96] V. D. Agrawal, "Design automation, expert opinion," *IEEE Spectrum*, vol. 26, pp. 36–37, Jan. 1989.
- [97] V. D. Agrawal, K. T. Cheng, and P. Agrawal, "A directed search method for test generation using a concurrent simulator," *IEEE Trans. on Computer-Aided Design*, vol. 8, pp. 131–138, Feb. 1989.
- [98] S. C. Seth, V. D. Agrawal, and H. Farhat, "A theory of testability with application to fault coverage analysis," in *Proc. European Test Conference*, (Paris, France), pp. 139–143, Apr. 1989.
- [99] S. C. Seth and V. D. Agrawal, "A new model for computation of probabilistic testability in combinational circuits," *INTEGRATION, The VLSI Journal*, vol. 7, pp. 49–75, 1989.
- [100] K. T. Cheng and V. D. Agrawal, "Concurrent test generation and design for testability," in *Proc. Int. Symp. Circ. Syst. (ISCAS)*, (Portland, Oregon), pp. 1935–1938, May 1989.
- [101] K. T. Cheng and V. D. Agrawal, *Unified Methods for VLSI Simulation and Test Generation*. Boston: Kluwer Academic Publishers, 1989.
- [102] K. T. Cheng and V. D. Agrawal, "An economical scan design for sequential logic test generation," in *Proc. 19th Fault-Tolerant Computing Symposium (FTCS-19)*, pp. 28–35, June 1989.
- [103] P. Agrawal, V. D. Agrawal, K. T. Cheng, and R. Tutundjian, "Fault simulation in a pipelined multiprocessor system," in *Proc. Int. Test Conf.*, (Washington, DC), pp. 727–734, Aug. 1989.

- [104] K. T. Cheng and V. D. Agrawal, "State assignment for initializable synthesis," in *Proc. Int. Conf. Computer-Aided Design (ICCAD-89)*, (Santa Clara, CA), pp. 212–215, Nov. 1989.
- [105] K. T. Cheng and V. D. Agrawal, "Design of sequential machines for efficient test generation," in *Proc. Int. Conf. Computer-Aided Design (ICCAD-89)*, (Santa Clara, CA), pp. 358–361, Nov. 1989.
- [106] V. D. Agrawal and K. T. Cheng, "An architecture for synthesis of testable finite state machines," in *Proc. First European Design Automation Conference*, (Glasgow, UK), pp. 612–616, Mar. 1990.
- [107] K. T. Cheng and V. D. Agrawal, "A partial scan method for sequential circuits with feedback," *IEEE Trans. Comput.*, vol. 39, pp. 544–548, Apr. 1990.
- [108] S. C. Seth, V. D. Agrawal, and H. Farhat, "A statistical theory of digital circuit testability," *IEEE Trans. Comput.*, vol. 39, pp. 582–586, Apr. 1990.
- [109] P. Agrawal and V. D. Agrawal, "Can logic simulators handle bidirectionality and charge sharing?," in *Proc. Int. Symp. Circ. Syst. (ISCAS)*, (New Orleans), pp. 411–414, May 1990.
- [110] K. T. Cheng and V. D. Agrawal, "Synthesis of testable finite state machines," in *Proc. Int. Symp. Circ. Syst. (ISCAS)*, (New Orleans), pp. 3114–3117, May 1990.
- [111] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Automatic test generation using quadratic 0-1 programming," in *Proc. 27th ACM/IEEE Des. Autom. Conf.*, (Orlando, FL), pp. 654–659, June 1990.
- [112] V. D. Agrawal and K. T. Cheng, "Test function specification in synthesis," in *Proc. 27th ACM/IEEE Des. Autom. Conf.*, (Orlando, FL), pp. 235–240, June 1990.
- [113] K. T. Cheng and V. D. Agrawal, "An entropy measure for the complexity of multi-output Boolean functions," in *Proc. 27th ACM/IEEE Des. Autom. Conf.*, (Orlando, FL), pp. 302–305, June 1990.
- [114] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Polynomial time solvable fault detection problems," in *Proc. 20th Fault-Tolerant Computing Symposium (FTCS-20)*, (Newcastle-upon-Tyne, UK), pp. 56–63, June 1990.
- [115] V. D. Agrawal and H. Kato, "Fault sampling revisited," *IEEE Design & Test of Computers*, vol. 7, pp. 32–35, Aug. 1990.
- [116] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Toward massively parallel automatic test generation," *IEEE Trans. CAD*, vol. 9, pp. 981–994, Sept. 1990.

- [117] D. V. Das, S. C. Seth, P. T. Wagner, J. C. Anderson, and V. D. Agrawal, "An experimental study on reject ratio prediction for VLSI circuits: Kokomo revisited," in *Proc. Int. Test Conf.*, pp. 712–720, Sept. 1990.
- [118] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Neural net and Boolean satisfiability models of logic circuits," *IEEE Design & Test of Computers*, vol. 7, pp. 54–57, Oct. 1990.
- [119] V. D. Agrawal and K. T. Cheng, "Finite state machine synthesis with embedded test function," *J. Electronic Testing: Theory and Applications (JETTA)*, vol. 1, no. 3, pp. 221–228, 1990.
- [120] V. D. Agrawal and S. T. Chakradhar, "Statistical performance of a parallel processing system," in *Proc. ISMM Int. Conf. on Parallel and Distributed Computing and Systems*, pp. 212–216, Oct. 1990.
- [121] V. D. Agrawal and S. T. Chakradhar, "Logic simulation and parallel processing," in *Proc. Int. Conf. on CAD (ICCAD)*, pp. 496–499, Nov. 1990.
- [122] V. D. Agrawal and S. T. Chakradhar, "Performance estimation in a massively parallel system," in *Proc. Supercomputing '90*, pp. 306–313, Nov. 1990.
- [123] K. T. Cheng, V. D. Agrawal, and E. S. Kuh, "A simulation-based method for generating tests for sequential circuits," *IEEE Trans. on Computers*, vol. 39, pp. 1456–1463, Dec. 1990.
- [124] V. D. Agrawal, S. C. Seth, and J. S. Deogun, "Design for testability and test generation with two clocks," in *Proc. 4th CSI/IEEE International Symp. on VLSI Design*, pp. 112–117, Jan. 1991.
- [125] S. T. Chakradhar and V. D. Agrawal, "A novel VLSI solution to a difficult graph problem," in *Proc. 4th CSI/IEEE International Symp. on VLSI Design*, pp. 124–129, Jan. 1991.
- [126] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, *Neural Models and Algorithms for Digital Testing*. Boston: Kluwer Academic Publishers, 1991.
- [127] K. T. Cheng and V. D. Agrawal, "Methods for synthesizing testable sequential circuits," *AT&T Technical Journal*, vol. 70, pp. 64–86, Jan. 1991.
- [128] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "On test generation using neural computers," *Intl. J. Computer Aided VLSI Design*, vol. 3, pp. 241–257, 1991.
- [129] K. T. Cheng and V. D. Agrawal, "State assignment for testable design," *Intl. J. Computer Aided VLSI Design*, vol. 3, pp. 291–307, 1991.

- [130] S. Bhawmik, C. J. Lin, K. T. Cheng, and V. D. Agrawal, "PASCANT: A partial scan and test generation system," in *Proc. Custom Integrated Circ. Conf.*, May 1991.
- [131] S. T. Chakradhar and V. D. Agrawal, "A transitive closure based algorithm for test generation," in *Proc. 28th Design Automation Conf.*, June 1991.
- [132] P. C. Sardeshmukh and V. D. Agrawal, "Filtering of SEM voltage contrast images," *3rd European Conf. Electron and Optical Beam Testing*, Sept. 1991.
- [133] J. Villoldo, P. Agrawal, and V. D. Agrawal, "Stafan algorithms for MOS circuits," in *Proc. Intl. Conf. Computer Design*, pp. 56–59, Oct. 1991.
- [134] V. D. Agrawal, "Design and test — the two sides of a coin," in *Proc. Intl. Conf. Computer Design*, p. 12, Oct. 1991.
- [135] D. V. Das, S. C. Seth, and V. D. Agrawal, "Estimating the quality of manufactured digital sequential circuits," in *Proc. Intl. Test Conf.*, pp. 210–217, Oct. 1991.
- [136] P. Agrawal, V. D. Agrawal, and S. C. Seth, "A new method for generating tests for delay faults in non-scan circuits," in *Proc. 5th Intl. Conf. VLSI Design*, pp. 4–11, Jan. 1992.
- [137] J. Jacob and V. D. Agrawal, "Functional test generation for sequential circuits," in *Proc. 5th Intl. Conf. VLSI Design*, pp. 17–24, Jan. 1992.
- [138] V. D. Agrawal, "Technology forecast and weather prediction (keynote address)," in *Proc. 2nd Great Lakes Symp. on VLSI*, pp. 1–2, Feb. 1992.
- [139] K. T. Cheng and V. D. Agrawal, "Initializability considerations in sequential machine synthesis," *IEEE Trans. Comput.*, vol. 41, pp. 374–379, Mar. 1992.
- [140] S. T. Chakradhar, M. A. Iyer, and V. D. Agrawal, "Energy minimization based delay testing," in *Proc. European Design Autom. Conf.*, pp. 280–284, Mar. 1992.
- [141] S. T. Chakradhar, S. Kanjilal, and V. D. Agrawal, "A synthesis for testability technique for PLA-based finite state machines," in *Proc. European Design Autom. Conf.*, pp. 361–365, Mar. 1992.
- [142] E. Ulrich, K. P. Lentz, J. Arabian, M. Gustin, V. D. Agrawal, and P. L. Montessoro, "The comparative and concurrent simulation of discrete-event experiments," *J. Electronic Testing: Theory and Applic. (JETTA)*, vol. 3, pp. 107–118, May 1992.

- [143] J. Jacob and V. D. Agrawal, "Multiple fault detection in two-level multi-output circuits," *J. Electronic Testing: Theory and Applic. (JETTA)*, vol. 3, pp. 171–173, May 1992.
- [144] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Delay fault models and test generation for random logic sequential circuits," in *Proc. Design Autom. Conf.*, pp. 165–172, June 1992.
- [145] D. Bhattacharya, P. Agrawal, and V. D. Agrawal, "Delay fault test generation for scan/hold circuits using Boolean expressions," in *Proc. Design Autom. Conf.*, pp. 159–164, June 1992.
- [146] S. T. Chakradhar, S. Kanjilal, and V. D. Agrawal, "Finite state machine synthesis with fault tolerant test function," in *Proc. Design Autom. Conf.*, pp. 562–567, June 1992. also *J. Electronic Testing: Theory and Applic. (JETTA)*, vol. 4, pp. 57–69, February 1993.
- [147] M. K. Srinivas, J. Jacob, and V. D. Agrawal, "Finite state machine testing based on growth and disappearance faults," in *Proc. 22nd Fault-Tolerant Comput. Symp.*, pp. 238–245, July 1992.
- [148] P. Agrawal, V. D. Agrawal, and S. C. Seth, "DynaTAPP: Dynamic timing analysis with partial path activation in sequential circuits," in *Proc. EURO-DAC*, pp. 138–141, Sept. 1992.
- [149] V. D. Agrawal and S. T. Chakradhar, "Performance analysis of synchronized iterative algorithms on multiprocessor systems," *IEEE Trans. Parallel and Distr. Syst.*, vol. 3, pp. 739–746, Nov. 1992.
- [150] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Path delay simulation algorithms for sequential circuits," in *Proc. First Asian Test Symp.*, pp. 52–56, Nov. 1992.
- [151] S. Bose, P. Agrawal, and V. D. Agrawal, "A path delay fault simulator for sequential circuits," in *Proc. 6th International Conf. VLSI Design*, pp. 269–274, Jan. 1993.
- [152] P. Agrawal, V. D. Agrawal, and S. C. Seth, "Generating tests for delay faults in nonscan circuits," *IEEE Design & Test of Computers*, vol. 10, pp. 20–28, Mar. 1993.
- [153] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A tutorial on built-in self-test, part 1: Principles," *IEEE Design & Test of Computers*, vol. 10, pp. 73–82, Mar. 1993.
- [154] K. L. Einspahr, S. C. Seth, and V. D. Agrawal, "Clock partitioning for testability," in *Proc. 3rd Great Lakes Symp. VLSI*, pp. 42–46, Mar. 1993.
- [155] S. Bose, P. Agrawal, and V. D. Agrawal, "Delay fault testability evaluation through timing simulation," in *Proc. 3rd Great Lakes Symp. VLSI*, pp. 18–21, Mar. 1993.

- [156] V. D. Agrawal and T. J. Chakraborty, "Partial scan testing with single clock control," in *Proc. IEEE VLSI Test Symp.*, pp. 313–315, Apr. 1993.
- [157] V. D. Agrawal and S. T. Chakradhar, "Combinational ATPG theorems for identifying untestable faults in sequential circuits," in *Proc. European Test Conf.*, pp. 249–253, Apr. 1993.
- [158] V. D. Agrawal, "A tale of two designs: the cheapest and the most economic (keynote talk)," in *Second International Workshop on the Economics of Design, Test and Manufacturing*, May 1993. Also Proc. 12th AT&T Conference on Electronic Testing, September 1993, pp. 241–244.
- [159] S. T. Chakradhar, V. D. Agrawal, and S. G. Rothweiler, "A transitive closure algorithm for test generation," *IEEE Trans. CAD*, vol. 12, pp. 1015–1028, July 1993.
- [160] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A tutorial on built-in self-test, part 2: Applications," *IEEE Design & Test of Computers*, vol. 10, pp. 69–77, June 1993.
- [161] P. Agrawal, V. D. Agrawal, and J. Villoldo, "Sequential circuit test generation on a distributed system," in *Proc. 29th Design Autom. Conf.*, pp. 107–111, June 1993.
- [162] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Design for testability for path delay faults in sequential circuits," in *Proc. 29th Design Autom. Conf.*, pp. 453–457, June 1993.
- [163] P. Agrawal, V. D. Agrawal, and J. Villoldo, "Test pattern generation for sequential circuits on a network of workstations," in *Proc. 2nd International Symp. High Performance Distr. Comput.*, pp. 114–120, July 1993.
- [164] S. Bose, P. Agrawal, and V. D. Agrawal, "The optimistic update theorem for path delay testing of sequential circuits," *J. Electronic Testing: Theory and Applic.*, vol. 4, pp. 285–290, Aug. 1993.
- [165] S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "Test function embedding algorithms with application to interconnected finite state machines," in *Proc. EURO-DAC*, pp. 219–224, Sept. 1993.
- [166] S. Bose, P. Agrawal, and V. D. Agrawal, "Logic systems for path delay test generation," in *Proc. EURO-DAC*, pp. 200–205, Sept. 1993.
- [167] S. Bose, P. Agrawal, and V. D. Agrawal, "Generation of compact delay tests by multiple path activation," in *Proc. International Test Conf.*, pp. 714–723, Oct. 1993.
- [168] S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "A synthesis approach to design for testability," in *Proc. International Test Conf.*, pp. 754–763, Oct. 1993.

- [169] P. R. Sureshkumar, J. Jacob, M. K. Srinivas, and V. D. Agrawal, "FAS-SAD: Fault simulation with sensitivities and depth-first propagation," in *Proc. 2nd Asian Test Symp.*, pp. 66–71, Nov. 1993.
- [170] S. Bose, P. Agrawal, and V. D. Agrawal, "Path delay fault simulation of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 1, pp. 453–461, Dec. 1993.
- [171] D. Das, S. C. Seth, and V. D. Agrawal, "Accurate computation of field reject ratio based on fault latency," *IEEE Trans. VLSI Systems*, vol. 1, pp. 537–545, Dec. 1993.
- [172] S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "A test function architecture for interconnected finite state machines," in *Proc. 7th International Conference VLSI Design*, pp. 113–116, Jan. 1994.
- [173] R. Chou, K. Saluja, and V. D. Agrawal, "Power constraint scheduling of tests," in *Proc. 7th International Conference VLSI Design*, pp. 271–274, Jan. 1994.
- [174] P. R. Sureshkumar, J. Jacob, M. K. Srinivas, and V. D. Agrawal, "An improved deductive fault simulator," in *Proc. 7th International Conference VLSI Design*, pp. 307–310, Jan. 1994.
- [175] E. G. Ulrich, V. D. Agrawal, and J. H. Arabian, *Concurrent and Comparative Discrete Event Simulation*. Boston: Kluwer Academic Publishers, 1994.
- [176] S. T. Chakradhar, V. D. Agrawal, and M. L. Bushnell, "Energy minimization and design for testability," *J. Electronic Testing: Theory and Applic.*, vol. 5, pp. 55–64, Feb. 1994.
- [177] T. J. Chakraborty and V. D. Agrawal, "Delay independent initialization of sequential circuits," in *Proc. 4th Great Lakes Symp. VLSI Design*, pp. 228–230, Mar. 1994.
- [178] K. Heragu, V. D. Agrawal, and M. L. Bushnell, "FACTS: Fault coverage estimation by test vector sampling," in *Proc. 12th IEEE VLSI Test Symp.*, pp. 266–271, Apr. 1994.
- [179] V. D. Agrawal, "A tale of two designs: the cheapest and the most economic," *J. Electronic Testing: Theory and Applic.*, vol. 5, pp. 131–135, May 1994.
- [180] K. Heragu, M. L. Bushnell, and V. D. Agrawal, "An efficient path delay fault coverage estimator," in *Proc. 31st Design Automation Conf.*, pp. 516–521, June 1994.
- [181] S. T. Chakradhar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops," in *Proc. 31st Design Automation Conf.*, pp. 81–86, June 1994.

- [182] V. D. Agrawal, C. J. Lin, P. Rutkowski, S. Wu, and Y. Zorian, "Built-in self-test for digital integrated circuits," *AT&T Tech. Jour.*, vol. 73, pp. 30–39, Mar. 1994.
- [183] T. J. Chakraborty and V. D. Agrawal, "Test generation and fault simulation algorithms for sequential circuits with embedded RAMs," in *Proc. Third Asian Test Symp.*, pp. 2–7, Nov. 1994.
- [184] P. Agrawal, V. D. Agrawal, M. L. Bushnell, and J. Sienicki, "Superlinear speedup in multiprocessing environment," in *Proc. First International Workshop on Parallel Processing*, pp. 261–265, Dec. 1994.
- [185] J. Sienicki, M. L. Bushnell, P. Agrawal, and V. D. Agrawal, "An asynchronous algorithm for sequential circuit test generation on a network of workstations," in *Proc. 8th International Conf. VLSI Design*, pp. 36–41, Jan. 1995.
- [186] T. J. Chakraborty and V. D. Agrawal, "Robust testing for stuck-at faults," in *Proc. 8th International Conf. VLSI Design*, pp. 42–46, Jan. 1995.
- [187] M. K. Srinivas, J. Jacob, and V. D. Agrawal, "Functional test generation for non-scan sequential circuits," in *Proc. 8th International Conf. VLSI Design*, pp. 47–52, Jan. 1995.
- [188] A. K. Majhi, J. Jacob, L. M. Patnaik, and V. D. Agrawal, "An efficient automatic test generation system for path delay faults in combinational circuits," in *Proc. 8th International Conf. VLSI Design*, pp. 161–165, Jan. 1995.
- [189] K. Heragu, V. D. Agrawal, and M. L. Bushnell, "Statistical methods for delay fault coverage analysis," in *Proc. 8th International Conf. VLSI Design*, pp. 166–170, Jan. 1995.
- [190] D. Bhattacharya, P. Agrawal, and V. D. Agrawal, "Test generation for path delay faults using binary decision diagrams," *IEEE Trans. Computers*, vol. 44, pp. 434–447, Mar. 1995.
- [191] S. T. Chakradhar, S. Rothweiler, and V. D. Agrawal, "Redundancy removal and test generation for circuits with non-Boolean primitives," in *Proc. 13th IEEE VLSI Test Symp.*, pp. 12–19, April-May 1995.
- [192] T. J. Chakraborty and V. D. Agrawal, "Simulation of at-speed tests for stuck-at faults," in *Proc. 13th IEEE VLSI Test Symp.*, pp. 216–220, April-May 1995.
- [193] K. Heragu, V. D. Agrawal, and M. L. Bushnell, "Fault coverage estimation by test vector sampling," *IEEE Trans. CAD*, vol. 14, pp. 590–596, May 1995. Correction, August 1995, p. 1037.

- [194] S. T. Chakradhar, M. Iyer, and V. D. Agrawal, "Energy models for delay testing," *IEEE Trans. CAD*, vol. 14, pp. 728–739, June 1995.
- [195] S. T. Chakradhar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops," *J. Electronic Testing: Theory and Applic.*, vol. 7, pp. 83–93, Aug. 1995.
- [196] S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "Test function embedding algorithms with application to interconnected finite state machines," *IEEE Trans. CAD*, vol. 14, pp. 1115–1127, Sept. 1995.
- [197] V. D. Agrawal and S. T. Chakradhar, "Combinational ATPG theorems for identifying untestable faults in sequential circuits," *IEEE Trans. CAD*, vol. 14, pp. 1155–1160, Sept. 1995.
- [198] J. Sienicki, M. L. Bushnell, P. Agrawal, and V. D. Agrawal, "An adaptive distributed algorithm for sequential circuit test generation," in *Proc. EURO-DAC*, pp. 236–241, Sept. 1995.
- [199] S. Kanjilal, S. T. Chakradhar, and V. D. Agrawal, "A partition and resynthesis approach to testable design of large circuits," *IEEE Trans. CAD*, vol. 14, pp. 1268–1276, Oct. 1995.
- [200] M. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "Classification and test generation for path-delay faults using single stuck-fault tests," in *Proc. International Test Conf.*, pp. 139–148, Oct. 1995.
- [201] V. D. Agrawal and T. J. Chakraborty, "High-performance circuit testing with slow-speed testers," in *Proc. International Test Conf.*, pp. 302–310, Oct. 1995.
- [202] M. K. Srinivas, V. D. Agrawal, and M. L. Bushnell, "Functional test generation for path delay faults," in *Proc. Fourth Asian Test Symp.*, pp. 339–345, Nov. 1995.
- [203] S. Bose and V. D. Agrawal, "Sequential logic path delay test generation by symbolic analysis," in *Proc. Fourth Asian Test Symp.*, pp. 353–359, Nov. 1995.
- [204] V. D. Agrawal, "Science, technology and the indian society, A keynote talk," in *Proc. 9th International Conf. VLSI Design*, pp. 6–8, Jan. 1996.
- [205] T. J. Chakraborty and V. D. Agrawal, "Design for high speed testability of stuck-at faults," in *Proc. 9th International Conf. VLSI Design*, pp. 53–56, Jan. 1996.
- [206] L. Pappu, M. L. Bushnell, and V. D. Agrawal, "Statistical path-delay fault coverage estimation for synchronous sequential circuits," in *Proc. 9th International Conf. VLSI Design*, pp. 290–295, Jan. 1996.

- [207] V. D. Agrawal and D. Lee, "Characteristic polynomial method for verification and test of combinational circuits," in *Proc. 9th International Conf. VLSI Design*, pp. 341–342, Jan. 1996.
- [208] A. K. Majhi, J. Jacob, L. M. Patnaik, and V. D. Agrawal, "On test coverage of path-delay faults," in *Proc. 9th International Conf. VLSI Design*, pp. 418–421, Jan. 1996.
- [209] K. Heragu, J. H. Patel, and V. D. Agrawal, "Improving accuracy in path-delay fault coverage estimation," in *Proc. 9th International Conf. VLSI Design*, pp. 422–425, Jan. 1996.
- [210] M. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "Parallel pattern concurrent fault simulation of path-delay faults with single-input change tests," in *Proc. 9th International Conf. VLSI Design*, pp. 426–431, Jan. 1996.
- [211] K. L. Einspahr, S. C. Seth, and V. D. Agrawal, "Improving circuit testability by clock control," in *Proc. Sixth Great Lakes Symp. on VLSI*, pp. 288–293, Mar. 1996.
- [212] K. Heragu, J. H. Patel, and V. D. Agrawal, "Segment delay faults: A new fault model," in *Proc. 14th IEEE VLSI Test Symp.*, pp. 32–39, April-May 1996.
- [213] M. K. Srinivas, J. Jacob, and V. D. Agrawal, "Functional test generation for synchronous sequential circuits," *IEEE Trans. on CAD*, vol. 15, pp. 831–843, July 1996.
- [214] V. D. Agrawal, "Testing in a mixed-signal world," in *Proc. 9th Annual IEEE International ASIC Conf.*, pp. 241–244, Oct. 1996.
- [215] M. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "An exact non-enumerative fault simulator for path-delay faults," in *Proc. International Test Conf.*, pp. 276–285, Oct. 1996.
- [216] V. D. Agrawal, R. D. Blanton, and M. Damiani, "Synthesis of self-testing finite state machines from high-level specification," in *Proc. International Test Conf.*, pp. 757–766, Oct. 1996.
- [217] V. D. Agrawal, M. L. Bushnell, and Q. Lin, "Redundancy Identification using Transitive Closure," in *Proc. Fifth IEEE Asian Test Symp.*, pp. 4–9, Nov. 1996.
- [218]
- [219] K. Heragu, J. H. Patel, and V. D. Agrawal, "SIGMA: A Simulator for Segment Delay Faults," in *Proc. IEEE ACM International Conf. on CAD*, pp. 502–508, Nov. 1996.

- [220] M. K. Srinivas, M. L. Bushnell, and V. D. Agrawal, "Flags and Algebra for Sequential Circuit VNR Path Delay Fault Test Generation," in *Proc. 10th International Conf. on VLSI Design*, pp. 88–94, Jan. 1997.
- [221] V. D. Agrawal, "Low-power design by hazard filtering," in *Proc. 10th International Conf. on VLSI Design*, pp. 193–197, Jan. 1997.
- [222] J. Jacob, P. S. Sivakumar, and V. D. Agrawal, "Adder and comparator synthesis with exclusive-OR transform of inputs," in *Proc. 10th International Conf. on VLSI Design*, pp. 514–515, Jan. 1997.
- [223] S. T. Chakradhar and V. D. Agrawal, "Vlsi design," in *Encyclopedia of Microcomputers* (A. Kent and J. G. Williams, eds.), pp. 97–111, New York: Marcel Dekker, Inc., 1997. Volume 20.
- [224] R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling tests for vlsi systems under power constraints," *IEEE Trans. VLSI Systems*, vol. 5, pp. 175–185, June 1997.
- [225] K. Heragu, V. D. Agrawal, M. L. Bushnell, and J. H. Patel, "Improving a nonenumerative method to estimate path delay fault coverage," *IEEE Trans. CAD*, vol. 16, pp. 759–762, July 1997.
- [226] M. A. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "Classification and test generation for path-delay faults using single stuck-at fault tests," *J. Electronic Testing: Theory and Applications*, vol. 11, pp. 55–67, Aug. 1997.
- [227] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "On variable clock methods for path delay testing of sequential circuits," *IEEE Trans. CAD*, vol. 16, pp. 1237–1249, Nov. 1997.
- [228] S. T. Chakradhar, S. G. Rothweiler, and V. D. Agrawal, "Redundancy removal and test generation for circuits with non-Boolean primitives," *IEEE Trans. CAD*, vol. 16, pp. 1370–1377, Nov. 1997.
- [229] S. Bose, V. D. Agrawal, and T. G. Szymanski, "Algorithms for switch level delay fault simulation," in *Proc. International Test Conf.*, pp. 982–991, 1997.
- [230] T. J. Chakraborty and V. D. Agrawal, "Effective path selection for delay fault testing of sequential circuits," in *Proc. International Test Conf.*, pp. 998–1003, 1997.
- [231] K. Heragu, J. H. Patel, and V. D. Agrawal, "Fast identification of untestable delay faults using implications," in *Proc. International Conf. CAD*, pp. 642–647, 1997.
- [232] P. Chavda, J. Jacob, and V. D. Agrawal, "Optimizing logic using Boolean transforms," in *Proc. 11th International Conf. VLSI Design*, pp. 218–221, 1998.

- [233] A. K. Majhi and V. D. Agrawal, "Mixed-signal test," in *Proc. 11th International Conf. VLSI Design*, pp. 285–288, 1998.
- [234] A. K. Majhi and V. D. Agrawal, "Tutorial: Delay fault models and coverage," in *Proc. 11th International Conf. VLSI Design*, pp. 364–369, 1998.
- [235] S. Majumder, V. D. Agrawal, and M. L. Bushnell, "Path delay testing: Variable-clock versus rated-clock," in *Proc. 11th International Conf. VLSI Design*, pp. 470–475, 1998.
- [236] V. D. Agrawal and S. C. Seth, "Mutually disjoint signals and probability calculation in digital circuits," in *Proc. 8th Great Lakes Symp. VLSI*, pp. 307–312, 1998.
- [237] M. A. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "The path-status graph with application to delay fault simulation," *IEEE Trans. CAD*, vol. 17, pp. 324–332, Apr. 1998.
- [238] V. D. Agrawal, "Test education for vlsi systems design engineers," in *Proc. Computer Soc. Workshop on VLSI*, pp. 62–64, 1998.
- [239] S. Majumder, V. D. Agrawal, and M. L. Bushnell, "On delay-untestable paths and stuck-fault redundancy," in *Proc. 16th IEEE VLSI Test Symp.*, pp. 194–199, 1998.
- [240] S. Bose, P. Agrawal, and V. D. Agrawal, "A rated-clock test method for path delay faults," *IEEE Trans. VLSI Systems*, vol. 6, pp. 323–331, June 1998.
- [241] L. Pappu, M. L. Bushnell, V. D. Agrawal, and S. Mandyam-Komar, "Statistical delay fault coverage estimation for synchronous sequential circuits," *J. Electronic Testing: Theory and Applications*, vol. 12, pp. 239–254, June 1998.
- [242] V. D. Agrawal, D. Lee, and H. Woźniakowski, "Numerical computation of characteristic polynomials of Boolean functions and its applications," *Numerical Algorithms*, vol. 17, pp. 261–278, 1998.
- [243] S. Bose, P. Agrawal, and V. D. Agrawal, "Deriving logic systems for path delay test generation," *IEEE Trans. Computers*, vol. 47, pp. 829–846, Aug. 1998.
- [244] M. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "A parallel-vector concurrent-fault simulator and generation of single-input-change tests for path-delay faults," *IEEE Trans. CAD*, vol. 17, pp. 873–876, Sept. 1998.
- [245] C. G. Parodi, V. D. Agrawal, M. L. Bushnell, and S. Wu, "A non-enumerative path delay fault simulator for sequential circuits," in *Proc. International Test Conf.*, pp. 934–943, 1998.

- [246] M. Gharaybeh, V. D. Agrawal, and M. L. Bushnell, "False path removal using delay fault simulation," in *Proc. 7th IEEE Asian Test Symp.*, pp. 82–87, 1998.
- [247] V. D. Agrawal, "Design of mixed-signal systems for testability," *INTEGRATION, The VLSI Journal*, vol. 26, pp. 141–150, 1998.
- [248] V. D. Agrawal, M. L. Bushnell, G. Parthasarathy, and R. Ramadoss, "Digital circuit design for minimum transient energy and a linear programming method," in *Proc. 12th International Conf. VLSI Design*, pp. 434–439, 1999.
- [249] K. Heragu, J. H. Patel, and V. D. Agrawal, "A test generator for segment delay faults," in *Proc. 12th International Conf. VLSI Design*, pp. 484–491, 1999.
- [250] S. Majumder, B. B. Bhattacharya, V. D. Agrawal, and M. L. Bushnell, "A complete characterization of path delay faults through stuck-at faults," in *Proc. 12th International Conf. VLSI Design*, pp. 492–497, 1999.
- [251] Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "A correlation matrix method of clock partitioning for sequential circuit testability," in *Proc. 9th Great Lakes Symp. on VLSI*, pp. 300–303, 1999.
- [252] P. A. Thaker, V. D. Agrawal, and M. E. Zaghoul, "Validation vector grade (VVG): A new coverage metric for validation and test," in *Proc. 17th IEEE VLSI Test Symp.*, pp. 182–188, 1999.
- [253] Q. Peng, V. D. Agrawal, and J. Savir, "On the guaranteed failing and working frequencies in path delay fault analysis," in *Proc. 16th IEEE Instrumentation and Measurement Technology Conf.*, pp. 1794–1799, 1999.
- [254] V. D. Agrawal, "Choice of tests for logic verification and equivalence checking and the use of fault simulation," in *Proc. 13th International Conf. VLSI Design*, pp. 304–309, Jan. 2000.
- [255] H.-C. Tsai, K.-T. Cheng, and V. D. Agrawal, "A testability metric for path delay faults and its application," in *Proc. Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pp. 593–598, Jan. 2000.
- [256] J. T. deSousa and V. D. Agrawal, "Reducing the complexity of defect level modeling using the clustering effect," in *Proc. Design, Automation and Test in Europe (DATE) Conf.*, pp. 640–644, Mar. 2000.
- [257] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Path delay fault simulation of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 8, pp. 223–228, Apr. 2000.
- [258] A. K. Majhi, V. D. Agrawal, J. Jacob, and L. M. Patnaik, "Line coverage of path delay faults," *IEEE Trans. VLSI Systems*, vol. 8, pp. 610–614, Oct. 2000.

- [259] M. A. Gharaybeh, V. D. Agrawal, M. L. Bushnell, and C. G. Parodi, "False-path removal using delay fault simulation," *J. Electronic Testing: Theory and Applic.*, vol. 16, pp. 463–476, Oct. 2000.
- [260] P. A. Thaker, V. D. Agrawal, and M. E. Zaghloul, "Register-transfer level fault modeling and test evaluation techniques for vlsi circuits," in *Proc. International Test Conf.*, pp. 940–949, Oct. 2000.
- [261] A. Giani, S. Sheng, M. Hsiao, and V. D. Agrawal, "Compaction-based test generation using state and fault information," in *Proc. 9th Asian Test Symp.*, pp. 159–164, Dec. 2000.
- [262] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Boston: Kluwer Academic Publishers, 2000.
- [263] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Improving path delay testability of sequential circuits," *IEEE Trans. VLSI Systems*, vol. 8, pp. 736–741, Dec. 2000.
- [264] Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "Combinational test generation for acyclic sequential circuits using a balanced ATPG model," in *Proc. 14th International Conf. VLSI Design*, pp. 143–148, Jan. 2001.
- [265] A. Giani, S. Sheng, M. Hsiao, and V. D. Agrawal, "Efficient spectral techniques for sequential ATPG," in *Proc. Design, Automation and Test in Europe (DATE) Conf.*, pp. 204–208, Mar. 2001.
- [266] A. Giani, S. Sheng, M. Hsiao, and V. D. Agrawal, "Novel spectral methods for built-in self-test in a system-on-a-chip environment," in *Proc. 19th IEEE VLSI Test Symp.*, pp. 163–168, Apr. 2001.
- [267] Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "Combinational test generation for various classes of acyclic sequential circuits," in *Proc. International Test Conf.*, pp. 1078–1087, Oct. 2001.
- [268] Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "Multiple faults: Modeling, simulation and test," in *Proc. 7th ASPDAC/15th International Conf. VLSI Design*, pp. 592–597, Jan. 2002.
- [269] V. Gaur, V. D. Agrawal, and M. L. Bushnell, "A new transitive closure algorithm with application to redundancy identification," in *Proc. 1st International Workshop on Electronic, Design and Test Applications (DELTA '02)*, pp. 496–500, Jan. 2002.
- [270] A. Giani, S. Sheng, M. Hsiao, and V. D. Agrawal, "Compaction-based test generation using state and fault information," *J. Electronic Testing: Theory and Applic.*, vol. 18, pp. 63–72, Feb. 2002.

- [271] A. D. Sathe, M. L. Bushnell, and V. D. Agrawal, "Analog macromodeling of capacitive coupling faults in digital circuit interconnects," in *Proc. International Test Conf.*, pp. 375–383, Oct. 2002.
- [272] A. V. S. S. Prasad, V. D. Agrawal, and M. V. Atre, "A new algorithm for global fault collapsing into equivalence and dominance cells," in *Proc. International Test Conf.*, pp. 391–397, Oct. 2002.
- [273] V. D. Agrawal, D. H. Baik, Y. C. Kim, and K. K. Saluja, "Exclusive test and its applications in fault diagnosis," in *Proc. 16th International Conf. VLSI Design*, pp. 143–148, Jan. 2003.
- [274] V. Mehta, K. Dave, V. D. Agrawal, and M. L. Bushnell, "A fault-independent transitive closure algorithm for redundancy identification," in *Proc. 16th International Conf. VLSI Design*, pp. 149–154, Jan. 2003.
- [275] L. Rao, M. L. Bushnell, and V. D. Agrawal, "Graphical  $I_{DDQ}$  signatures reduce defect level and yield loss," in *Proc. 16th International Conf. VLSI Design*, pp. 353–360, Jan. 2003.
- [276] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Minimum dynamic power CMOS circuit design by a reduced constraint set linear program," in *Proc. 16th International Conf. VLSI Design*, pp. 527–532, Jan. 2003.
- [277] P. A. Thaker, V. D. Agrawal, and M. E. Zaghoul, "A test evaluation technique for VLSI circuits using register-transfer level fault modeling," *IEEE Trans. CAD*, vol. 22, pp. 1104–1113, Aug. 2003.
- [278] V. D. Agrawal, A. V. S. S. Prasad, and M. V. Atre, "Fault collapsing via functional dominance," in *Proc. International Test Conf.*, pp. 274–280, Sept. 2003.
- [279] T. Raja, V. D. Agrawal, and M. L. Bushnell, "CMOS circuit design for minimum dynamic power and highest speed," in *Proc. 17th International Conf. VLSI Design*, pp. 1035–1040, Jan. 2004.
- [280] T. Raja, V. D. Agrawal, and M. L. Bushnell, "A tutorial on the emerging nanotechnology devices," in *Proc. 17th International Conf. VLSI Design*, pp. 343–360, Jan. 2004.
- [281] S. Majumder, B. B. Bhattacharya, V. D. Agrawal, and M. L. Bushnell, "New classification of path-delay fault testability in terms of stuck-at faults," *Journal of Computer Science and Technology (Academia Sinica)*, vol. 19, pp. 955–964, Nov. 2004.
- [282] J. Zhang, M. L. Bushnell, and V. D. Agrawal, "On random pattern generation with the selfish gene algorithm for testing digital sequential circuits," in *Proc. International Test Conf.*, pp. 617–626, Oct. 2004.

- [283] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Variable input delay cmos logic for low power design," in *Proc. 18th International Conf. VLSI Design*, pp. 598–605, Jan. 2005.
- [284] K. Dave, V. D. Agrawal, and M. L. Bushnell, "Using contrapositive law in an implication graph to identify logic redundancies," in *Proc. 18th International Conf. VLSI Design*, pp. 723–729, Jan. 2005.
- [285] R. K. K. R. Sandireddy and V. D. Agrawal, "Diagnostic and detection fault collapsing for multiple output circuits," in *Proc. Design, Automation and Test in Europe (DATE'05)*, pp. 1014–1019, Mar. 2005.
- [286] F. Hu and V. D. Agrawal, "Dual-transition glitch filtering in probabilistic waveform power estimation," in *Proc. 15th IEEE Great Lakes Symp. on VLSI*, pp. 357–360, Apr. 2005.
- [287] Y. C. Kim, V. D. Agrawal, and K. K. Saluja, "Combinational automatic test pattern generation for acyclic sequential circuits," *IEEE Trans. CAD*, vol. 24, pp. 948–956, June 2005.
- [288] S. Uppalapati, M. L. Bushnell, and V. D. Agrawal, "Glitch-free design of low power asics using customized resistive feedthrough cells," in *Proc. 9th VLSI Design & Test Symp. (VDAT'05)*, pp. 41–49, Aug. 2005.
- [289] A. S. Mudlapur, V. D. Agrawal, and A. D. Singh, "A novel random access scan flip-flop design," in *Proc. 9th VLSI Design & Test Symp. (VDAT'05)*, pp. 226–236, Aug. 2005.
- [290] A. S. Doshi and V. D. Agrawal, "Independence fault collapsing," in *Proc. 9th VLSI Design & Test Symp. (VDAT'05)*, pp. 357–366, Aug. 2005.
- [291] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Variable input delay cmos logic design for low dynamic power circuits," in *Proc. Power and Timing Modeling, Optimization and Simulation Workshop (PATMOS'05)*, pp. 436–445, Sept. 2005.
- [292] Y. Lu and V. D. Agrawal, "Leakage and dynamic glitch power minimization using integer linear programming for  $V_{th}$  assignment and path balancing," in *Proc. Power and Timing Modeling, Optimization and Simulation Workshop (PATMOS'05)*, pp. 217–226, Sept. 2005.
- [293] F. Hu and V. D. Agrawal, "Enhanced dual-transition probabilistic power estimation with selective supergate analysis," in *Proc. IEEE International Conf. on Computer Design*, pp. 366–369, Oct. 2005.
- [294] A. S. Mudlapur, V. D. Agrawal, and A. D. Singh, "A random access scan architecture to reduce hardware overhead," in *Proc. International Test Conf.*, Nov. 2005. Paper 15.1.

- [295] V. D. Agrawal and A. S. Doshi, "Concurrent test generation," in *Proc. 14th IEEE Asian Test Symp.*, pp. 294–297, Dec. 2005.
- [296] K. R. Kantipudi and V. D. Agrawal, "On the size and generation of minimal N-detection tests," in *Proc. 19th International Conf. VLSI Design*, pp. 425–430, Jan. 2006.
- [297] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Transistor sizing of logic gates to maximize input delay variability," *Journal of Low Power Electronics*, vol. 2, pp. 121–128, Apr. 2006.
- [298] V. D. Agrawal, S. Bose, and V. Gangaram, "Upper bounding fault coverage by structural analysis and signal monitoring," in *Proc. 24th IEEE VLSI Test Symp.*, pp. 88–93, May 2006.
- [299] N. Yogi and V. D. Agrawal, "Spectral characterization of functional vectors for gate-level fault coverage tests," in *Proc. 10th VLSI Design & Test Symp. (VDAT'06)*, pp. 407–417, Aug. 2006.
- [300] F. Hu and V. D. Agrawal, "Input-specific dynamic power optimization for vlsi circuits," in *Proc. Int. Symp. on Low Power Electronics and Design (ISLPED'06)*, pp. 232–237, Oct. 2006.
- [301] S. Bose and V. D. Agrawal, "Fault coverage estimation for non-random functional input sequences," in *Proc. Int. Test Conf.*, pp. 19.3.1–19.3.10, Oct. 2006.
- [302] N. Yogi and V. D. Agrawal, "Spectral RTL test generation for gate-level stuck-at faults," in *Proc. 15th IEEE Asian Test Symp. (ATS06)*, pp. 83–88, Nov. 2006.
- [303] Y. Lu and V. D. Agrawal, "CMOS leakage and glitch minimization for power-performance tradeoff," *Journal of Low Power Electronics*, vol. 2, pp. 378–387, Dec. 2006.
- [304] Y. Lu and V. D. Agrawal, "Statistical leakage and timing optimization for submicron process variation," in *Proc. 20th International Conf. VLSI Design*, pp. 439–444, Jan. 2007.
- [305] N. Yogi and V. D. Agrawal, "Spectral RTL test generation for microprocessors," in *Proc. 20th International Conf. VLSI Design*, pp. 473–478, Jan. 2007.
- [306] K. R. Kantipudi and V. D. Agrawal, "A reduced complexity algorithm for minimizing N-detect tests," in *Proc. 20th International Conf. VLSI Design*, pp. 492–497, Jan. 2007.
- [307] N. Yogi and V. D. Agrawal, "Transition delay fault testing of microprocessors by spectral method," in *Proc. 39th Southeastern Symp. on System Theory*, pp. 283–287, Mar. 2007.

- [308] S. Bose and V. D. Agrawal, "Delay test quality evaluation using bounded gate delays," in *Proc. 25th IEEE VLSI Test Symp.*, pp. 23–28, May 2007.
- [309] R. K. K. R. Sandireddy and V. D. Agrawal, "Using hierarchy in design automation: The fault collapsing problem," in *Proc. 11th VLSI Design & Test Symp. (VDAT'07)*, pp. 174–184, Aug. 2007.
- [310] S. Bose and V. D. Agrawal, "Estimating stuck fault coverage in sequential circuits using state traversal and entropy analysis," in *Proc. Int. Test Conf.*, pp. 26.1.1–26.1.10, Oct. 2007.
- [311] S. Bose, H. Grimes, and V. D. Agrawal, "Delay fault simulation with bounded gate delay model," in *Proc. Int. Test Conf.*, pp. 26.3.1–26.3.10, Oct. 2007.
- [312] O. I. Khan, M. L. Bushnell, S. K. Devanathan, and V. D. Agrawal, "SPARTAN: a spectral and information theoretic approach to partial scan," in *Proc. Int. Test Conf.*, Oct. 2007. Paper 21.1.
- [313] L. Rao, M. L. Bushnell, and V. D. Agrawal, "Graphical  $I_{DDQ}$  signatures reduce defect level and yield loss," *IEEE Trans. VLSI Systems*, vol. 15, pp. 1245–1255, Nov. 2007.
- [314] F. Wang and V. D. Agrawal, "Single event upset: An embedded tutorial," in *Proc. 21st International Conf. VLSI Design*, pp. 429–434, Jan. 2008.
- [315] Y. Lu and V. D. Agrawal, "Total power minimization in glitch-free CMOS circuits considering process variation," in *Proc. 21st International Conf. VLSI Design*, pp. 531–536, Jan. 2008.
- [316] N. Yogi and V. D. Agrawal, " $N$ -model tests for VLSI circuits," in *Proc. 40th Southeastern Symp. System Theory*, pp. 242–246, Mar. 2008.
- [317] F. Wang and V. D. Agrawal, "Soft Error Rate Determination for Nanometer CMOS VLSI Logic," in *Proc. 40th Southeastern Symp. System Theory*, pp. 324–328, Mar. 2008.
- [318] R. Sethuram, M. L. Bushnell, and V. D. Agrawal, "Fault Nodes in Implication Graph for Equivalence/Dominance Collapsing, and Identifying Untestable and Independent Faults," in *Proc. 26th IEEE VLSI Test Symp.*, pp. 329–335, Apr. 2008.
- [319] M. A. Shukoor and V. D. Agrawal, "A Primal-Dual Solution to Minimal Test Generation Problem," in *Proc. 12th IEEE VLSI Design & Test Symp.*, pp. 269–279, July 2008.
- [320] W. Jiang and V. D. Agrawal, "Built-in Self-Calibration of On-Chip DAC and DAC," in *Proc. International Test Conf.*, Oct. 2008. Paper 32.2.

- [321] N. Yogi and V. D. Agrawal, "Sequential Circuit BIST Synthesis using Spectrum and Noise from ATPG Patterns," in *Proc. 17th IEEE Asian Test Symp. (ATS08)*, pp. 69–74, Nov. 2008.
- [322] F. Wang and V. D. Agrawal, "Soft Error Rates with Inertial and Logical Masking," in *Proc. 22nd International Conf. VLSI Design*, pp. 459–464, Jan. 2009.
- [323] J. D. Alexander and V. D. Agrawal, "Computing Bounds on Dynamic Power Using Fast Logic Simulation," in *Proc. 41st Southeastern Symp. System Theory*, pp. 107–112, Mar. 2009.
- [324] S. Menon, A. D. Singh, and V. D. Agrawal, "Output Hazard-Free Transition Delay Fault Test Generation," in *Proc. 27th IEEE VLSI Test Symp.*, pp. 97–102, May 2009.
- [325] S. Sindia, V. Singh, and V. D. Agrawal, "Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuits," in *Proc. 19th IEEE Great Lakes Symp. on VLSI*, pp. 69–74, May 2009.
- [326] J. D. Alexander and V. D. Agrawal, "Algorithms for Estimating Number of Glitches and Dynamic Power in CMOS Circuits with Delay Variations," in *Proc. IEEE Computer Society Annual Symp. on VLSI*, pp. 127–132, May 2009.
- [327] J. T. Tudu, E. Larsson, V. Singh, and V. D. Agrawal, "On Minimization of Peak Power for Scan Circuit during Test," in *Proc. 14th IEEE European Test Symp.*, pp. 25–30, May 2009.
- [328] M. A. Shukoor and V. D. Agrawal, "A Two Phase Approach for Minimal Diagnostic Test Set Generation," in *Proc. 14th IEEE European Test Symp.*, pp. 115–120, May 2009.
- [329] W. Jiang and V. D. Agrawal, "Designing Variation-Tolerance in Mixed-Signal Components of a System-on-Chip," in *Proc. International Symp. Circuits and Systems*, pp. 126–129, May 2009.
- [330] S. Sindia, V. Singh, and V. D. Agrawal, "Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing," in *Proc. 13th IEEE VLSI Design & Test Symp.*, July 2009.
- [331] N. Yogi and V. D. Agrawal, "BIST/Test-Decompressor Design using Combinational Test Spectrum," in *Proc. 13th IEEE VLSI Design & Test Symp.*, July 2009.
- [332] S. Sindia, V. Singh, and V. D. Agrawal, "V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non-Linear Analog Circuits," in *Proc. 7th IEEE East-West Design & Test Symp.*, (Moscow, Russia), Sept. 2009.

- [333] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Variable input delay cmos logic for low power design," *IEEE Trans. on VLSI Systems*, vol. 17, pp. 1534–1545, Oct. 2009.
- [334] S. Sindia, V. Singh, and V. D. Agrawal, "Multi-Tone Testing of Linear and Nonlinear Analog Circuits using Polynomial Coefficients," in *Proc. 18th IEEE Asian Test Symp.*, (Taichung, Taiwan), Nov. 2009.
- [335] S. Sindia, V. Singh, and V. D. Agrawal, "Parametric Fault Diagnosis of Nonlinear Analog Circuits using Polynomial Coefficients," in *Proc. 23rd International Conf. on VLSI Design*, (Bangalore), Jan. 2010.