

# Low Cost Launch-on-Shift Delay Test with Slow Scan Enable (*ETS06*)

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# Outline

- Transition Delay Test (Launch-on-Shift, Launch-on-Capture)
- The issue of LOS: requiring fast scan enable signals
- Current approach I: Pipeline structure methods
- Current approach II: Partial-shift-partial-capture methods
- Other approaches: Hybrid method and Enhanced Scan method
- Our solution: Using Delay Test Scan Flip-flops with slow scan enable signals

# Transition Delay Test

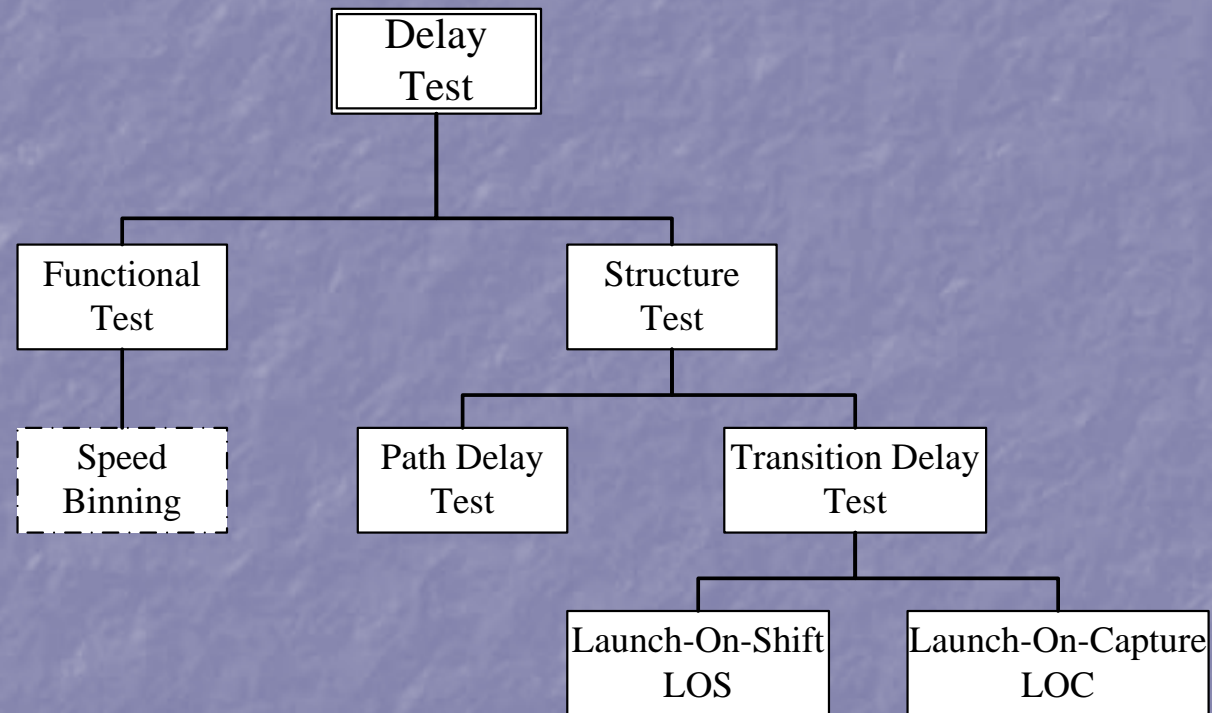


Figure 1: Classification of Delay Test

# LOS & LOC Delay Test

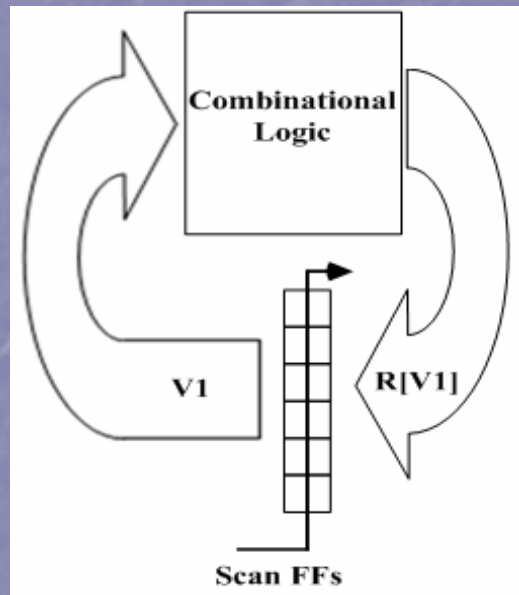


Figure 2: Overview of scan based delay testing

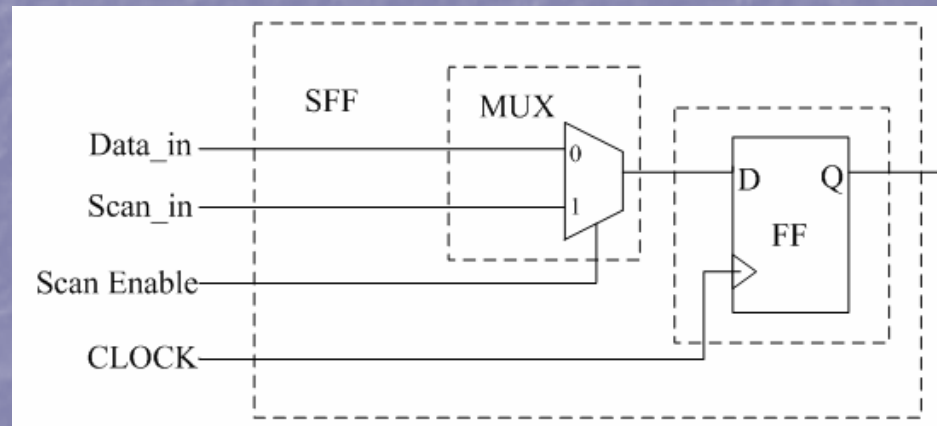


Figure 3: Multiplexer based scan flip-flop

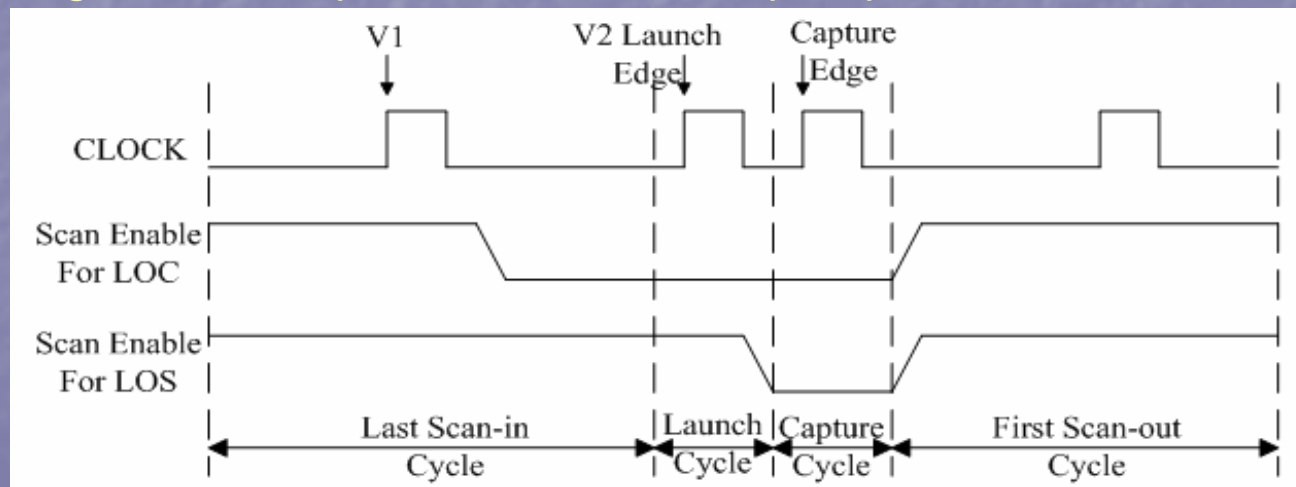


Figure 4: Waveforms for LOS and LOC delay test

# LOS & LOC Delay Test

	Launch-on-Shift (LOS)	Launch-on-Capture (LOC)
Advantage	<ul style="list-style-type: none"><li>1) High fault coverage</li><li>2) Few test patterns</li><li>3) Combination ATPG</li></ul>	<ul style="list-style-type: none"><li>1) No requirement for fast scan enable signals</li></ul>
Disadvantage	<ul style="list-style-type: none"><li>1) Requiring fast scan enable signals</li></ul>	<ul style="list-style-type: none"><li>1) Medium fault coverage</li><li>2) More test patterns</li><li>3) Sequential ATPG</li></ul>

Table1: Comparison of LOS & LOC

# Issue of LOS: Requiring Fast Scan Enable Signals

- DFT design cost

High speed global scan enable signal -> routing the scan enable signal as clock signal -> DFT design cost is expensive

- Hard to meet time closure

"From our experience, the design effort involved in designing a fast SEN signal and the resulting impact on turnaround time is considered unacceptable for many designs. We believe that this concern is shared by others in the design and test community." (ref.[8])

# Approach I: Pipeline structure methods

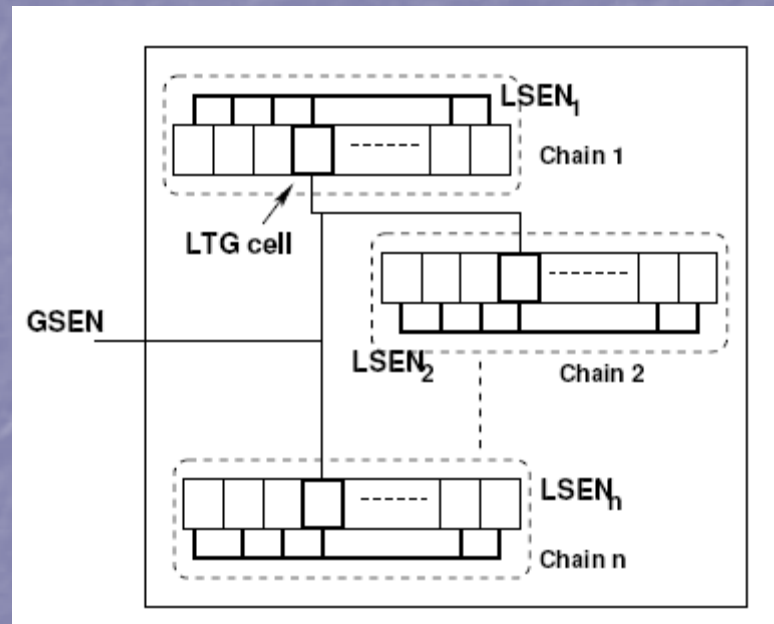


Figure 5: Test architecture

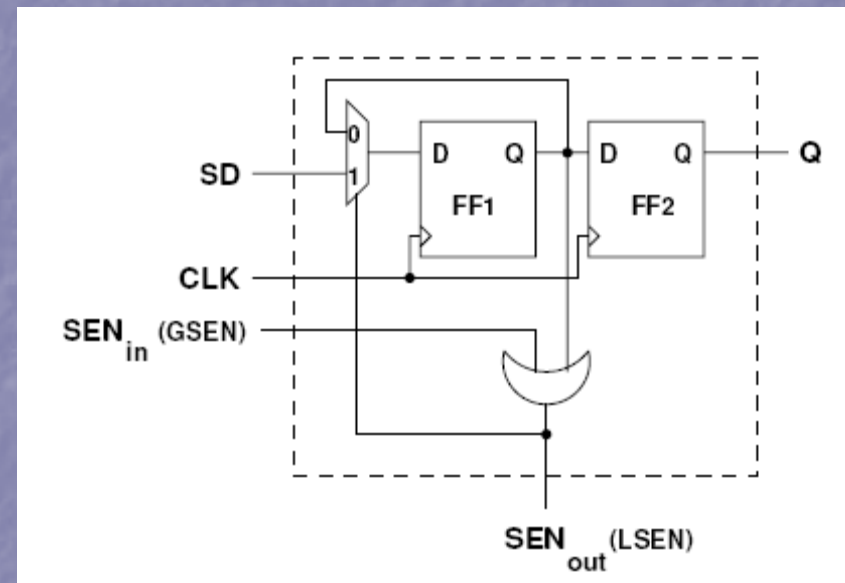
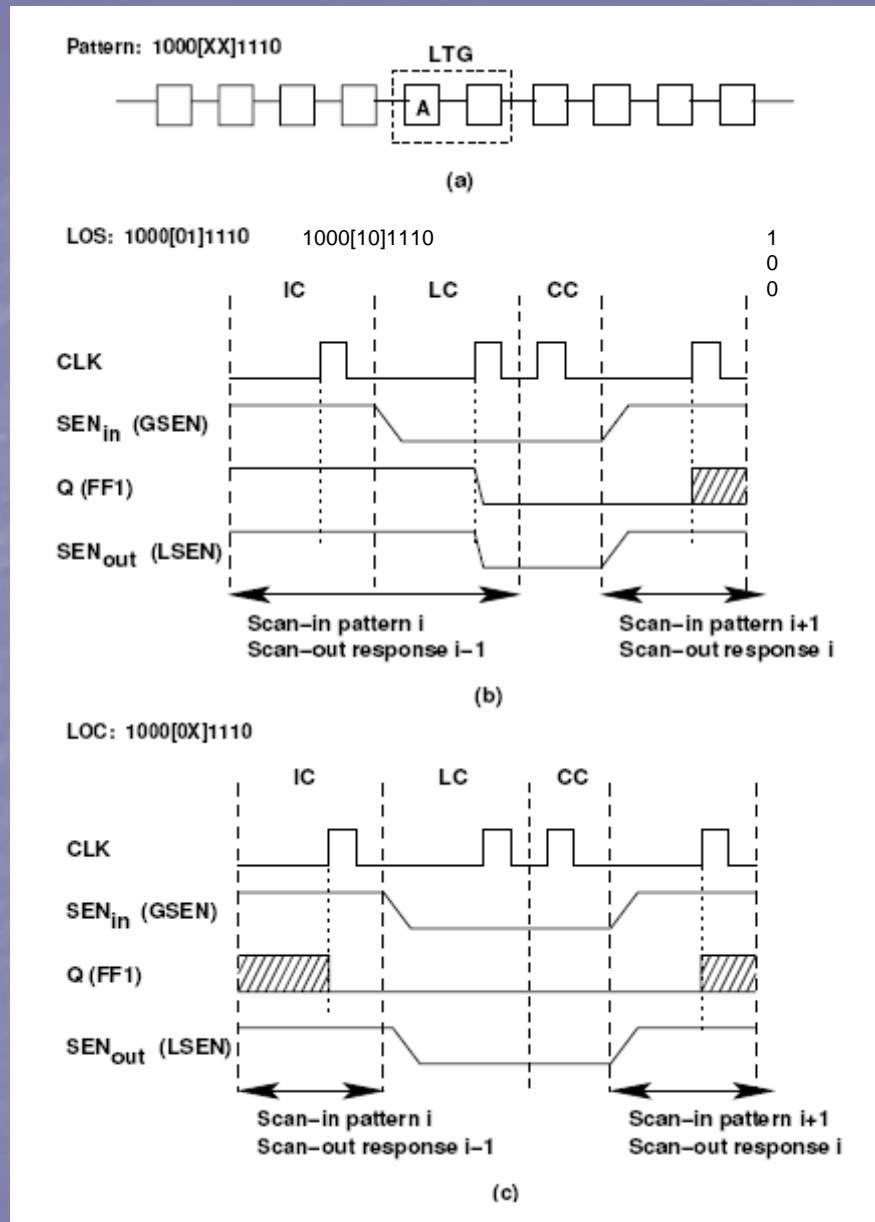


Figure 6: Last transition generator (LTG) cell



- The values in LTG cell determine the test mode (LOS or LOC).
- Both LOS and LOC test are allowed.
- Local fast scan enable signals are needed and drivability requirements for these signals are considerable.
- Timing critical signals (enable signals) complicate layout and timing closure.

Figure 7: Operation of LTG cell, (b) LOS and (c) LOC

# Approach II: Partial-shift-partial-capture methods

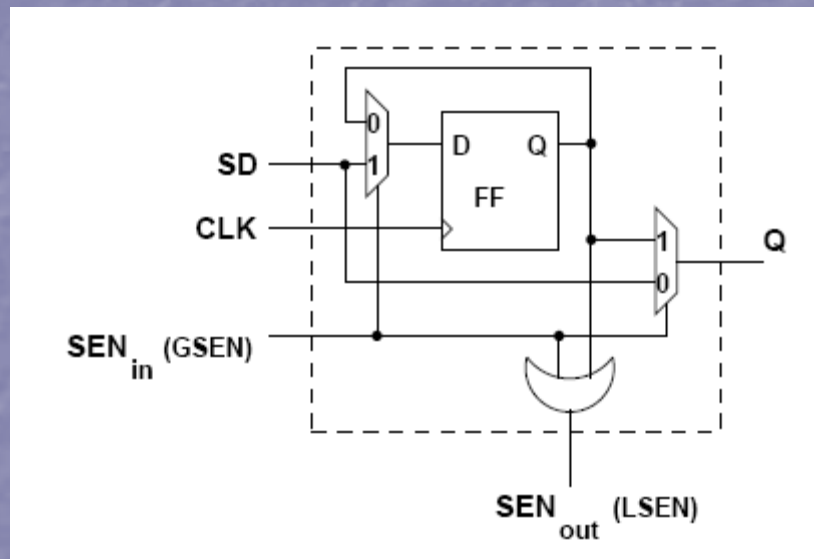


Figure 8: Modified Local scan enable generator (LSEG) cell

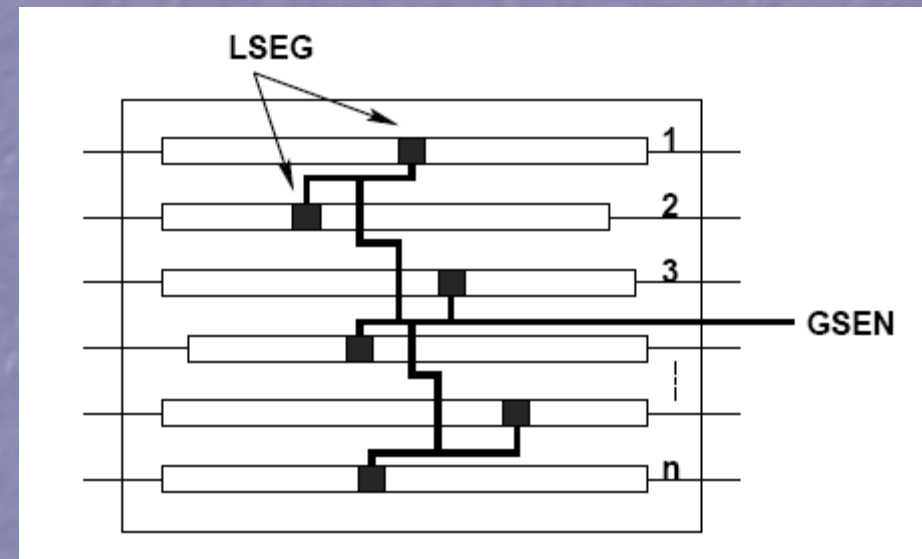


Figure 9: Test Structure

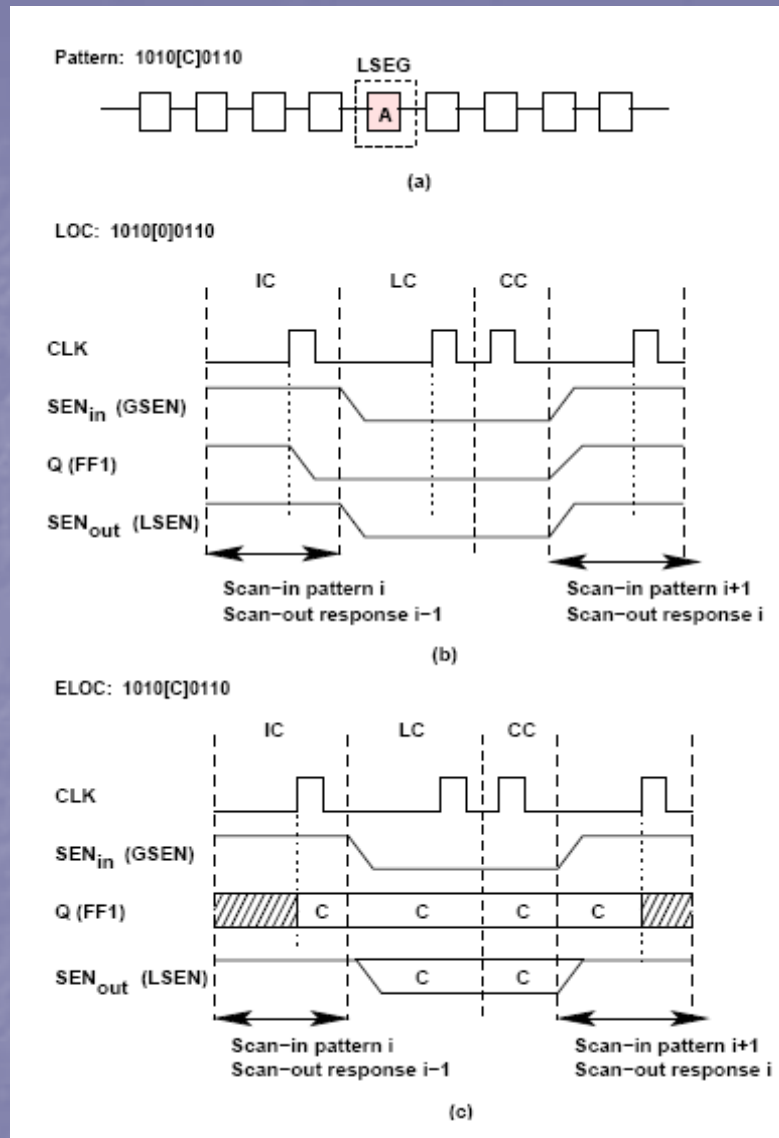


Figure 10: Operation of LSEG cell (a) Scan chain (b) Conventional LOC and (c) Enhanced LOC

- The value in LSEG determines the mode (LOC or enhanced LOC).
- LOC and enhanced LOC mode which restricts a subset of scan chain only operating in shift mode are allowed.
- Fault coverage is only a little higher than pure LOC
- Timing critical signals (enable signals) complicate layout and timing closure.

# Other approaches: Hybrid method

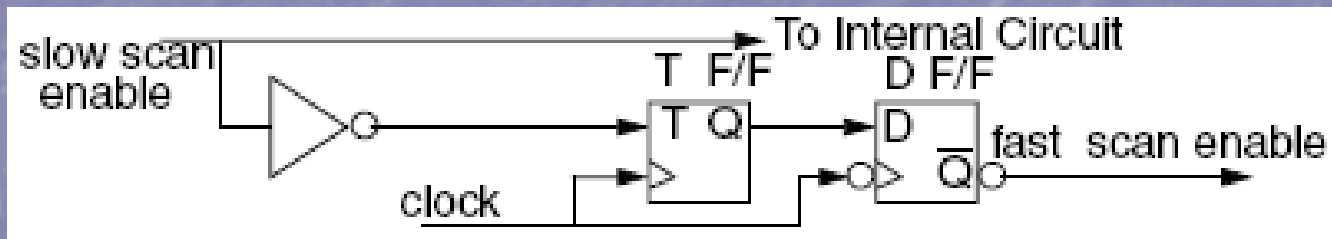


Figure 11: Fast Scan Enable Signal Generator

- Using a slow scan enable signal to generate a fast scan enable signal
- Some Scan Flip-flops are controlled by Slow Scan Enable signal and other Scan Flip-flops (few) are controlled by Fast Scan Enable signal.

# Other approaches: Enhanced Scan method

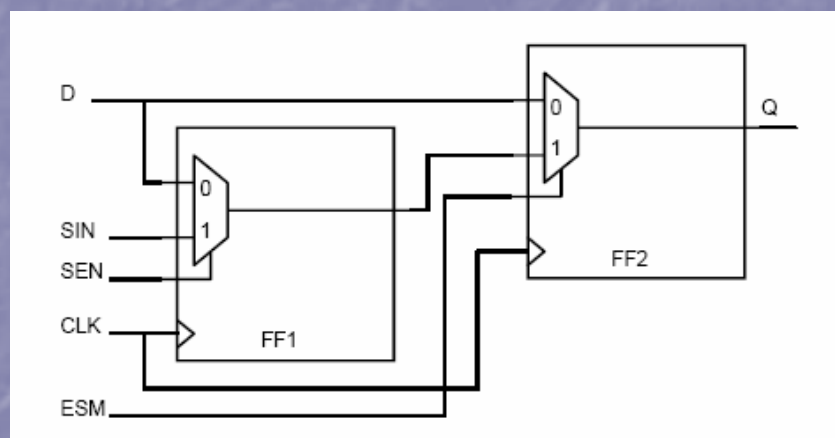


Figure 12: Dual Flip-flop

SEN	ESM	Operation of Flip-flop
0	0	Functional mode/Standard broadside test mode
0	1	Enhanced broadside test mode
1	1	Scan shift mode
1	0	Not allowed

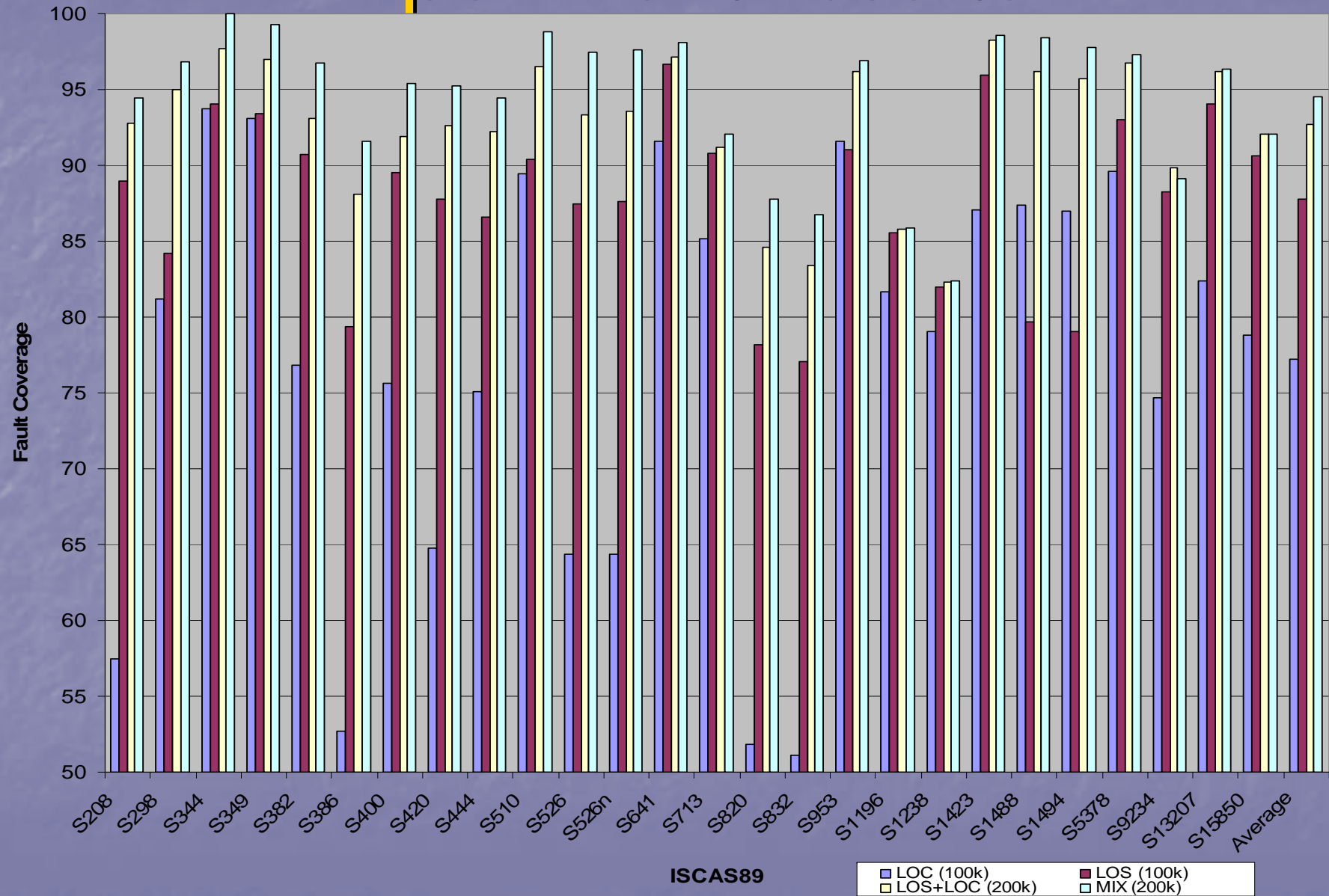
Table 2: Dual Flip-flop operation

- Double all scan Flip-flops to allow LOS and LOC
- If partial scan Flip-flops are doubled, it works as Partial-shift-partial-capture mode

# Contribution of this paper

- Designed a new structure -- Delay Test Scan Flip-flop (DTSFF) to support LOS transition delay testing
- Designed modified DTSFF (type I) to support both LOS and LOC delay testing
- Designed modified DTSFF (type II) to support mixed LOS and LOC delay testing (even higher fault coverage)

# Experiment results



# Conclusion

- Basic DTSFF allows LOS test with slow scan enable signal
- Modified DTSFF (type I & II) allow LOS+LOC test and Mix LOS/LOC test
- The overhead for DTSFF is small.
- The Fault coverage for DTSFF design is high.
- DTSFF is compatible with current EDA tools and design flows.

# Reference

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Thank you!