Solutions to Homework 2 Problems
ELEC 7250 VLSI Testing (Spring 2006)

February 6, 2006

Problem 3.2 Economic decision

(a) Let x be the daily wages of a technician and c be the cost of components on a board. When n technicians work in the assembly shop, the cost of one board is,

$$\begin{aligned} C(n) &= \frac{Warehouse\ cost}{n} + technician's\ wages + component\ cost \\ & \quad + workspace\ cost \\ &= \frac{10,000}{n} + x + c + \frac{500n^2}{n} \end{aligned}$$

To minimize this cost, we write

$$\frac{dC(n)}{dn} = -\frac{10,000}{n^2} + 1,000n = 0 \quad \text{or} \quad n = \sqrt{20} = 4.47$$

This is a minimum since $\frac{d^2C(n)}{dn^2} > 0$. We obtain the minimum cost as,

$$C(4) = C(5) = \$4,500 + x + c$$

To minimize the cost we should either hire four technicians, or reduce the workforce to five if more than five technicians were already employed.

(b) Substituting $x = 200$ and $c = 10,000$ in the last equation, we get

$$C(4\ or\ 5) = \$4,500 + 200 + 10,000 = \$14,700$$

The minimum cost of a single-board system is $14,700.

Problem 3.3 Benefit-cost analysis

Please note a correction in the statement of this problem. The part (a) should read: Show that this scheme is beneficial for chips whose total cost is less than ten times the burn-in cost when the burn-in yield is 90%. (Corrected in later printings).

(a) *Complete elimination of burn-in:* Let C_t be the total cost of a chip in the present scheme where burn-in test is applied to every chip that passes the conventional test. Let C_b be the per chip cost of burn-in. C_t includes C_b, as well as another component, C_f, which accounts for the costs of fabrication, conventional test, etc. It is given by,

$$C_t = \frac{C_f + y_c C_b}{y_c y_b}$$

where y_c is the yield with the conventional test and y_b is the yield reduction due to burn-in. Since the cost of I_{DDQ} test is 10% of the burn-in cost and there is a 10% yield loss, the cost of a chip when burn-in is replaced by I_{DDQ} test is given by,

$$C'_t = \frac{C_f + 0.1 y_c C_b}{0.9 y_c y_b}$$

For the new scheme to be beneficial, we must have

$$C'_t < C_t \quad \text{or} \quad C_t < \frac{9C_b}{y_b}$$

For the given 90% burn-in yield, $y_b = 0.9$, and $C_t < 10C_b$. **The total cost should not exceed ten times the burn-in cost.**

(b) *Apply burn-in test only to chips that fail I_{DDQ} test:* Let y_b be the burn-in yield. Consider all chips that have passed pre-burn-in tests. A fraction y_b of these is "good" chips. We apply I_{DDQ} test to all chips passing the pre-burn-in test. Due to the 10% yield loss, this will produce a fraction $0.9y_b$ consisting of good chips. The remaining fraction, $1 - 0.9y_b$, must be subjected to the burn-in test to recover the lost yield. For the new scheme to be beneficial, we must have

$$0.1C_b + (1 - 0.9y_b)C_b < C_b \quad \text{or} \quad y_b > \frac{1}{9}$$

Burn-in yield should be greater than 1/9 or 11.1%.

Problem 3.7 Defect level

Defect level, $DL(T)$, given by Equation 3.20 (p. 50 of the book), can be written as:

$$\begin{aligned} DL(T) &= 1 - \frac{(1 + TAf/\beta)^\beta}{(1 + Af/\beta)^\beta} \\ &= 1 - \frac{e^{TAf}}{e^{Af}} = 1 - e^{-Af(1-T)}, \quad \text{as} \quad \beta \to \infty \end{aligned}$$

Also, as $\beta \to \infty$, Equation 3.19 (p. 50 of the book) gives the yield,

$$Y = \left(1 + \frac{Af}{\beta}\right)^{-\beta} = e^{-Af}$$

Substituting this expression for yield in the defect level, we get

$$DL(T) = 1 - (e^{-Af})^{1-T} = 1 - Y^{1-T}$$

which is the required result.