SCAN BASED DELAY TESTING

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***Abstract**:* - Scan Based Delay Testing is used to perform delay testing in the sequential circuits which have the scan capability. In this paper, basics of delay testing and several techniques to perform delay testing for scan based circuits are discussed. The construction of several scan flip-flops along with their advantages and disadvantages is also presented.

1. INTRODUCTION

High speed performance has been given the highest priority for the current day digital circuits. As the size of the transistors is decreasing, the speed at which the chips are being operated is increasing. So, delay fault testing has become an important means to verify quality requirements of digital circuits. The main reason to perform delay testing, is to verify whether the signal transition reaches the outputs or to the internal flip-flops within the specified time period. If the delay in the signal transition exceeds the expected time period, a faulty value is seen at the output at that particular instance or a false value could be latched up in the flip-flop.Because the circuit has to be operated at high frequency to perform delay test, delay testing is also known as AC testing. Considering the stuck-at faults, it is difficult to test sequential circuits compared to the combinational circuits. The same is the case for delay testing also. So, people have started using the scan design to perform delay testing, which was introduced primarily to improve the fault coverage due to the stuck-at fault tests. Scan based delay testing is also used to performed speed binning of chips.

As the size of the circuits keeps increasing and the feature sizes keep decreasing, no. of connections in the circuit and the probability that minor defects (due to over etching, under etching, etc.) increase. These increase the overall probability of occurrence of the delay defects in the circuit. So, delay test is one of the areas where advancements are necessary to reduce the test time and the area overhead.

2. BACKGROUND

Delay faults are caused when a net functions properly but fails to meet timing requirement. Delay faults are sometimes caused by the defects that are not large enough to cause a stuck-at failure by changing logic level, but affect the signal propagation time [1]. Signal propagation time may be affected due to manufacturing defects and random variation in process [2]. The manufacturing defects include under- or over-etching during the fabrication process, which produces Metal Oxide Semi-conductor Field Effect Transistors with channel widths that are much narrower or channel lengths that are much longer than intended. Therefore, some paths through the circuits may not meet the performance specifications of the device [3]. The other factors which may contribute to the propagation delay of the circuit are the device parameters, routing capacitances, switching delay of the circuit and the transport delay of the interconnects. The propagation delay is the time that a single event takes to traverse a path [4]. The goal of delay testing is to find and expose any of these defects that may exist in a fabricated device.

In order to examine the timing operation of a circuit signal transitions should be examined. So, the input signal consists of a pair of vectors. The first vector is used to initialize the circuit to a known state and the application of the second vector detects the fault. Considering all possible input vector-pairs, “the longest delay combinational path” of the circuit is known as the critical path. The delay of the critical path determines the smallest clock period at which the circuit can function properly. For any circuit to function correctly, the output transition region for any vector pair combination should not exceed the clock period [4].

Mainly two types of delay fault models have been popular: Gate delay fault [5] and Path delay fault [6]. The gate delay fault model is a localized fault model in a sense similar to the stuck-at fault model. The gate delay fault is assumed to be either associated with a gate input or a gate output. If a slow-to-rise delay fault is associated with a gate input, any logic 0-to-1 transition at that input will be delayed by a magnitude equal to the size of the delay fault. Thus, each delay fault has two attributes associated with it: the type of transition it affects (rising transition or a falling transition) and the magnitude (the amount by which an affected transition is delayed). Each line or net can potentially have two types of delay faults associated with it: a slow-to-rise (STR) fault (delays the rising transition) and a slow-to-fall (STF) fault (delays the falling transition) [7]. These faults are also known as “Transition Faults”. For detecting a STR fault on a line, the test for stuck-at-0 on that line is considered. This test will set the line to 1 in the fault-free circuit and propagate the sate of the line to a primary output, let this vector be V2 and it is preceded by another vector V1 which sets the line to 0. This vector pair (V1, V2) is a test for the STR transition fault

on that line. Similar vector pairs can also be found for STF faults. The major disadvantage of this model is that the defects due to the cumulative effects of small delay variations from primary inputs to primary outputs may not be captured [4].

Path-oriented delay fault models overcome this disadvantage. In path delay fault models, the cumulative delay of various gates in a path is considered as a test parameter. The transitions from 0-1 and 1-0 are propagated along a path from the primary inputs to the primary outputs. If the cumulative delay exceeds the slack for the path, then the chip fails [8]. In any circuit, *slack* of a path can be defined as the difference between the clock period when the circuit outputs are latched and the propagation delay of the path under consideration. To cause an incorrect value to be latched or to appear at a circuit output, the size of the delay fault must be such that it exceeds the slack of at least one path from the fault site to an output pin or scan flip-flop [9].

In path delay tests, a set of paths is selected such that at least one path in the set will exhibit maximum modeled delay. In an arbitrary circuit, there are a large number of possible paths from the inputs to the outputs. The size of one path may significantly differ from others. Generally the longest (called critical path) is examined [8]. If the propagation delays of all paths passing through a particular fault site exceed the clock period, such a fault is referred to as a *gross delay fault* [7].

Like single stuck-at faults and multiple stuck at faults, there are two kinds of path delay faults. They are

1) Single Faulty Path: - If only one path is faulty then it is known as single faulty path.

2) Multiple Faulty Paths: - If more than one path in a circuit is faulty then they are called multiple faulty paths. In this case, sometimes, the two defects may cancel out each other and no fault may be observed.

The single faulty path defects can be tested with non-robust delay tests. In the case of multiple stuck-at fault tests as one fault can cancel another fault we need robust delay tests. Non-robust path delay test guarantees to detect a path-delay fault, when no other path-delay fault is present. i.e., the path delay fault for which a non-robust test exists is called a "singly-testable path-delay fault [10]," Whereas, a robust path-delay test guarantees to produce an incorrect value at the destination, if the delay of the path under test exceeds a specified time interval (clock period), irrespective of the delay distribution in the circuit [4].

Among these fault models, the transition delay fault model is most widely used in industry for its simplicity. Automatic Test Pattern Generators and fault simulators that are developed for stuck-at faults can be reused for transition delay faults with minor modifications. Unlike the path delay fault model where the number of target faults is often exponential, the number of transition delay faults is linear to the number of circuit lines. A *line* is a connection between any two gates with no gates in between.

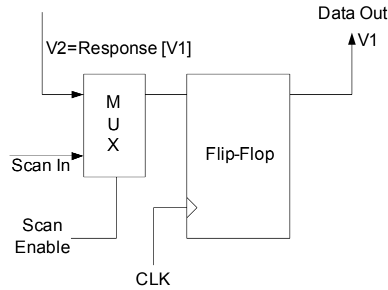
Till this point, several causes for delay defects, different types of delay defects and their definitions have been discussed. In the further sections, description of three important scan based techniques Launch from capture, Launch from shift, Enhanced scan test are discussed in section. A new improved enhanced scan test which reduces the area and delay overhead is discussed in section 4 and finally the paper is concluded in section 5.

3. Scan Based Delay Test Techniques

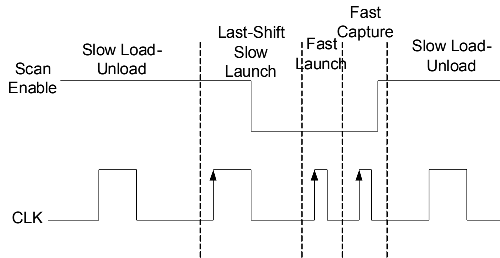
Economics and time-to-market pressures are forcing chip designers and production test engineers to learn and use structural test techniques such as scan, logic BIST, built-in vector compression, and AC scan. In the past few years, structured scan-based methods, most often full-scan, are being increasingly used to generate test patterns that are capable of achieving high fault coverage. The advantage lies in the short cycle time for ease in debugging them. Test application times may not be short if many flip-flops are included in long serial scan chains. Designers often make use of multiple parallel scan chains to reduce the test application time. However, as design sizes increase, most types of automatic test equipment (ATE) are incapable of supporting the increased number and depth of scan chains. Scan based methods still remain the most viable alternative to for delay tests and many improvements are being devised for such methods [13] [14].

3.1. Launch from Capture

Launch from capture technique is also known as the "broad-side" or "functional justification" technique. As already said, transition fault tests require a pair of vectors - one to set a target node to an initial value and the next to launch the transition and propagate the effect to a primary output or scan cell [5], [11]. In this technique, the first vector of the pair is scanned into the chain and the second vector is derived as the combinational circuit's response to the first vector [12].



a) Flip-Flop set-up



b) Timing Wave Form

Fig.1 Operation of Launch on Capture

Fig. 1.a. shows the flip-flop required to perform Launch on Capture. In a scan-based design, if the scan chain contains N cells, a vector pair is obtained by applying the following steps:

1) Data is shifted into the scan-chain N times. This will be the vector V1 which is applied at the first clock edge shown in Fig 1.b. Then 'Scan Enable' is changed to 0.

2) At the clock edge 2, the response of V1 is captured in the flip-flop to launch the timed transition, this is vector V2.

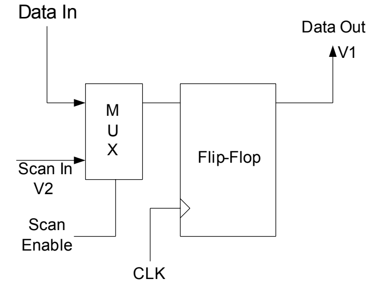
3) At the clock edge 3, the response of V2 is captured.

The important point to note here is that the launch and capture are performed with the scan-enable signal set to functional mode and the scan-shift frequency is much slower than the functional operation frequency in most industrial designs. Also the scan-shift speed may also be limited by the maximum frequency supported by the tester hardware being used.

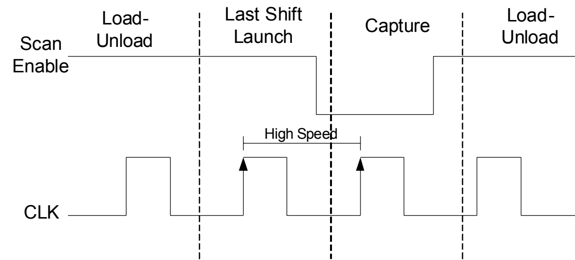
3.2. Launch from Shift

This technique is also known as the "Skewed-Load" or "Transition Shifting" technique. Here, both the first and second vectors of the pair are delivered through the scan cells themselves [12].

The inputs applied at the inputs of the multiplexer are different from Launch from capture and are shown in Fig 1.b. In a scan chain containing N cells, this approach consists of the following steps:



a) Flip-Flop set-up



b)Timing Wave Form

Fig.2 Operation of Launch on Shift

1) Data is shifted into the scan-chain required number of times to obtain the first vector in the vector pair.

2) At the first clock edge V2 is launched (Scan Enable=1). V2 is obtained by scanning a bit into the last flip-flop. Then Scan Enable is switched to 0 as shown in Fig 2.b.

3) At the second clock edge the response due to V2 is captured.

Most designs consist of a muxed data scan cell as shown in the figs 1.a. and 1.b., where a multiplexer (mux) is used to choose between the value from the combinational logic and the value from the scan-chain. The scan-enable signal is used to control this mux. The most important difference between the two techniques described above with respect to muxed data scan designs is the need for at-speed scan-enable operation in the launch-from-shift technique. Further, the launch-from-capture technique requires a sequential ATPG algorithm, while launch from-shift patterns can be generated with a purely combinational ATPG algorithm.

In Launch on Last Scan, the Mux-Scan "Scan Enable" signal must be toggled after the launch clock edge and before the capture clock edge. This is not always easy because Scan Enable is rarely timed and skew controlled as well as the clocks. If there is both positive and negative edge clocking, the timing of that toggle becomes even more difficult. As a result, Launch on Last Shift is used relatively infrequently in the mux-Scan architecture. It is relatively easy to use in Level Sensitive Scan Design (LSSD), where the launch and

capture clocks are separately controlled, allowing the test pattern generator more flexibility [16].

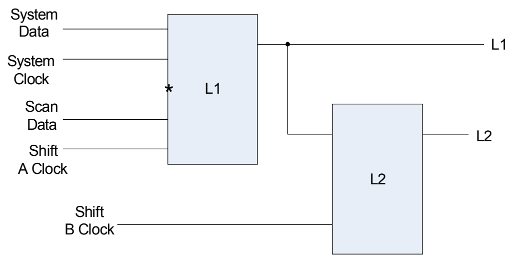


Fig.3 LSSD Flip-Flop Implemented as Shift Register Latch

All latches in LSSD are implemented as part of a Shift Register Latch (SRL) as shown in Fig. 3. The latch pair (L1 and L2) has two inputs: system data is gated into L1 using system clock and scan data is gated into L1 using shift A-Clock. The L1 value is gated into L2 using the shift B Clock. The asterisk (*) in Fig. 2 denotes logic pin group separation. Using this convention, the System Clock is understood to operate on the System Data, and the Shift **A-**Clock is understood to operate on the Scan Data. All SRLs are chained together into one or more shift register strings. As a benchmark for overhead analysis, the SRL shown in Fig. 3can be implemented using 10 NAND gates and 2 Inverters. Its CMOS implementation cost is much lower and the circuit is shown in Fig. 4. Because of the absence of skew in the clock signals, Launch on Shift can be performed without any problem using LSSD.

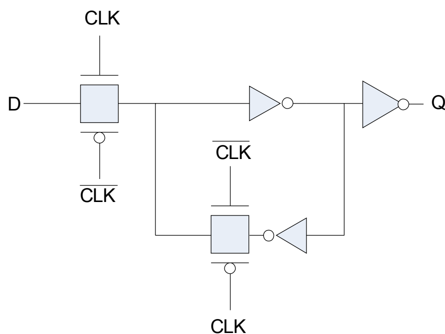
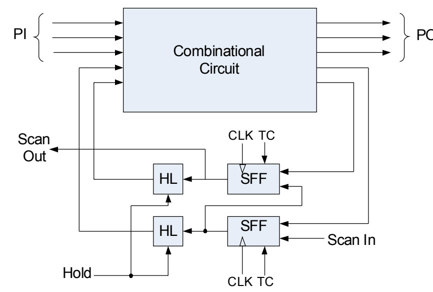


Fig.4 Latch implementation in MOS

3.3. Enhanced Scan Test

In enhanced-scan test technique, two vectors (V1, V2) are stored in the tester scan memory. The first scan shift loads V1 into the scan chain. It is then applied to the circuit under test to initialize the circuit. Next, V2 is scanned in, followed by an apply and a subsequent capture of the response. During shifting in of V2 it is assumed that the initialization of V1 is not destroyed. Therefore enhanced-scan transition testing assumes a hold-scan design [14].



PI/PO – Primary Inputs/Primary Outputs
HL – Hold Latch
SFF – Scan Flip-Flop
TC – Test Control

Fig. 5 Enhanced Scan Flip-Flop

The architecture of the enhanced scan flip-flop is shown in Fig. 5. Enhanced scan transition test has two primary advantages: coverage and test data volume. Since enhanced scan testing allows the application of any arbitrary vector pair to the combinational part of a sequential circuit, complete fault coverage can be attained.

Tester memory requirement is also important issue, and considerable attention is being paid to reduce the tester memory requirement for stuck-at tests. The problem is far worse for transition tests. In [15] it was reported that for skewed load transition tests for an ASIC, the stuck-at vector memory requirement was 8.51M versus 50.42M for transition test. This implies an increase of a factor of 5.9.

The downside of using enhanced-scan transition test is that special scan design, viz. hold-scan cell that can hold two bits, is required. This may lead to higher area overhead, which may prevent it from using widely in ASICs. However, in microprocessors and other high performance circuits, requiring custom design, such cells are used for other reasons. In custom designs, when the circuit is often not fully decoded, hold scan cells are used to prevent contention in the data being shifted, as well as preventing excessive power dissipation in the circuit during the scan shift phase. The excessive power dissipation is occurred due to unnecessary transitions in the circuit which are occurred during shifting. Furthermore, if hold-scan cells are used, the failing parts in which only the scan logic failed can often be retrieved; thus enhancing, to some extent, the diagnostic capability associated with scan DFT. Therefore, for such designs enhanced-scan transition tests is preferred.

Among the three approaches for applying delay tests, broadside-delay test suffers from poor fault

coverage [12]. In Enhanced scan test, there is no dependency between the two vectors and so it can give better coverage than skewed-load transition test. Skewed-load transition tests also lead to larger test data volume. Compared to stuck-at tests, the increase in the number of vectors required for enhanced scan to get complete coverage is about 4X [16]. For skewed-load transition test, it has been observed that the data volume for an ASIC has an increase of 5.9X [15]. For most circuits, test sets generated by the skewed-load approach achieve higher fault coverage than those generated by the broadside approach [17]. Sizes of test pattern sets generated by the skewed-load approach are also typically smaller than those generated by the broad-side approach [18]. However, the skewed-load approach requires higher hardware overhead and may require longer design times

4. Novel Extended Scan Based Delay Testing [1]

This technique, referred as First Level Hold (FLH) employs the principle of "supply gating" to hold the state of combinational logic. Instead of holding the initialization pattern at the scan hold latch as done in the case of enhanced scan, the state of the combinational circuit is held in response to the first pattern by gating the VDD and GND of the first level logic gates. Test application remains as in enhanced scan approach, except that the control for holding state is now moved from the hold latches to the gating control of the first level of the logic gate.

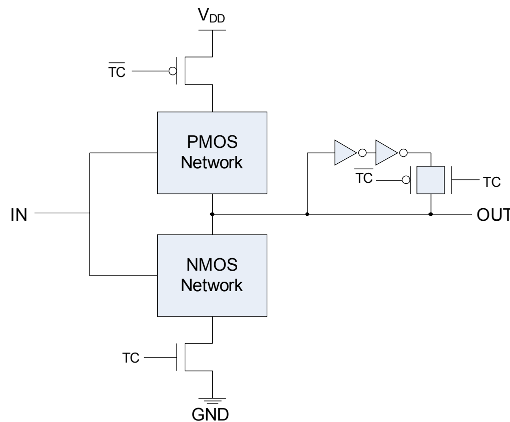


Fig.6 Supply Gating Scheme with Output Hold Capability

The general scheme of the proposed supply gating scheme is shown in Fig. 6. The two inverters, , form a cross-coupled inverter loop if the transmission gate is closed. In the sleep mode (TC='0'), the transmission gate is closed and the inverter loop holds the state of the output node. In the normal mode (TC='1'), however, the transmission gate is open and the gate can control its output. Therefore, in this scheme, the output of the gate never gets floated and there cannot be any static short circuit current on the next stage gates in the sleep mode. The proposed scheme is called "First Level Hold (FLH)" since only the first stage is set in the hold mode.

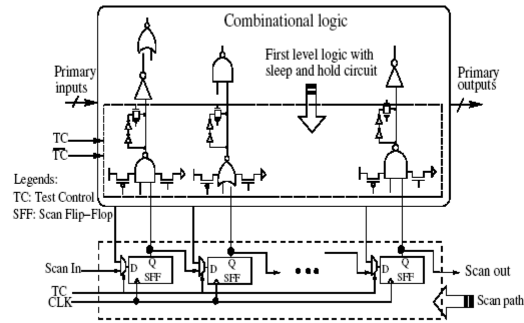


Fig. 7 Implementation of Supply Gating Scheme

The actual implementation of first level hold is shown in Fig. 7. The main idea in this technique is to store the charge which indicates the logic value of the previous state. When TC=0 there is no path for the charge stored in the inverters to be discharge. Thus the previous state is retained. When this enhanced scan flip-flop is implemented in ISCAS 85 benchmark circuits a reduction of 33% in area overhead, average improvement of 71% in delay overhead and 90% in power overhead during normal operation are observed.

5. Conclusion

Basics of Delay testing including the causes for delay defects and different kinds of delay tests are introduced. Architecture of different scan based delay techniques along with their advantages and disadvantages have been explained. And a new architecture for Enhanced Scan Based delay testing which reduces the area, delay and power overheads is also explained. Scan based delay testing techniques consume more time and memory than normal stuck-at fault testing techniques.

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