

# Random Access Scan

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## Abstract:

*Random Access Scan, the alternate scan Architecture has begun to gain acceptance in the recent past because it addresses the problems encountered in serial scan such as the “test application time” and the “power consumption”. Consumption of power during testing is much higher than compared to the normal circuit operation. It is important to keep the power dissipation to a minimum level, which may otherwise damage the circuit. The (SS) Serial Scan induces unnecessary circuit activity, which may dissipate enormous amount of power in the circuit under test. This paper aims at bringing the idea behind the Random Access Scan, its design methodology and its advantages.*

## Introduction:

The greatest challenge faced by today's VLSI world is testing sequential circuits. Scan based methodologies are being implemented for testing purposes. The goal of Scan design is to achieve complete or almost total controllability and observability in sequential circuits. In normal mode the flip-flops and latches are configured for parallel operation. In test mode, the flip-flops and latches are loaded by serially clocking in the desired data. Of the available scan based designs, (SS) Serial Scan has been known to be the most successful. But due to the presence

of some inherent drawbacks like increased test time, and power consumption research was on for a substitute for this (SS) technique. Several methods were suggested to substitute (SS) Serial Scan based design, one of them was Partial Scan but the cost associated with Partial Scan design was high [1]. The long scanin/scanout may lead to increase in circuit activity, which eventually increases the power consumption. Test scheduling was adopted to avoid the damage of the device due to high power dissipation. With the frequent transitions in the scan chain the serial scan based design induce undesirable activity, which increases the power consumption [2,3]. To counter this problem we slow down the scan clock but end up increasing the test application time, which is undesirable.

The power dissipation issue was targeted by using ATPG based methods [4] but eventually it increased the test sequence length, which led to compaction of test sequence. But the compaction of test sequence doesn't seem to solve the problem since it increased the activity of the circuit there by increasing the power consumption [5]. Different techniques have been proposed to counter the power dissipation and increased test sequence problem, these are

1. Test Vector Ordering,



Figure 3. gives a system perspective of the random-access scan technique. SDI scans data in for the addressed latch, and SDO scans data out for the addressed latch. The test hardware comprises of an X and a Y Decoder and the addressable storage elements (the random-access scan cells) as seen in Figure 3. The random-access scan technique provides observability at any point in the combinational network. The random-access scan approach requires about three to four gates per storage element compared to two latches for every point in the scan path approach or the LSSD approach [13]. Implementing this approach requires 10 to 20 I/O pins. Using a serial approach for the scan address, which leads to a six pin I/O overhead, could reduce the pin overhead.

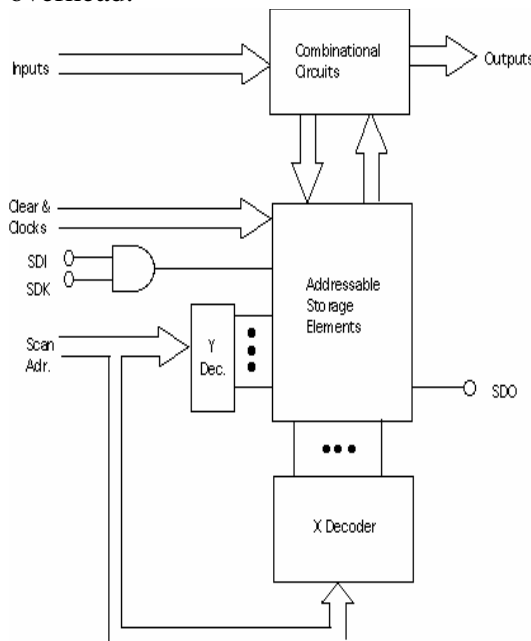


Figure3. Random-Access Scan System [13].

### 3. Features of Random Access Scan: [8]

- Uses addressable latches.

- Provides random access to FF's via multiplexing—address selection.
- Fast; minimal impact on normal path.
- Fast for testing—random access.
- Ability to 'watch' a node in normal operation mode (impossible with LSSD).
- Address decoder—and thus area overhead—is large.
- More pins added (parallel address).
- No asynchronous circuits.

### 4. Routing:

The conventional architecture given in Figure1, controls any flip-flop with the use of 3 signals apart from the signal feeding in from the combinational logic, which could be otherwise substituted with a decoder which serves the same objective of selecting the flip-flops. Also the design becomes cumbersome, as a single wire has to be routed through each of the flip-flops present.

A more feasible design had been proposed. The grid architecture shown in Figure 4 was found to be the most efficient way to layout the decoders. The total number of extra routes added is  $m + n$ . With a minimum of two layers of metal routing, the row wires can be accommodated within the channel in between the cell rows and the column wires can be routed over the cell in the next metal layer. Hence there will be an increase of one track per channel (assuming  $m$  channels) and  $n$  tracks that are routed on the next metal layer [9].

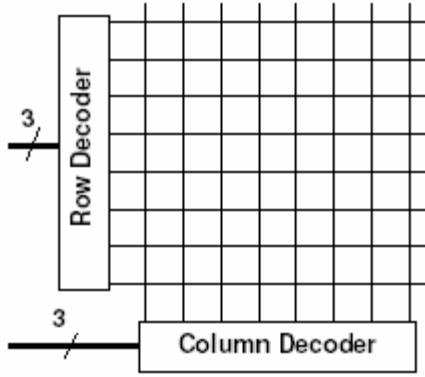


Figure 4. Decoder Design

## 5. Overhead of Scan design:

The use of scan design has two types of penalties. The scan hardware increases the chip size (area overhead) and slows down (performance overhead).

*Gate overhead:* Suppose a circuit has  $n_g$  gates and  $n_{ff}$  flip-flops, then the gate overhead of the scan is given by the equation below. More accurate estimate must consider scan wiring and layout area. The number of transistors required to decode ' $\log_2 c$ ' lines to ' $c$ ' lines approximately equals to  $2 * c$ . Assuming that a gate is made up of 4 transistors and  $n_{ff} = c$  (*horizontal lines*) \*  $d$  (*vertical lines*), the gate overhead of RAS can be approximated as,

$$\text{Gate overhead of RAS} = \frac{6 \times n_{ff} + \frac{c+d}{2}}{n_g + 10 \times n_{ff}} \times 100\%$$

*Performance overhead:* Scan design also has a performance overhead. The multiplexer of the scan flip-flop adds delay equivalent to two gate-delays in all clocked paths. In general, scan design can reduce the clock speed by 5 to 10% this results in reduced performance penalty [9,10].

## 6. Reduction in Scan operation:

The total number of RAS operations is proportional to the number of flip-flop transition and the test data length. To reduce the RAS operation two methods have been proposed 1) "test vector ordering, 2) hamming distance reduction"[7].

### 6.1 Test vector ordering:

Test vector ordering with vector repetition has been presented as a method to reduce the average as well as the peak power dissipation of a circuit during testing. Experimental results validate that the proposed technique achieve considerable savings in energy and average power dissipation while reducing the length of the resulting test sequences compared to the original method [11].

### 6.2 Hamming distance reduction:

Based on re-ordering of the test-pair sequences, the switching activities of the circuit-under-test during test application can be minimized. Hamming distance between test-pair is defined to guide test-pair re-ordering. It minimizes power dissipation during test application without reducing delay fault coverage. Experimental results have been presented to demonstrate a reduction of power dissipation during test application in the range from 84.69 to 98.08% [12].

## 7. Testing of the circuit:

It is found to detect all SAF in the circuit. The decoder is tested for faults initially, then the flip-flops are cleared by clear operation and test is performed on them. Once the circuit is tested for fault free condition the flip-flops are set up to perform routine test [9].

## 8. Results:

The benchmark circuits were tested with the RAS based design and found that the fault coverage were found to be the same as that of the SS method and there was an reduction in test sequence length and test time. The reduction in power dissipation is tabulated for both SS and RAS based design and it is found that as the size of the circuit increases the reduction in power dissipation is found to rise till 99% [9].

| Circuit | No. of FFs | No. of Combi. vectors | No. of clock cycles in SS | No. of clock cycles in RAS | Test time red. (%) |
|---------|------------|-----------------------|---------------------------|----------------------------|--------------------|
| s208    | 8          | 64                    | 584                       | 301                        | 48.46              |
| s349    | 11         | 42                    | 687                       | 366                        | 46.72              |
| s386    | 6          | 138                   | 972                       | 450                        | 53.70              |
| s420    | 16         | 128                   | 2192                      | 1056                       | 51.82              |
| s510    | 6          | 110                   | 776                       | 344                        | 55.67              |
| s641    | 19         | 142                   | 2859                      | 1148                       | 59.85              |
| s838    | 32         | 240                   | 7952                      | 3595                       | 54.79              |
| s1196   | 18         | 344                   | 6554                      | 2447                       | 62.66              |
| s1269   | 37         | 118                   | 4521                      | 1981                       | 56.18              |
| s3271   | 116        | 264                   | 31004                     | 12540                      | 59.55              |
| s3384   | 183        | 260                   | 48759                     | 21119                      | 56.69              |
| s5378   | 179        | 618                   | 111419                    | 48677                      | 56.31              |
| s13207  | 638        | 1138                  | 727820                    | 309132                     | 57.53              |

Table 1: Results of Vector Compaction for various Benchmark Circuits [9].

| Circuit | No. of Transitions in SS tests | No. of Transitions in RAS tests | Test power saving (%) |
|---------|--------------------------------|---------------------------------|-----------------------|
| s208    | 1866                           | 1209                            | 35.21                 |
| s349    | 4755                           | 1233                            | 74.07                 |
| s386    | 2495                           | 1515                            | 39.28                 |
| s420    | 11587                          | 4708                            | 59.37                 |
| s510    | 3141                           | 2382                            | 24.16                 |
| s641    | 27715                          | 7924                            | 71.41                 |
| s838    | 72914                          | 17782                           | 75.61                 |
| s1196   | 57409                          | 10601                           | 81.53                 |
| s1269   | 77755                          | 7880                            | 89.87                 |
| s3271   | 1744149                        | 45971                           | 97.36                 |
| s3384   | 4299362                        | 77665                           | 98.19                 |
| s5378   | 8947677                        | 175710                          | 98.04                 |
| s13207  | 230176409                      | 211048                          | 99.91                 |

Table 2: Power estimation based on number of transitions at the inputs for various Benchmark Circuits [9].

## 9. Conclusion:

Random Access Scan has gained importance due to the disadvantages in SS. It is found to address both “power dissipation” and “test time”, which was drawback of Serial Scan. Experimental results show that it is better than the conventional serial scan though it suffers from area overhead.

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