CIRCULAR BUILT-IN SELF-TEST

By

Sudheer Vemula
Electrical and Computer Engineering Dept.
Auburn University
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ABSTRACT: - A program to implement Circular BIST for any circuit described in Auburn Simulation Language (ASL) has been developed. Circular BIST has been implemented for the circuit S5378 and the fault simulation results have been analyzed. The code is written in 'C'- Language and ASL tools have been used to convert the circuit net list from HITEC to ASL. Fault simulation is performed using Auburn University Simulator (AUSIM).

INTRODUCTION:-

The basic idea of BIST is to make the circuit test itself. The difficulty to test the VLSI chips has been increasing continuously. The number of I/O pins for most VLSI devices has increased by an order of magnitude where as the number of transistors has increased by four orders of magnitude. In-circuit testing of most circuits became infeasible because of the introduction of the surface mounted components, where the components are placed on both sides of the Printed Circuit Board (PCB). The cost of the test equipment is increasing as they are required to handle larger no. of I/O pins, higher operating frequencies, and are required to generate larger sets of test vectors. All the above mentioned difficulties can be minimized by the implementation of BIST in the circuits.

In order to implement BIST we need to include extra circuitry. The extra circuitry consists of Test Pattern Generator (TPG), to generate the test patterns, the Output Response Analyzer (ORA), to compact the test results and the Test controller to control the test.

BASIC BIST ARCHITECTURES:-

Built-in Logic Block Observer (BILBO) was the first BIST approach that was proposed and was widely used. Its architecture is as shown in the fig.1. This BIST structure was implemented by converting the normal flip-flops in BILBO flip-flops. The BILBO structure is used both as a TPG and ORA. This can be operated in four modes of operation as given in table 1.

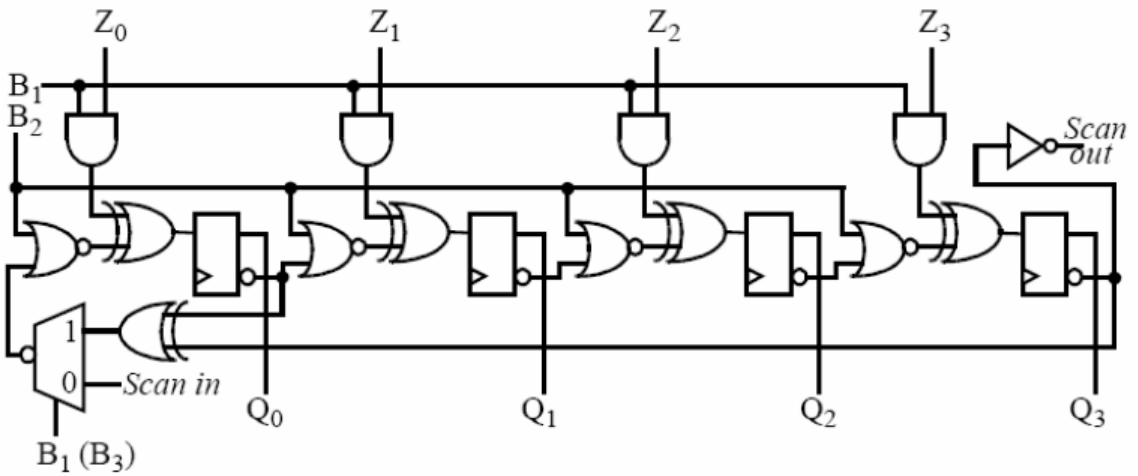


Fig. 1 Built-in Logic Block Observer

B2	B1	Mode of Operation
0	0	Shift (scan) mode
0	1	MISR (BIST) mode
1	0	Initialization Mode
1	1	System mode

Table 1. Modes of operation of BILBO

The application and operation of BILBO is shown in fig. 2. BILBO is a test-per-clock BIST architecture.

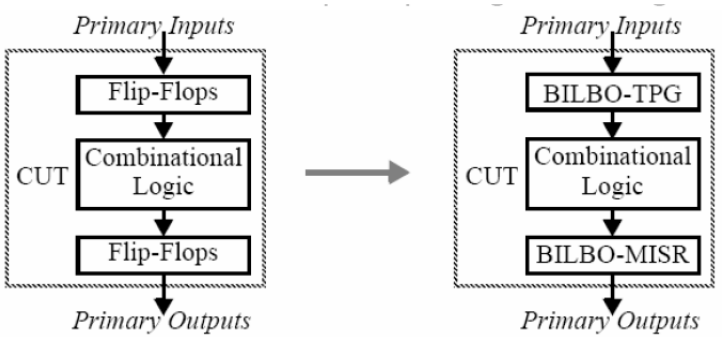
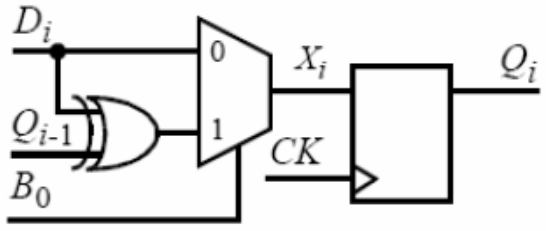


Fig. 2 Simple BILBO application to a CUT

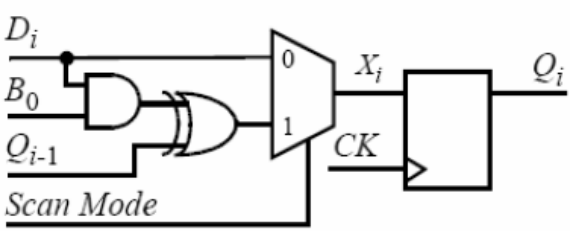
This approach has been modified into a test per clock Circular BIST approach by connecting all the flip-flops in the form of a circular chain and operating the flip-flops in the BIST mode. And the basic flip-flop architecture has been slightly modified from the initial one.

Three different circular BIST approaches have been proposed. They are Circular Self-Test path (CSTP), Simultaneous Self-Test (SST) and Circular BIST.



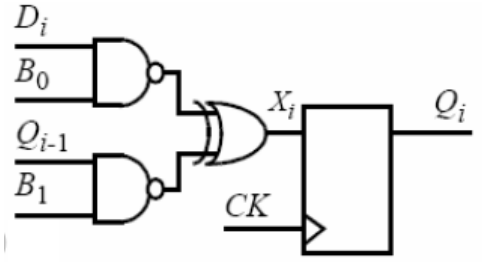
B0	X_i	Mode
0	D_i	System
1	$D_i \oplus Q_{i-1}$	BIST

(a) CSTP flip-flop and modes of operation



Scan Mode	B0	X_i	Mode
0	0	0	Initialization
0	1	D_i	System
1	0	Q_{i-1}	Shift(Scan)

(b) SST flip-flop and modes of operation



B1	B0	X_i	Mode
0	0	0	Initialization
0	1	D_i	System
1	0	Q_{i-1}	Shift(Scan)
1	1	$D_i \oplus Q_{i-1}$	BIST

(c) Circular BIST flip-flop and modes of operation
Fig 3. Comparison of circular BIST flip-flops

The basic idea of all these approaches is to partition the circuit into flip-flops and combinational logic and the flip-flops are augmented with additional logic to operate in BIST mode to test the circuit.

The circular BIST approach forms a large Multiple Input Signature Register (MISR) structure connecting all the flip-flops in the circuit. The output of the MISR for the current cycle will be applied as the input for the next cycle. As we are using an MISR the output responses are also being compacted simultaneously. The circular feed back path is equivalent to a characteristic polynomial $P(x) = x^n + 1$, where 'n' is the number of flip-flops.

AREA OVERHEAD DUE TO FLIP-FLOPS:-

The area over head for CSTP flip-flop is an ex-or gate and a multiplexer. It has an overhead of 7 gates, if we assume a 2-to-1 multiplexer is made up of 3 elementary logic gates and an ex-or with 4 gates. The main disadvantage is that it does no have scan mode. The area overhead for SST flip-flop is 9 gates and for Circular BIST flip-flop is 6 gates. The circular BIST approach has the lowest area overhead and it has 4 possible modes of operation including scan and initialization mode.

MY WORK:-

The Circular BIST approach has been used, for implementing the circular BIST for s5378, as it has the lowest area and highest flexibility (not required for this project). All the flip-flops, outputs and inputs of the circuit have been replaced by the circular BIST flip-flop shown in fig. 3c. .

PROCEDURE TO IMPLEMENT CIRCULAR BIST:-

1) The file in 'bench' format has to be converted in to ASL file. This is done using the tools provide by Dr. Stroud, the command is
   ~strouce/bin/isc2asl name.bench, name.asl file is created.

2) Circular BIST can be implemented by executing the provided program. This can be done using the commands

cc name.c , An executable a.out is created, then the command

a.out name.asl cbistname.asl (name.asl is the input ASL file and cbistname.asl is the output ASL file with the Circular BIST inserted).

3) After the Circular BIST has been implemented, fault coverage by implementing the Circular BIST has to be calculated. Fault coverage can be calculated by using fault simulation.

Procedure to perform Fault Simulation using ASL:-

a) The vector file (cbistname.vec) has to be created with the no. of inputs + 2. The two additional inputs are the control lines to control the operation of the circuit. The no. of vectors decide the no. of cycle for which the circuit has to be run in BIST mode.
b) The control file (cbistname.cnt) has to be created. This file contains the commands to generate fault list and perform the logic and fault simulation. (Once the fault simulation has been done, we can find the fault profile).

EFFICIENCY OR COVERAGE :-

As the circuit is a sequential circuit, the test generation is difficult when compared to the combinational circuit. So, the vectors produced by HITEC do not give good enough fault coverage because of the difficulty in controlling the state of the flip flops.

ADVANTAGES:-

The testing is performed by the BIST circuitry at the system clock frequency; this helps in the detection of delay faults also.

POSSIBLE IMPROVEMENTS:-

Once full circular BIST has been implemented, the program can be modified to implement partial circular BIST. By implementing partial circular BIST, we can remove the BIST flip-flops in the critical paths and reduce the delay overhead.

CONCLUSION:-

Circular BIST gives better fault coverage for this circuit than the fault coverage with vectors produced by HITEC. The fault coverage is not too high when the circuit is operated for 10,000 cycles in BIST mode. From the fault profile, we can notice that the first 250 vectors (500 cycles) detect around 2900 faults where as the next 9,750 vectors detected only 500 faults. Because we cannot apply deterministic vectors as inputs, we cannot achieve the required fault coverage within limited no. of clock cycles. Hard to detect faults take more amount of test time, this is one of the main problems associated with BIST. The fault coverage can be improved and the test time can be reduced if we use the scan mode of operation in between BIST cycles.

RESULTS:-

The fault coverage of HITEC can't be compared with that produced by ASL because they use different algorithms for collapsing the faults. The fault lists provided by the two do not match. The fault coverage statistics of HITEC are presented just for comparison. There are separate tests to test the scan chain, so the faults present in the scan chain are removed when the fault simulation is performed with circular BIST included.

Fault Coverage achieved using HITEC:-
Total No. of faults present: 4603
No. of faults detected: 3146
No. Undetected Faults: 1379
No. of Potentially Detected Faults: 78
No. of redundant faults: 166
No. of aborted faults: 1291
Coverage: 0.6385
No. of vectors generated by HITEC: 894

Fault Coverage achieved when Circular BIST was implemented and the circuit was executed for 10,000 Clock cycles (Excluding faults in BIST flip-flops):-
No. of collapsed faults: 3905
No. of faults detected: 3409
No. of undetected faults: 496
Fault coverage: 0.87

Fault Profile:-
Vecnum – Vector Number, Each vector is counted twice so that it is applied for both the low and high states of the clock
Numflts – No. of faults
Cumm – Cumulative number of faults

Fault detection distribution

vecnum	numflts	cumm
6	356	356
8	163	519
10	243	762
12	121	883
14	103	986
16	90	1076
18	96	1172
20	86	1258
22	94	1352
24	93	1445
26	84	1529
28	63	1592
30	64	1656
32	39	1695
34	38	1733
36	36	1769
38	34	1803
40	22	1825
42	27	1852
44	20	1872
46	45	1917
48	22	1939
50	13	1952
52	24	1976
54	17	1993
56	18	2011
58	23	2034
60	10	2044
62	9	2053
64	5	2058
66	8	2066
68	32	2098
70	7	2105

72	54	2159
74	23	2182
76	38	2220
78	13	2233
80	30	2263
82	9	2272
84	14	2286
86	3	2289
88	48	2337
90	5	2342
92	14	2356
94	9	2365
96	16	2381
98	12	2393
102	4	2397
104	5	2402
106	12	2414
108	5	2419
110	6	2425
112	5	2430
114	3	2433
116	22	2455
118	6	2461
120	2	2463
122	5	2468
124	2	2470
126	1	2471
128	2	2473
130	6	2479
134	5	2484
138	2	2486
140	3	2489
144	3	2492
146	9	2501
150	5	2506
152	1	2507
154	1	2508
156	2	2510
162	1	2511
164	1	2512
166	8	2520
170	2	2522
174	2	2524
180	52	2576
182	29	2605
182	29	2605
184	51	2656
188	2	2658
190	1	2659
192	3	2662
198	7	2669
200	1	2670
202	4	2674
206	2	2676
230	15	2691
234	2	2693
236	4	2697
242	25	2722
244	2	2724
248	1	2725
250	2	2727
256	1	2728
258	1	2729
262	1	2730
284	1	2731
310	2	2733
316	2	2735
318	2	2737
328	1	2738
334	12	2750
336	3	2753
338	3	2756
346	29	2785
360	9	2794
370	1	2795
382	1	2796
392	8	2804
396	1	2805
398	27	2832
400	18	2850
410	1	2851
426	1	2852
428	17	2869
430	43	2912
438	1	2913
444	9	2922
452	3	2925
456	1	2926
468	1	2927
478	1	2928
496	1	2929
500	2	2931
504	4	2935
506	2	2937
510	1	2938
522	3	2941
542	1	2942
562	1	2943
584	2	2945
586	1	2946
596	1	2947
614	4	2951
634	2	2953
652	3	2956
654	1	2957
662	1	2958
668	1	2959
670	5	2964
678	1	2965
696	3	2968
702	2	2970
704	6	2976
706	10	2986
708	7	2993
710	1	2994
712	3	2997
714	5	3002
720	1	3003
768	1	3004
800	1	3005
802	8	3013
822	8	3021
824	2	3023
826	3	3026
830	1	3027
832	3	3030
836	4	3034
852	2	3036
894	1	3037
912	4	3041
914	1	3042
920	2	3044
948	2	3046
950	1	3047
952	1	3048
992	2	3050
994	9	3059
996	3	3062

1008	1	3063
1016	2	3065
1028	3	3068
1030	1	3069
1034	2	3071
1048	1	3072
1058	1	3073
1060	1	3074
1084	1	3075
1096	5	3080
1102	2	3082
1116	1	3083
1120	3	3086
1122	2	3088
1134	1	3089
1136	2	3091
1164	2	3093
1168	1	3094
1174	1	3095
1180	1	3096
1186	10	3106
1188	14	3120
1196	2	3122
1198	1	3123
1204	2	3125
1234	1	3126
1280	4	3130
1282	4	3134
1286	2	3136
1306	2	3138
1314	1	3139
1316	1	3140
1378	1	3141
1380	5	3146
1424	2	3148
1426	5	3153
1470	1	3154
1508	1	3155
1540	2	3157
1552	2	3159
1556	10	3169
1592	2	3171
1622	7	3178
1624	3	3181
1716	3	3184
1744	1	3185
1756	1	3186
1764	1	3187
1856	2	3189
1900	1	3190
1998	3	3193
2072	1	3194
2078	1	3195
2082	3	3198
2086	1	3199
2090	4	3203
2108	1	3204
2134	1	3205
2144	2	3207
2154	4	3211
2186	1	3212
2218	2	3214
2258	1	3215
2260	2	3217
2318	2	3219
2334	2	3221
2374	1	3222
2376	1	3223
2384	1	3224
2458	3	3227
2530	2	3229
2560	1	3230
2564	1	3231
2624	1	3232
2644	2	3234
2686	1	3235
2770	1	3236
2772	1	3237
2814	1	3238
2822	5	3243
2888	1	3244
2932	1	3245
3028	2	3247
3040	7	3254
3042	1	3255
3044	3	3258
3046	1	3259
3210	2	3261
3306	1	3262
3314	1	3263
3336	1	3264
3338	2	3266
3368	1	3267
3402	2	3269
3532	5	3274
3556	4	3278
3562	1	3279
3594	2	3281
3810	4	3285
3974	2	3287
4072	2	3289
4140	2	3291
4168	10	3301
4426	1	3302
4430	1	3303
4450	1	3304
4476	2	3306
4520	1	3307
4658	5	3312
4662	4	3316
4922	1	3317
4958	4	3321
4960	1	3322
5038	1	3323
5120	1	3324
5196	2	3326
5292	1	3327
5490	1	3328
5492	2	3330
5582	2	3332
5688	1	3333
5700	3	3336
5930	1	3337
5962	2	3339
6200	3	3342
6252	1	3343
6378	1	3344
6454	1	3345
6536	3	3348
6908	1	3349
7042	1	3350
7232	1	3351
7282	1	3352
7304	1	3353
7342	1	3354
7356	1	3355
7726	2	3357
7820	1	3358

7858	1	3359
7892	1	3360
7894	2	3362
8018	1	3363
8576	2	3365
9216	1	3366
9568	1	3367
9618	1	3368
9760	1	3369
9958	2	3371
11588	1	3372
11670	1	3373
12110	1	3374
12316	1	3375
12488	1	3376
12634	1	3377
12770	2	3379
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13394	1	3385
13530	1	3386
13756	7	3393
13892	1	3394
13894	1	3395
14112	1	3396
14132	4	3400
14824	2	3402
16598	2	3404
16794	1	3405
18598	2	3407
19536	1	3408
19540	1	3409