

Making s5378 scan testable

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Abstract— The steps to make s5378 scan-testable are presented. Combinational vectors have been generated and converted to scan sequences in order to simulate faults in the sequential mode. Trivial implementation details are also mentioned. Atalanta, hope, hitec and proofs were the tools used for testing and fault simulation. The result of the fault simulation of the combinational and scan vectors are compared and analysed with respect to their coverage. The scan sequence was found to have less coverage than the combinational vectors due to hard to detect and redundant faults in the scan circuit itself.

I. INTRODUCTION

In order to test a sequential circuit, the time required to stabilize the test with the combinational and sequential parts together takes a long time. Initialization is a problem for most sequential circuits. Purely combinational circuits are found easier to handle. Hence, decoupling the testing of each eases the problem. This technique is known as scan design. It required extra hardware such as MUXes to be incorporated.

A sequential circuit can be visualized as a bunch of D flip flops whose inputs and outputs are connected to combinational logic. For a detail of the technique of scan design, please view [1]

The given circuit s5378 has 35 inputs, 49 outputs, 179 D-type FF's and 1775 inverters and 1004 other logic gates. This is an example of a rather large circuit in terms of combinational and sequential elements. As discussed later, the results show the practical difficulty of testing this circuit.

In this report, Section II presents the history of the idea of Scan Design as given in [1]. Section III illustrates the procedure I have taken. Section IV discusses the results and Section V concludes.

II. BACKGROUND

Scan design for hardware test was detailed in the 1973 paper by Williams and Angell [2]. Various implementations of the concept were used in companies like IBM, NEC, and others. Apart from the full-scan method used here, random access memory scan and partial scan are also different techniques for scan design. Current research focusses on reducing the area overhead and hardware required for scan design.

III. ANALYSIS AND ALGORITHMS

In order to scan design, the circuit's FF are represented as D-FF. The circuit requires to follow 4 rules, i.e.,

- Only D-type master-slave FFs should be used
- At least one primary input pin must be available for test.

- All FF clocks must be controllable from primary inputs
- Clocks must not feed data inputs of FFs

If the circuit does not follow some of the above rules, techniques for converting the circuit to follow them exist. In order to make the s5378 scan testable, I taken the following steps

- From the directories /opt/atalanta/iscas89/ I have taken the bench file of the s5378 containing only the combinational logic and all the inputs to it turned to pseudo-primary-inputs and outputs going to the flip flops as pseudo-primary-outputs. The pseudo-primary-outputs going to more than one FF have been considered as buffered outputs. This is in file s5378.scan
- Using atalanta generate the compact test vectors for this s5378.scan by first converting it to the format that atalanta takes the file in. It generates 244 test vectors for this part of the circuit with 40 redundant faults.
- The scan hardware is then added to the s5378.scan to place in the scan FF's using Transform.java and kept as s5378-Pri.bench
- The vectors are then parsed and the scan-sequence generated using ScanSequence.java to be kept as s5378-input-scan-sequence
- Using hope, the test vectors s5378-scan-sequence are simulated upon the s5378-Pri.bench.

The relevant files are attached in a zip archive.

IV. RESULTS

The s5378.bench was simulated using hitec and found to take 263.267 cpu seconds, to generate tests with a lot of backtracking and quite few aborted faults, 1288, as is evident from the log file, s5378.grs. As can be seen from the log file, LOG, the fault simulation for the combinational part using hope took 0.600 secs and had a coverage of 99.121% with 40 faults being redundant and the sequential part took 87.550 secs with a fault coverage of 93.344%. The undetected fault list was obtained by simulating the circuit using Proofs, and the 40 redundant faults from the combinational part were found to exist. Most of the other faults were in the scan design part of the circuit. I have not diagnosed why there are more undetected faults than these.

V. CONCLUSIONS AND ACKNOWLEDGEMENT

The scan design shows that indeed the time to generate the test for the circuit has reduced greatly. Although the scan chain sequence is long, we find that it takes much less time

than without the scan design. I have accomplished the full-scan design of the s5378.bench circuit. Amongst the lessons that I have learnt are that converting a given benchmark circuit to full-scan design is a rather easy process and I could see a marked improvement in the testability of such a circuit. As further work, I need to find out comprehensively the reason for different coverage. I would like to acknowledge Anand S. Mudlapur's for his help in understanding Scan Design.

REFERENCES

- [1] Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI circuits, M.L. Bushnell and V.D. Agrawal
- [2] Enhancing Testability of Large-Scale Integrated Circuits via Test Points and Additional Logic, M.J.Y Willaims, J.B. Angell, IEEE Trans on Computers , Jan 1973.