

Fault Diagnosis Using Fault Dictionaries and Probability

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Abstract—A method for fault diagnosis using fault dictionaries, diagnostic trees, and probability is presented. A diagnostic algorithm is described which implements various test vectors on a failing chip while dynamically assigning a probabilistic value, called a “Likelihood”, to each fault. Single stuck-at faults are assumed. The algorithm’s results are examined on a 74181 4-bit ALU circuit. In most cases, the algorithm yields a list of probable occurring faults, with a likelihood associated with each fault. In some cases, only one fault is present in the list and a 100% confidence can therefore be awarded to that fault. The real power of the algorithm is shown when faults do not all begin with equal likelihoods. Fault Likelihoods can be given more “weight” due to such things as maintenance logs and the type of error that caused the chip to fail. When faults begin with this weighted likelihood, the results are much more conclusive.

Introduction

VLSI Testing asks the question, “Did a fault occur?” In diagnosis, however, the question is, “Which fault occurred?” Answering this question can be a considerably complex and even impossible task when 100% confidence is desired. In many diagnosis procedures, 100% confidence cannot be achieved due to chip complexity, algorithm performance, and inherent uncertainties associated with the test itself. The results produced by these diagnosis procedures are inconclusive unless there is a way to quantify the probability, or “Likelihood”, of each possible fault’s occurrence.

In this paper, a diagnostic algorithm is presented that identifies single stuck-at faults with some associated level of quantified probability. We begin with an introduction to the ideas of fault dictionaries and diagnostic trees, the key ideas behind the most fault diagnosis algorithms. With this information in hand, the proposed Diagnostic Algorithm is presented. The Likelihood Function, which introduces probability into the algorithm, is defined and explained. This function behaves very differently when the beginning probabilities of the occurrence of faults are not assumed to be equal. This concept is explained and explored. The paper concludes with several example results of the Diagnostic Algorithm, using the 74181 4-bit ALU as a test circuit.

Fault Dictionaries

Applying a test to a chip simply identifies a faulty chip; this is used in testing. For diagnosis, there must be something that “maps out” which tests activate and propagate which faults. From here, the possibility, or probability, of a particular fault’s occurrence in a failing chip can be eliminated if a test that theoretically activates and propagates that fault yields good results (i.e. non-faulty outputs). Likewise, a fault will be more suspicious if a test that theoretically activates and propagates that fault yields bad results (i.e. faulty outputs).

The fault dictionary is the simplest form for mapping out which tests activate and propagate which faults. Fault dictionaries are made in the design stage for a theoretical non-faulty chip. They are then used in the diagnosis stage to compare with experimental results on a failing chip.

A typical fault dictionary is shown below in Figure 1. Each fault for a chip (or system) is listed down the left side of the table and the test vectors that activate and propagate the faults are listed along the top. Usually the fault list is collapsed by rules of equivalence. If not, an unnecessary amount of faults will share the same test syndrome (described below). The test vectors typically consist of a complete test set for the chip if one is known. The matrix of ones and zeros in the fault dictionary relate the faults to the tests that detect each fault. For matrix element $[i,j]$, a “1” means the particular test set, Test j , detected the fault, Fault i . A “0” means Test j did not detect Fault i . A row, i , of ones and zeros is known as the test syndrome for the corresponding Fault i . For example, the test syndrome for Fault 5 is $\{0\ 0\ 0\ 1\ 0\ 0\}$. Two or more faults can have the same test syndrome. For example, the test syndromes for Fault 2 and Fault 3 are both $\{1\ 0\ 0\ 0\ 0\ 0\}$.

	Test1	Test2	Test3	Test4	Test5	Test6
⋮						
Fault1	0	1	0	0	0	0
Fault2	1	0	0	0	0	0
Fault3	1	0	0	0	0	0
Fault4	0	1	0	1	0	0
Fault5	0	0	0	1	0	0
Fault6	0	0	1	0	0	0
Fault7	0	0	0	0	0	1
⋮						

Figure 1: Example of a Fault Dictionary

The fault dictionary for the 74181 4-bit ALU is shown in Appendix A. For this dictionary, a red cell in position $[i,j]$ indicates that Fault i was detected by Test j , similar to a “1” in the fault dictionary above. This 74181 fault dictionary will be explained in more detail.

Diagnostic Trees

Another way to look at the fault dictionary is through the diagnostic tree. An example of a diagnostic tree is shown in Figure 2 below. This tree is just another representation of the fault dictionary in Figure 1. The results of each test (“1” for detection of a fault, “0” for no detection) reveal which branch we will follow in our diagnostic tree. When we reach the end of a branch, the correct fault will be identified. In some cases, two or more faults cannot be distinguished by the given test set. This happens when two faults share the same test syndrome. An example is Faults 2 and 3 below. Fault dictionaries and diagnostic trees cannot distinguish between these two

faults¹. The Diagnostic Algorithm presented in this paper provides a probabilistic way to deal with this problem.

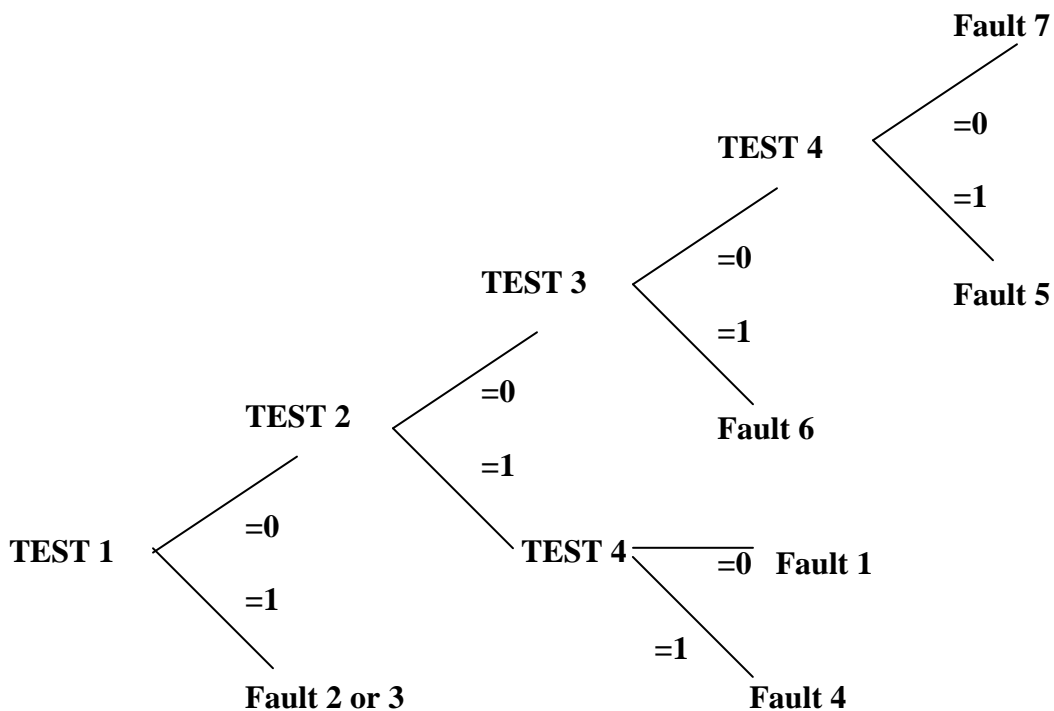


Figure 2: Example of a Diagnostic Tree

The first test applied in a diagnosis method is at the “trunk” of the diagnostic tree. From here, the diagnosis method will typically trace to the end of a tree depending on the outcome of each test. The decision of the order of tests greatly affects the length of the diagnostic tree. For example, consider again Figure 2 above. In this case, Test 1 is applied first and is found at the “trunk” of the tree. The order of tests increases until Test 4 is applied last. At its longest “branch”, this diagnostic tree is five levels deep: {TEST 1, TEST 2, TEST 3, TEST 4, Fault 7}. Consider if the order had been reversed, starting with Test 7 and going to Test 1. In this case, the longest branch would have been 8 branches deep!

Diagnostic Algorithm

Using the ideas of fault dictionaries and diagnostic trees, diagnosis algorithms can be run on failing chips that will match experimental test vector results with information from these dictionaries and trees to find the fault that is occurring. As stated previously,

¹ In some cases, more test vectors may be used to distinguish between the two faults. However, this is not always possible and tends to be computationally expensive.

it is often impossible or too computationally expensive to exhaustively test a complex chip using complete test sets to yield a single fault with 100% confidence. If diagnosis results that include multiple possible faults are to be useful, some method of quantifying each fault's probability must be established.

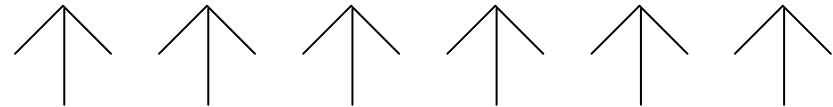
The Likelihood Function

The probability associated with the occurrence of a fault, i , in a failing chip will be referred to as the *likelihood of Fault i* . A "0" likelihood indicates that the fault did not occur, and a "1" indicates that the fault definitely occurred. After each test, faults that pass will be dropped² from the list of possible occurring faults (i.e. they will be assigned a likelihood of zero). The total likelihood of the dropped faults will be divided equally between the faults that remain in the list of possible occurring faults. Stated formally,


$$L_i(t) = L_i(t-1) + \frac{L_0(t-1) + \dots + L_m(t-1)}{N(t)} \quad (1)$$

where $L_i(t)$ is the likelihood associated with fault i at time t . Faults $0, \dots, m$ are the faults that failed the test at time $t-1$. $N(t)$ is the total number of remaining faults in the list at time t . Time is represented by the application of tests, so if time t represents the test that is about to be applied, time $t-1$ represents the test that was most recently applied.


	Test1	Test2	Test3	Test4	Test5	Test6
Fault1	0	1	0	0	0	0
Fault2	1	0	0	0	0	0
Fault3	1	0	0	0	0	0
Fault4	0	1	0	1	0	0
Fault5	0	0	0	1	0	0
Fault6	0	0	1	0	0	0
Fault7	0	0	0	0	0	1




Two faults dropped if zero




Two faults dropped if zero



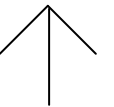
One fault dropped if zero



One fault dropped if zero



Only one fault remains



Likelihood of each remaining fault:	0.14	0.2	0.33	0.5	1	1
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Figure 3: Dynamic Likelihood during Diagnostic Test

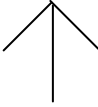
² Only if there is 100% confidence in the results of the test, which may not be the case.

This is best illustrated by an example. Consider the fault dictionary of Figure 3 above. This faulty chip is being diagnosed and blue represents that the fault is still under consideration (i.e. still in the list of possible faults). Recall that Tests represent time. For this example, the results of Tests 1-5 are “0”, and the result of Test 6 is “1”. A “0” result of a test indicates that no faults were found by that test, and a “1” result indicates that faults were found. Before Test 1 is applied at time t , the likelihood³ of each fault is $1/N(t)=1/7=0.14$. When the results of Test 1 do not reveal the presence of a fault (i.e. result =0), Faults 2 and 3 are dropped since they are theoretically supposed to be found by Test 1. The likelihood of both of these faults is divided up evenly among the remaining five faults yielding new likelihoods of $0.14 + (0.14+0.14)/5=0.2$ for each fault. Tests 2-4 are applied in the same manner and likelihoods are adjusted accordingly until only one fault remains. After Test 4, Fault 7 is the only fault remaining and its likelihood is therefore 1.⁴

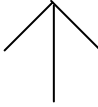
Beginning Probabilities

In the example in Figure 3, the likelihood function of equation 1 appears to have only calculated the mean probability of each remaining fault (i.e. $1/7=0.14$, $1/5=0.2$, $1/3=0.33$). The reason for this is the assumption we began with, that all faults begin with equal likelihood. Indeed, if there is no knowledge of the chip-under-test beforehand, this is the only possibility. However, most chips undergoing diagnosis have large amounts of beforehand knowledge associated with them. An example of this is a maintenance log, which records the history of failures and repairs associated with the chip or system.

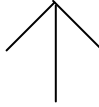
	Beginning Likelihoods	Likelihoods after Test 1	Likelihoods after Test 2	Ending Likelihoods
Fault1	0.22	0.27	0.56	0.56
Fault2	0.11	0	0	0
Fault3	0.11	0	0	0
Fault4	0.11	0.16	0.45	0.45
Fault5	0.11	0.16	0	0
Fault6	0.22	0.27	0	0
Fault7	0.11	0.16	0	0



Two faults
dropped if
Test 1="0"



Three faults
dropped if
Test 2="1"



Fault 4
dropped--
less
likelihood

Figure 4: Dynamic Likelihood during Diagnostic Test with Unequal Beginning Likelihoods

³ This is calculated assuming that all faults start off with equal likelihood. This will not always be the case.

⁴ A likelihood of “1” means that fault is occurring with 100% confidence. This is only possible if you have 100% confidence in the results of the tests.

Consider again the example in Figure 3; but this time a maintenance log reveals that Faults 1 and 6 have occurred twice as many times as any other fault on the chip. With this new information, a “beginning likelihood” column is added and shown in Figure 4 with a new distribution that allows Faults 1 and 6 to be twice as likely as the other five faults. After Tests 1 and 2 are run, Fault 1 is selected as the most likely fault. On a system level, this faulty part can be replaced; and if that does not fix the problem, the part associated with Fault 4 (the second most likely fault) will be replaced.

Many other things may affect the beginning and/or dynamic likelihoods of each fault. Risky manufacturing processes such as thin gate oxides of some transistors may point to certain parts of a chip for high fault likelihood. Some tests may not be as reliable as others, producing a different distribution of dynamic likelihood (this would require some re-working of equation 1). All of these things would produce a different beginning likelihood (or dynamic distribution) that would allow a diagnosis method to produce more conclusive results.

The Algorithm

Building on the ideas of fault dictionaries, diagnostic trees, and the likelihood function, a Diagnostic Algorithm is written and shown in Figure 5 below.⁵ The algorithm takes in a table of beginning likelihoods (received from a maintenance log, etc.) and dynamically redistributes the likelihoods with the application of each new test vector. The algorithm assumes that only single stuck-at faults are present. The algorithm also assumes 100% confidence in each test vector, so that the likelihood is zeroed and the fault dropped if a test shows that the fault is not possible. As mentioned before, this may not be the case and the algorithm can be changed to include different likelihood distribution functions for each test vector.⁶

<i>START</i>	<i>Assign beginning likelihoods to each fault</i>
<i>LOOP</i>	<i>Apply next test vector to faulty circuit</i> <i>If outputs are faulty (i.e. Test yields “1”)</i> <i> Assign zero likelihood to faults that show “0” for current test vector</i> <i>Else</i> <i> Assign zero likelihood to faults that show “1” for current test vector</i> <i>Redistribute likelihoods using equation 1</i> <i>Repeat LOOP</i>
<i>END</i>	<i>Output final fault likelihoods</i>

Figure 5: Pseudo code for Diagnostic Algorithm

The output of the algorithm will yield a set of possible faults (in some cases only one fault), with different likelihoods. However, a major advantage of this algorithm is that it need not be completed to yield useful results. If the algorithm is stopped at any point, there will still be a list of possible faults with different likelihoods. This list just gets smaller and smaller as more tests are tried. This is useful when complex circuits are

⁵ Given a lack of experience with code writing, only the pseudo code is given for the algorithm. The algorithm was, however, tested manually and the results are given in the following section.

⁶ These cases are not explored in this paper.

being diagnosed which may take hours to apply every test vector. It may be advantageous in this case to sacrifice diagnostic resolution for diagnosis time.

Results

This algorithm was implemented on the 74181 4-bit ALU. The complete fault dictionary of this circuit is given in Appendix A. It was found using the Proofs simulator of the University of Illinois. A collapsed fault list was used and the equivalent faults are not shown. The smallest known complete test set of 12 vectors was used. In this dictionary and in the following figures, a red cell indicates that the test of that column detected the fault of that row.

The Diagnostic Algorithm was applied on this circuit for several randomly selected faults. In the following pages, results are given for each trial. Examples 1 and 2 show snapshots of the Diagnostic Algorithm in process. The “More Examples” section shows only the end result of the algorithm. As stated before, the algorithm assumes only single-stuck at faults are present. We also assume that all faults begin with equal likelihood. In the last example, we disregard this second assumption. In each example, the fault that is actually occurring is highlighted in blue.

Example 1: Fault 36-2-1

The fault that is occurring is fault 36-2-1, using the Hitec/Proofs software’s format. This corresponds to a stuck-at-1 fault on the second input of gate #36. Figure 6 shows a snapshot of the algorithm after the second loop. Notice that the only faults that remain in the list (i.e. the only faults with non-zero likelihood) are the faults that have a test syndrome of {0,1} for the first two test vectors. There are 39 total faults in this list, so each fault has a likelihood of 0.0256 (there were 237 faults to begin with, so the list has already been reduced by over 80%). Figure 7 shows a snapshot after the fourth loop. Here, only the faults remain in the list that have a test syndrome of {0,1,0,0} for the first four test vectors. Each of the 20 remaining faults is assigned a probability of 0.05. Figure 8 and Figure 9 show snapshots after the sixth and eighth loops respectively. With each loop, the list of likely faults is shortened. After the eighth loop, only two faults remain. These two faults each have a probability of 0.5 and are indistinguishable since they share the same test syndrome. The use of more test vectors or beforehand knowledge in the form of differing beginning likelihoods may allow us to make an educated guess about which fault is occurring.

Example 2: Fault 28-2-1

The fault that is occurring in this example is the stuck-at-1 fault of the second input of gate #28. Results are shown in Figure 10 and Figure 11. After 6 loops of the Diagnostic Algorithm, the likelihood list is only decreased to 56 possible faults, each with a probability of 0.0179. This is not as good as in Example 1, which only had 19 possible faults after the sixth loop. After all tests are applied the algorithm was able to get down to four possible faults, again not as good as Example 1.

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
1	0	1										
13	0	1										
15	0	1										
16	0	1										
17	0	1										
18	0	1										
20	1	1										
22	1	1										
24	1	1										
26	1	1										
28	1	1										
30	1	1										
32	1	1										
34	1	1										
36	2	1										
56	5	1										
59	5	1										
60	4	1										
61	3	1										
62	2	1										
64	4	1										
65	3	1										
66	2	1										
68	3	1										
69	2	1										
76	2	0										
82	0	1										
83	0	1										
84	0	1										
85	1	0										
86	1	0										
87	1	0										
88	0	1										
89	0	1										
90	0	1										
91	0	1										
92	0	1										
93	0	1										
95	0	1										

Figure 6: Example One, after Tests 1 & 2

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
1	0	1										
13	0	1										
15	0	1										
16	0	1										
17	0	1										
18	0	1										
20	1	1										
22	1	1										
24	1	1										
26	1	1										
28	1	1										
30	1	1										
32	1	1										
34	1	1										
36	2	1										
56	5	1										
59	5	1										
64	4	1										
68	3	1										
76	2	0										

Figure 7: Example One, after Tests 3 & 4

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
1	0	1										
13	0	1										
15	0	1										
16	0	1										
17	0	1										
18	0	1										
20	1	1										
22	1	1										
24	1	1										
26	1	1										
28	1	1										
30	1	1										
32	1	1										
34	1	1										
36	2	1										
56	5	1										
59	5	1										
64	4	1										
68	3	1										

Figure 8: Example One, after Tests 5 & 6

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
13	0	1										
36	2	1										

Figure 9: Example One, after Tests 7 & 8

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
1 0								1 0	0	1 0		1 0
2 0							2 0	1	2 0	3		
3 0							3 0	0	3 0	0		3 0
4 0							4 0	1	4 0	1		4 0
6 0											6 0	6 0
8 0											8 0	
20 2							20 2	1				
20 3												20 3
21 1											21 1	
22 2							22 2					
22 3								22 3				
23 1											23 1	
24 2								24 2				
24 3							24 3					
25 1												
26 2									26 2			
26 3							26 3	1				
27 1							27 1	1				
28 2										28 2		
28 3							28 3					
29 1												29 1
29 2										29 2		
30 3							30 3					
31 1								31 1				
32 3								32 3				
33 1							33 1					
34 3									34 3			
35 1							35 1	1		35 1		
37 1										37 1		
38 1							38 1	0		38 1		
39 1										39 1		
40 1							40 1	1	0			40 1
41 1										41 1		0
42 1							42 1	0				42 1
43 1							43 1	0		43 1		0
44 1											44 1	0
46 0							46 0	0		46 0	0	46 0
58 2										58 2	0	58 2
72 0							72 0	1	72 0	1	72 0	1
72 1							72 1	0			72 1	0
72 2								72 2	0			72 2
72 3									72 3			
73 4												73 4
73 1							73 1	0				
73 2								73 2	0			
73 3									73 3	0		
74 1							74 1	0				
74 2								74 2	0			
75 1							75 1	0				
77 0							77 0	1	77 0	1	77 0	1
78 2							78 2	1	78 2	1	78 2	1
94 1							94 1	1			94 1	1
94 2									94 2			94 2
94 3										94 3		
94 4							94 4				94 4	

Figure 10: Example Two, after Tests 1-6

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
21 2											21 2	1
28 2											28 2	1
29 2											29 2	1
94 2											94 2	1

Figure 11: Example Two, after Tests 1-12

More Examples

Figure 12 through Figure 15 show more examples of single stuck-at faults. In these examples, only the end result of the Diagnostic Algorithm is shown. In Example 3, fault 61-3-1 is found with 100% confidence. This means that there are no other faults that are equivalent to this fault or have the same test syndrome: {0,1,1,1,0,0,0,0,0,0,0,0}.

In Example 4, fault 85-1-1 is found as the only fault with the test syndrome {1,0,0,0,0,0,1,1,1,0,1,0}. However, there are 3 more equivalent faults that are not shown in the fault dictionary, yielding a total of 4 possible faults. Each of these faults has a likelihood of 0.25 and cannot be distinguished without beginning likelihoods. One good thing about equivalent faults is that they typically point to one gate that can easily be replaced (if diagnosis is on the system level).

Example 5 yields the worst results yet. It correctly identifies fault 22-1-1, but keeps eleven other faults as possibilities. It is interesting to notice that the examples with the worst results typically have only one identifying test in the fault’s test syndrome (i.e. test syndrome {0,0,0,0,0,0,0,0,0,0,1,0} of example 2 and test syndrome {0,1,0,0,0,0,0,0,0,0,0,0} of Example 5).

In Example 6, fault 41-2-0 is correctly identified along with one incorrectly identified fault. This case is even worse since the incorrectly identified fault, fault 41-2-0, has 4 equivalent faults attached with it, making a total of 6 possible faults.

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
61 3	1	61 3	1	61 3	1	61 3	1					

Figure 12: Example Three, fault 61-3-1 found with 100% confidence

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
85 1	1	85 1	1					85 1	1	85 1	1	85 1

Figure 13: Example Four, fault 85-1-1 found with possible equivalent faults

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
1 0	1	1 0										
20 1	1	20 1										
22 1	1	22 1										
24 1	1	24 1										
26 1	1	26 1										
28 1	1	28 1										
30 1	1	30 1										
32 1	1	32 1										
34 1	1	34 1										
56 5	1	56 5										
59 5	1	59 5										
64 4	1	64 4										

Figure 14: Example Five, fault 22-1-1 found with several wrong faults

FAULTS (EQUIV)	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12
10 0	0			10 0	0						10 0	0
41 2	0			41 2	0						41 2	0

Figure 15: Example Six, fault 41-2-0 found with 6 parasitic equivalent faults

Example with Beginning Likelihoods

Reconsider Example 5, which yielded the worst results. In this example, fault 22-1-1 is correctly identified along with eleven other incorrectly identified faults. Imagine that the faults had a maintenance log, which gave a greater beginning likelihood to a section of the circuit involving gates 20-30. Also, imagine that the type of error that caused the failure gives more likelihood to the first section of 25 gates. So, faults associated with gates 1-30 begin with twice the likelihood, and faults associated with gates 20-25 begin with four times the likelihood of other faults.

Figure 16 shows the beginning and ending likelihood distributions. Now, the final probable occurring fault list is down to only three faults, instead of twelve. The rest of the twelve are still in the possible fault list, but with less likelihood.

Faults (EQUIV)	Beginning Likelihoods	Ending Likelihoods
1 0 1	0.006	0.073
20 1 1	0.012	0.136
22 1 1	0.012	0.136
24 1 1	0.012	0.136
26 1 1	0.006	0.073
28 1 1	0.006	0.073
30 1 1	0.006	0.073
32 1 1	0.003	0.06
34 1 1	0.003	0.06
56 5 1	0.003	0.06
59 5 1	0.003	0.06
64 4 1	0.003	0.06
ALL OTHER FAULTS	{0.003, 0.006, 0.012}	0

Figure 16: Example Five redone, this time with beginning likelihoods

Conclusion

The Diagnostic Algorithm has given accurate results for the 74181 4-bit ALU, even when equal beginning likelihoods are assumed. The results are much more conclusive when the beginning Likelihood of each fault is weighted by beforehand knowledge such as maintenance logs. During each loop of the algorithm, Likelihoods are dynamically allocated to each possible fault, yielding one of the algorithm's most useful characteristics: it can be halted at any point and useful information can still be obtained.

One possible improvement of the Likelihood function, as previously mentioned, is to allow different Likelihood distributions for each test vector, depending on the confidence in the results of a particular test vector. Another area of future study is the relationship between the number of 1's in an occurring fault's test syndrome and the number of faults that remain possible after the algorithm is run. Examples two and five both had only one "1" in the test syndrome, and these examples yielded the worst results (the largest number of wrongly guessed faults). Examples three and four had three and five 1's in the test syndromes, respectively, and yielded the best results. This relationship was found to be consistent in several other examples that are not shown.

Appendix A⁷

		Circuit 74181 4-Bit ALU Complete Fault Dictionary												
FAULTS (EQUIV)		TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8	TEST 9	TEST 10	TEST 11	TEST 12	
1	0									1 0 0		1 0 0		1 0 0
1	0	1 0												
2	0		2 0 0	2 0 0	2 0 0	2 0 0							2 0 0	
2	0									2 0 1	2 0 1	2 0		2 0 0
3	0				3 0 1	3 0 1	3 0 1		3 0 0	3 0 0	3 0 0			3 0 0
3	0												3 0 1	
4	0	4 0 0		4 0 0	4 0 0									4 0 1
4	0													4 0 0
5	0	5 0 0	5 0 0	5 0 0	5 0 0		5 0 0		4 0 1	4 0 1	4 0 1		5 0 0	5 0 0
5	0					5 0 1		5 0 1	5 0 1	5 0 1		5 0 1		5 0 1
6	0					6 0 0						6 0 0		
6	0												6 0 1	6 0 1
7	0	7 0 0	7 0 0	7 0 0	7 0 0							7 0 0	7 0 0	7 0 1
7	0					7 0 1	7 0 1	7 0 1	7 0 1					7 0 1
8	0						8 0 0							
8	0									8 0 1				8 0 1
9	0	9 0 0	9 0 0	9 0 0								9 0 0		9 0 0
9	0				9 0 1	9 0 1	9 0 1	9 0 1					9 0 1	
10	0				10 0 0								10 0 0	
10	0							10 0 1		10 0 1				
11	0	11 0 0	11 0 0								11 0 0			11 0 0
11	0			11 0 1	11 0 1	11 0 1	11 0 1					11 0 1	11 0 1	11 0 1
12	0		12 0 0									12 0 0		12 0 0
12	0				12 0 1			12 0 1						
13	0	13 0 0		13 0 0	13 0 0									
13	0		13 0 1					13 0 1	13 0 1	13 0 1				13 0 1
15	0					15 0 0			15 0 0					
15	0	15 0												15 0 1
16	0						16 0 0							16 0 0
16	0	16 0 1								16 0 1				
17	0				17 0 0									17 0 0
17	0	17 0							17 0 1					
18	0			18 0 0									18 0 0	
18	0		18 0 1					18 0 1						18 0 1
19	0	19 0 0		19 0 0	19 0 0			19 0 0	19 0 0	19 0 0	19 0 0			19 0 0
19	0					19 0 1								19 0 1
20	1		20 1											
20	1								20 2 1					
20	3													20 3 1
21	1													21 1 1
21	1												21 2 1	
22	1		22 1											
22	1								22 2 1					
22	3									22 3 1				
23	1									23 1 1				
23	2					23 2 1							23 2 1	
24	1		24 1											
24	1										24 2 1			
24	3								24 3 1					
25	1								25 1 1					
25	2					25 2 1	25 2 1							
26	1		26 1											
26	2										26 2			
26	3								26 3 1					
27	1								27 1 1					
27	2				27 2 1	27 2 1	27 2 1							
28	1		28 1											
28	2												28 2	
28	3									28 3 1				
29	1													29 1 1
29	2												29 2 1	
30	1		30 1											
30	2												30 2	
30	3									30 3 1				
31	1										31 1 1			
31	2						31 2 1						31 2 1	
32	1		32 1											
32	2						32 2 1	32 2 1						
32	3										32 3 1			
33	1									33 1 1				
33	2						33 2 1	33 2 1						
34	1		34 1											
34	2				34 2 1	34 2 1	34 2 1							
34	3											34 3		
35	1								35 1 1					
35	2					35 2 1	35 2 1	35 2 1						
36	1						36 1 1							
36	2									36 2 1	36 2 1	36 2 1		36 1 1
37	1		36 2										37 1 0	
37	2													
37	3						37 2 0							
38	1								38 1 0				38 1 0	
38	2		38 2 0											
38	3						38 2 0						38 3 0	
39	1												39 1 0	
39	2													
39	3													
40	1													40 1 0
40	2		40 2 0											
40	3												40 3 0	
41	1												41 1 0	
41	2													41 2 0
42	1													
42	2		42 2 0											
42	3												42 3 0	42 3 0
43	1												43 1 0	
43	2													43 2 0
44	1									44 1 0				
44	2		44 2 0											
44	3												44 3 0	44 3 0
45	0		45 0 0	45 0 0	45 0 0	45 0 0	45 0 0	45 0 0	45 0 0	45 0 0	45 0 0		45 0 0	45 0 0
45	0												45 0 1	
46	0													46 0 0
46	0		46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1	46 0 1
47	0		47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0	47 0 0
47	0												47 0 1	
48	0													48 0 0
48	0		48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1	48 0 1
49	0		49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0	49 0 0
49	0												49 0 1	49 0 1
50	0													50 0 0
50	0		50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1	50 0 1
51	0		51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0	51 0 0
51	0												51 0 1	51 0 1

⁷ The Fault Dictionary uses a collapsed equivalent fault list and a complete 12-vector test set. The equivalent faults are not shown. Faults are labeled using the Hitec/Proofs software's format. A red cell indicates that the fault was found using the test vector of the cell's corresponding column.

