

PowerPC(short for **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC **P**rocessor **C**hip, often abbreviated as **PPC**) is a RISC architecture created by the 1991 Apple–IBM–Motorola alliance, known as *AIM*. PowerPC is largely based on IBM's POWER architecture, the architectures have remained close enough that the same programs and operating systems will run on both if some care is taken in preparation. Most personal-computers today contain an Intel produced 80X86/Pentium processor - about 85% of personal computers use Intel chips. In an effort to break Intel's hold on the market, IBM has formed an alliance with Apple and Motorola to produce the PowerPC.

Design Features of PowerPC:

The PowerPC is designed along RISC principles, and allows for a superscalar implementation. Versions of the design exist in both 32-bit and 64-bit implementations. Starting with the basic POWER specification, the PowerPC added:

1. Support for operation in both big-endian and little-endian modes; the PowerPC can switch from one mode to the other at run-time.
2. Single-precision forms of some floating point instructions, in addition to double-precision forms
3. Additional floating point instructions at the behest of Apple, a fused multiply add.
4. A complete 64-bit specification that is backward compatible with the 32-bit mode
5. A paged memory management architecture which is used extensively in server and PC systems.

The MPC601 (RISC) is the first of a series of PowerPC chips announced by the alliance. It contains fixed length 32-bit wide instructions and three parallel execution units. The three execution units are the Branch Processing Unit (BPU), Integer Unit (IU) and Floating-point Unit (FPU). Instructions are dispatched to the different execution units via an Instruction Unit, which can queue up to eight instructions and has a dedicated adder for prefetching. Instructions and data are fetched from a 32kB unified eight-way, set-associative cache. This cache uses a least-recently used (LRU) replacement algorithm. The Memory Management Unit supports demand paging for 4kB pages and supports block addressing for block sizes ranging from 123kB to 8MB.

Present Status:

- **PowerPC G5** - 64-bit Power Architecture processors
- **Cell** is a microprocessor architecture jointly developed by Sony Computer Entertainment, Toshiba, and IBM – PS3 game console
- **Xenon** - based on IBM's PowerPC ISA – XBOX 360 game console.
- **Broadway** – based on IBM's PowerPC ISA – Nintendo Wii gaming console.

Future Technologies:

- **POWER7, PowerPC e700** or **NG-64** (Next Generation 64-bit) a line of future high performance 64-bit embedded RISC-processor cores built using Power Architecture technology designed by Freescale.

32-bit and 64-bit PowerPC processors have been a favorite of embedded computer designers. To keep costs low on high-volume competitive products, the CPU core is usually bundled into a system-on-chip (SOC) integrated circuit. The PowerPC architecture combines advanced reduced instruction computing and pipelining techniques into a small, low-power CMOS chip. It has advanced pipelining, independent execution units which allow up to three instructions to be executed in parallel, while at the same time having simple static branching techniques and a relatively simple unified data and instruction cache. These simplified design techniques have left room for a relatively large cache (32k) to provide a high cache hit ratio.

References:

- Michael K. Becker, Michael S. Allen, Charles R. Moore, John S. Muhich, David P. Tuttle, "The Power PC 601 Microprocessor," IEEE Micro, vol. 13, no. 5, pp. 54-68, Sep/Oct, 1993
- <http://en.wikipedia.org/wiki/PowerPC>