VLSI and ASIC Design (CE-VLS)

CE-VLS0. History and overview of VLSI and ASIC design [core]
CE-VLS1. MOS Transistor Fundamentals
CE-VLS2. Processing and Layout
CE-VLS3. Function of the Basic Inverter Structure
CE-VLS4. Circuit Characterization and Performance
CE-VLS5. Combinational Logic Circuits
CE-VLS6. Sequential Logic Circuits
CE-VLS7. Alternative Circuit Structures/Low Power Design
CE-VLS8. Semiconductor Memories and Array Structures
CE-VLS9. Chip Input/Output Circuits
CE-VLS10. Semi custom Design Technologies
CE-VLS11. ASIC Design Methodology

MOS transistor fundamentals, CMOS logic circuits; VLSI fabrication and design rules; clocking strategies and sequential design; performance estimation; memories and programmable arrays; standard cell design methodologies; computer aided design (CAD) tools, top-down design of application-specific integrated circuits (ASICs).

CE-VLS0. History and overview of VLSI and ASIC design [core]

Suggested time: 1 hour

Topics:

- Indicate some reasons for studying VLSI and ASIC design.
- Highlight some people that influenced or contributed to the area of VLSI and ASIC design.
- Indicate some important topic areas such as MOS transistors, inverter structure, circuit performance, combinational and sequential circuits, memory and array structures, chip I/O design, and application-specific integrated circuits.
- Describe a transistor and relate it to a semiconductor.
- Indicate the characteristics of a MOS transistor.
- Describe CMOS transistors and contrast them with MOS technologies.
- Describe some sequential logic circuits such as latches and clock distribution.
- Describe the structure of memory design.
- Contrast memory structures with array structures.
- Contrast the advantages of SRAM and DRAM memory devices.
- Describe at which point a circuit becomes a chip.
- Provide some examples of application-specific integrated circuits.
- Explore some additional resources associated with VLSI and ASIC design.
- Explain the purpose and role of VLSI and ASIC design in computer engineering.

Learning objectives:

- Identify some contributors to VLSI and ASIC design and relate their achievements to the knowledge area.
- Define a semiconductor.
- Explain the difference between MOS and CMOS transistors.
- Define a sequential circuit.
- Identify some memory devices related to VLSI circuits.
- Define the meaning of a chip.
- Give an example of an ASIC chip design.
- Describe how computer engineering uses or benefits from VLSI and ASIC design.

CE-VLS1. MOS Transistor Fundamentals
Suggested time: 6 hours
Topics:

Semiconductor materials and characteristics
Semiconductor doping and its effects
Diode construction, function, and modeling
MOS transistor characteristics and equations
Sub-micro MOS transistor characteristics
MOS transistor parasitic
Device modeling and simulation
Bipolar devices (optional)

Learning Objectives:

1. Understand the current carrying mechanism and I/V characteristics of intrinsic and doped semiconductor materials.
2. Understand the behavior and I/V characteristics of a reverse-biased and forward-biased PN junction.
3. Understand the function of a PMOS and NMOS field effect transistor (FET) and how to model that function using the device equations.
4. Understand the effect of sub-micron device sizes on the function of MOSFETS.
5. Understand the origin and effect of parasitic resistances and capacitances within the transistor itself.
6. Understand the basics of how MOSFET simulation is performed by SPICE (and optionally BSIM) and what parasitic are included in the device model itself.
7. (Optionally) Understand the function of a Bipolar Junction Transistor (BJT) and how to model that function using the device equations.

CE-VLS2. Processing and Layout
Suggested time: 2 hours
Topics:

Processing steps for patterning SiO_2 on a silicon wafer

CMOS processing technology steps and their results
Layout design rules and their objectives
Scalable (λ-based) design rules
Design-rule checking

Learning Objectives:

1. Understand the **basic** steps of photolithography, its limitations, and how that determines minimum line width and device sizes.
2. Understand the processing steps required for fabrication of CMOS devises and the general results of each step.
3. Understand the physical defects that can arise in silicon processing and how design rules attempt to minimize their effects.
4. Understand the spacing and minimum device sizes specified by a typical set of design rules.
5. Understand the benefits and tradeoffs of a λ-based scalable design rule.
6. Understand the process and tools used for design rule checking.

CE-VLS3. Function of the Basic Inverter Structure
Suggested time: 5 hours
Topics:

Connectivity, layout, and basic functionality of a CMOS inverter
The CMOS inverter voltage transfer characteristic (VTC)
Analysis of the CMOS VTC for switching threshold, V_{OH}, V_{OL}, V_{IH}, V_{IL}, and Noise Margins
Effect of changing the inverter configuration on the CMOS VTC
Connectivity and basic functionality of a Bipolar ECL inverter (optional)
Connectivity and basic functionality of a Bipolar TTL inverter (optional)

Learning Objectives:

1. Understand the basic functionality of the CMOS inverter.
2. Understand how the VTC of a CMOS inverter is derived from the PMOS and NMOS characteristic I_D vs. V_{DS} family of curves.
3. Be able to analyze the VTC to determine switching threshold, V_{OH}, V_{OL}, V_{IH}, V_{IL}, and Noise Margins.
4. Understand how these quantities reflect the ability of the inverter to operate in the presence of noise.
5. Understand how changing the configuration of the inverter and the MOSFETS that make it up changes the VTC and thus the inverter's operation.
6. (Optionally) Understand the functionality of Bipolar-based logic gates

CE-VLS4. Circuit Characterization and Performance
Suggested time: 3 hours
Topics:

Switching characteristics (rise and fall times, gate delays)
Power dissipation
Resistance and capacitance estimation
CMOS transistor sizing
Conductor sizing

Learning Objectives:

1. Understand the basic causes of propagation delay and power dissipation in CMOS logic.
2. Understand the techniques for estimating parasitic resistance and capacitance for various layers on a CMOS integrated circuit.
3. Understand the effects of changing (and optimizing) the transistor widths in CMOS logic.
4. Understand the effects of changing (and optimizing) the conductor widths on a CMOS integrated circuit.

CE-VLS5. Combinational Logic Circuits
Suggested time: 4 hours
Topics:

Basic CMOS gate design
Layout techniques for combinational logic structures
Transistor sizing for complex CMOS logic devices
Transmission gates
Architectural building blocks (multiplexers, decoders, adders, counters, multipliers)

Learning Objectives:

1. Understand how the circuit design for CMOS logic gates is performed.
2. Understand the techniques, such as Euler paths and stick diagrams, which are used to optimize the layout of CMOS logic circuits.
3. Understand how the size for each transistor in a CMOS logic gate can be determined.
4. Understand the functionality of the CMOS transmission gate and how it is used in several logic functions (multiplexers, transmission gate-based XOR gates, etc.)
5. Understand the functionality of several of the more important architectural building blocks identified above and how they can be optimized for CMOS implementation.

CE-VLS6. Sequential Logic Circuits
Suggested time: 5 hours
Topics:

Storage mechanisms in CMOS logic
Dynamic latch circuits
Static latch and flip-flop circuits
Sequential circuit design
Single and multiphase clocking
Clock distribution, clock skew

Learning Objectives:

1. Understand how charge storage (capacitance) and feedback can be used to store values in CMOS logic.
2. Understand the circuit design, functionality and advantages and disadvantages of dynamic latches in CMOS.
3. Understand the circuit design, functionality and advantages and disadvantages of static latches and flip-flops (including edge-triggered) in CMOS.
4. Understand the concepts of bi-stability and metastability in static flip-flops.
5. Understand how latches and flip-flops are used in the design of state machines and data paths
6. Understand the functionality and advantages and disadvantages of single phase clocking, both level sensitive and edge triggered.
7. Understand the functionality and advantages and disadvantages of multi (two) phase clocking.
8. Understand the problems arising from clock skew and how clock distribution schemes (including the use of PLLs) can be used to solve it.

CE-VLS7. Alternative Circuit Structures/Low Power Design
Suggested time: 3 hours
Topics:

NMOS, Pseudo-NMOS, Domino-CMOS, CVSL
Low power design

Learning Objectives:

1. Understand how MOSFET-based logic families other than CMOS are implemented.
2. Understand the advantages and disadvantages of these logic families.
3. Understand the reasons for dynamic and static leakage power
4. Understand how to design CMOS circuits for low power

CE-VLS8. Semiconductor Memories and Array Structures
Suggested time: 4 hours
Topics:

Memory system organization
Read-only memory circuits

EPROM/EEPROM/Flash memory circuits
Static read-write memory (SRAM) circuits
Dynamic read-write memory (DRAM) circuits
Programmable Logic Array (PLA) circuits

Learning Objectives:

1. Understand how memory systems are organized and why they are not typically organized in the most simplistic arrangement – that of a one-dimensional word array.
2. Understand the circuit-level implementations possible for read-only memory (ROM) organizations.
3. Understand the layout and function of the specialized transistors used in non-volatile ROM devices and how their characteristics influence the circuit-level implementations of ROMs using them.
4. Understand the functionality and layout of cells used to implement static RAM (SRAM) memories.
5. Understand how SRAMs are typically organized and how their associated peripheral circuitry (sense amps, decoders, address translation detectors, etc.) is organized and functions.
6. Understand how a typical 3-transistor and 1-transistor DRAM cell functions and how they are typically laid out.
7. Understand how DRAMs are typically organized and accessed, and how their associated peripheral circuitry (sense amps, decoders, etc.) is organized and functions.
8. Understand how PLAs function, how can be implemented in CMOS, and how logic functions are mapped to them.

CE-VLS9. Chip Input/Output Circuits
Suggested time: 2 hours
Topics:

General I/O pad issues
Bonding pads
ESD Protection circuits
Input, Output, Bidirectional, and analog pads
VDD and VSS pads

Learning Objectives:

1. Understand the unique functions that I/O circuits must perform and their general circuit-level implementations.
2. Understand the functions of signal I/O pads and their general transistor-level implementations.
3. Understand the functions of VDD and VSS pads for both the core and padframe, and their general transistor-level implementations.

CE-VLS10. Semi custom Design Technologies
Suggested time: 2 hours

Topics:

Full custom methodology
Standard cell methodology
Gate array technologies
Programmable logic technologies
Field-programmable gate arrays (FPGAs)
Time to market and design economics

Learning Objectives:

1. Understand the different design techniques, methodologies, and implementation technologies available to implement a function on a single integrated circuit.
2. Understand the advantages and disadvantages of each and how a designer might go about selecting a specific one for his or her current project.

CE-VLS11. ASIC Design Methodology
Suggested time: 4 hours
Topics:

ASIC design flow (custom, semicustom)
Design hierarchy
Computer-aided design (CAD)
- Design modeling and capture (schematic, HDL)
- Design verification (formal, simulation, timing analysis)
- Automated synthesis
- Layout, floorplanning, place and route
- Back annotation

Semi-custom design with programmable logic devices and programmable gate arrays
System-on-chip (SOC) design and intellectual property (IP) cores
Testing and design for testability
Verification

Learning Objectives:

1. Understand the more detailed design issues present in implementing a given digital system on an Application-Specific Integrated Circuit (ASIC)
2. Understand the function, capabilities, and disadvantages of the various Computer-Aided Design (CAD) tools available to the ASIC designer to automate portions of the design process.
3. Understand the issues that come with implementing a real-world, complex design in an ASIC for a production environment.
4. Understand the basic principles of test generation and design for testability
5. Understand the difference between testing and verification