

Digital Logic (CE-DIG)

CE-DIG0. History and overview of digital logic [core]

CE-DIG1. Switching theory [core]

CE-DIG2. Combinational logic circuits [core]

CE-DIG3. Modular design of combinational circuits [core]

CE-DIG4. Memory elements [core]

CE-DIG5. Sequential logic circuits [core]

CE-DIG6. Register Transfer Logic [core]

CE-DIG7. Digital Systems Design [core]

The logic design area covers the digital building blocks, tools, and techniques in digital design. Emphasis is on a building-block approach. This subject area comprises approximately 3 semester hours.

CE-DIG0. History and overview of digital logic [core]

Suggested time: 1 hour

Topics:

- Indicate some reasons for studying digital logic.
- Highlight some people that influenced or contributed to the area of digital logic.
- Indicate some important topic areas such as logic circuits, switching, memory, registers, and digital systems.
- Highlight the importance of Boolean logic to the knowledge area.
- Mention the meaning and importance of sequential logic.
- Contrast the meanings of gates, circuits, combinational circuits, and modules.
- Indicate that memory is a logical circuit.
- Highlight that a special form of memory module forms registers.
- Mention how systems result from modules and circuits.
- Explore some additional resources associated with digital logic.
- Explain the purpose and role of digital logic in computer engineering.

Learning objectives:

- Identify some contributors to digital logic and relate their achievements to the knowledge area.
- Explain why Boolean logic is important to this subject.
- Articulate why gates are the fundamental elements of a digital system.
- Contrast the difference between a memory element and a register.
- Indicate some uses for sequential logic.
- Describe how computer engineering uses or benefits from digital logic.

CE-DIG1. Switching theory [core]

Suggested time: 6 hours

Topics:

Number systems and codes
Binary arithmetic
Boolean and switching algebra
Representation and manipulation of switching functions
Minimization of switching functions
Incompletely specified switching functions

Learning objectives:

1. To be able to work with binary number systems and arithmetic.
2. To be able to derive and manipulate switching functions, which form the basis of digital circuits.
3. To be able to reduce switching functions to simplified circuits used to realize them.

CE-DIG2. Combinational logic circuits [core]

Suggested time: 4 hours

Topics:

Basic logic gates (AND,OR,NOT,NAND,NOR,XOR)
Realization of switching functions with networks of logic gates
 2-level networks: AND-OR,OR-AND,NAND-NAND,NOR-NOR
 multi-level networks
Physical properties of logic gates (technology, fan-in, fan-out, propagation delay)
Elimination of timing hazards/glitches

Learning Objectives:

1. To be able to realize switching functions with networks of logic gates.
2. To be able to explain and apply fundamental characteristics of relevant electronic technologies, such as propagation delay, fan-in, fan-out, and power dissipation and noise margin.

CE-DIG3. Modular design of combinational circuits [core]

Suggested time: 6 hours

Topics:

Design of medium scale combinational logic modules
 Multiplexers, demultiplexers, decoders, encoders, comparators
Arithmetic functions (adders, subtracters, carry lookahead)
Multipliers, dividers
Arithmetic and logic units (ALUs)
Hierarchical design of combinational circuits using logic modules

Learning Objectives:

1. To be able to analyze and explain uses of small- and medium-scale logic functions as building blocks.
2. To be able to analyze and design combinational logic networks in a hierarchical, modular approach, using standard and custom logic functions.

CE-DIG4. Memory Elements

Suggested time: 3 hours

Topics:

- Unclocked and clocked memory devices (latches, flip flops)
- Level vs. edge-sensitive, and master-slave devices
- Basic flip flops (SR, D, JK, T)
- Asynchronous flip flop inputs (preset, clear)
- Timing constraints (setup time, hold time) and propagation delays
- Data registers (selection, clocking, timing)
- Random-access memory (RAM)

Learning Objectives:

1. To be able to design and describe the operation of basic memory elements.
2. To be able to analyze circuits containing basic memory elements.
3. To apply the concepts of basic timing issues, including clocking, timing constraints, and propagation delays during the design process.

CE-DIG5. Sequential Logic Circuits

Suggested time: 12 hours

Topics:

- Finite state machines (FSMs) - clocked and unclocked
- Mealy vs. Moore models of FSMs
- Modeling FSM behavior
 - State diagrams and state tables
 - Timing diagrams
 - Algorithmic state machine charts
- Analysis of synchronous and asynchronous circuits
- Design of synchronous sequential circuits
 - State minimization
 - State assignment
 - Next state and output equation realization
- Sequential functional units
 - Data registers
 - Shift registers
 - Counters
 - Sequence detectors
 - Synchronizers
 - Debouncers
 - Controllers

Learning Objectives:

1. To be able to analyze the behavior of synchronous and asynchronous machines
2. To be able to synthesize synchronous and asynchronous sequential machines

CE-DIG6. Register Transfer Logic [core]

Suggested time: 6 hours

Topics:

- Register transfer notation
 - data flow components
 - control flow components
- Conditional and unconditional transfers
- ALU control
- Bus structures
- Logic sequencers

Learning Objectives:

1. To introduce the notion of register transfer as a higher-level way to describe system behavior.

CE-DIG7. Digital Systems Design [core]

Suggested time: 12 hours

Topics:

- Hierarchical, modular design of digital systems
- Digital circuit modeling
 - Block diagrams
 - Timing diagrams
 - Register transfer languages
 - Algorithmic state machines
 - HDL (VHDL, Verilog)
- Simulation of digital circuit models (HDL, schematic, etc.)
- Synthesis of digital circuits from HDL models
- Design principles and techniques
 - Bridging conceptual levels – top down/bottom up
 - Divide and conquer
 - Iteration
 - Satisfying a behavior with a digital structure
- Functional units, building blocks and LSI components
 - Bus, adder, shifter, register, ALU, and control circuits
 - Tristate devices and buses
- Clock generation and distribution
- Control concepts
 - Major control state
 - Sequence of microoperations
 - Event schematic for macrosequences
 - Conditional execution of microoperations

Timing concepts

System timing dependencies

Sequencing

Clock skew

Programmable logic devices (PLDs) and field-programmable gate arrays (FPGAs)

PLAs, ROMs, PALs, complex PLDs

Digital-to-analog and analog-to-digital conversion

Testing

Learning Objectives:

1. To be able to apply digital system design principles and descriptive techniques.
2. To be able to analyze and design functional building blocks and control and timing concepts of digital systems.