Flip Chip Technologies
Constructions, Materials, Assembly & Reliability

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Flip Chip

- Introduction
- Types of Flip Chip Assemblies
- Issues
  - Bumping
  - Substrates
  - Assembly
  - Reliability
- Conclusions
Introduction - Flip Chip

Semiconductor die assembled by inverting die and making electrical contact between pads on die and pads on substrate. Also provides mechanical attachment.

Driving Forces

- Shortest electrical connection
  - High performance
    - Mainframes
  - Area array connections
    - High I/O
      - ASICs
      - Microprocessors
  - Smallest form factor
    - Portable electronics
- Mass reflow/SMT like assembly
  - High volume electronics
“Perceived” Limitations

- Requires underfill
- Limited pre-test, known good die
- Rework
- Die availability, bumping

Market Segmentation

- Flip Chip Packages
  - High I/O, High Performance
    - Microprocessors
    - ASICs
  - Component level qualification
Flip Chip Packages: Production and Developmental

Flip Chip on Laminate Package

Courtesy: Amkor
Flip Chip on Laminate Package

Courtesy: Amkor
Flip Chip in Package

Flip Chip on Ceramic Package

Courtesy: Amkor
### JEDEC Moisture Sensitivity

- Component level testing
- The flip chip package will be subjected to reflow cycle(s) in next level assembly.
- Popcorning

<table>
<thead>
<tr>
<th>Level</th>
<th>Floor Life</th>
<th>Soak</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conditions</td>
<td>Time</td>
</tr>
<tr>
<td>1</td>
<td>&lt;30°C 85%RH</td>
<td>Unlimited</td>
</tr>
<tr>
<td>2</td>
<td>&lt;30°C 60%RH</td>
<td>1 year</td>
</tr>
<tr>
<td>2a</td>
<td>&lt;30°C 60%RH</td>
<td>4 weeks</td>
</tr>
<tr>
<td>3</td>
<td>&lt;30°C 60%RH</td>
<td>168hrs</td>
</tr>
</tbody>
</table>

Joint IPC/JEDEC Standard J-STD-020A
JEDEC Moisture Sensitivity

- Following soak, parts are subjected to 3 reflow cycles
  - Eutectic Sn/Pb
  - Lead-free
- Inspected:
  - Electrical
  - Visual for cracks
  - Acoustic microscopy for delamination

Delamination

Courtesy: Amkor
Delamination & Solder Flow

Market Segmentation

- Flip Chip on Laminate
  - Low to medium I/O
  - Size, weight driven
  - Volume production driven
  - Cost sensitive
  - Mixed assembly with SMT
  - Rework (?)
  - Board level qualification
Interconnection Options

- Solder
  - High lead
  - Tin/Lead Eutectic
  - No-lead
- Conductive Adhesive
  - Isotropic
  - Anisotropic
- Themo-compression
  - Gold

Solder Based Interconnect
High Lead Solders (>90% Pb)

- Allows secondary assembly operations with eutectic Sn/Pb solder
- High temperature operation (automotive)
- Ceramic substrate
- Laminate substrates with eutectic paste

Eutectic Solder

- Most common
  - Compatible with laminate substrates
  - Compatible with SMT assembly*

* requires some process modification
No-Lead Solder

- Response to potential legislation banning use of lead in solders
- Activity in Europe and Japan
- Developmental

Table III: Thermal Fatigue Life Comparison of Bump Alloys
(normalized to 63Pb/Sn with no underfill)

<table>
<thead>
<tr>
<th>Solder Alloy Composition</th>
<th>Reflow Temperature (°C)</th>
<th>Fatigue Life without Underfill</th>
<th>Fatigue Life with Underfill</th>
</tr>
</thead>
<tbody>
<tr>
<td>63Sn/37Pb</td>
<td>230</td>
<td>1.0</td>
<td>15</td>
</tr>
<tr>
<td>58Sn/42Pb</td>
<td>360</td>
<td>1.2</td>
<td>Not Tested</td>
</tr>
<tr>
<td>37Sn/63Pb</td>
<td>260</td>
<td>2-3</td>
<td>&gt;30</td>
</tr>
<tr>
<td>3.5Ag/96Sn</td>
<td>260</td>
<td>0.5</td>
<td>11</td>
</tr>
<tr>
<td>58Sn/42Sb</td>
<td>280</td>
<td>0.3</td>
<td>11</td>
</tr>
<tr>
<td>SnTe/Cd/Zn</td>
<td>230</td>
<td>1.0</td>
<td>13</td>
</tr>
<tr>
<td>Sn/Ag/Cu/Sb</td>
<td>260</td>
<td>1.0</td>
<td>13</td>
</tr>
</tbody>
</table>

(Courtesy of K&S Flip Chip Division)

LF-2: 95.5Sn-3.8Ag-0.7Cu

RESULTS

![Graph showing results of LF-2 and other solder alloys](image)
Gold Stud Bumping

- Solder assembly
- Conductive adhesive
  - Isotropic
  - Anisotropic

Gold Stud Bumping

- Thermosonic gold wire bonder
- No special wafer processing
- Slow, not suited for high I/O density die
- Lower temperature assembly
  - With adhesives
Stud Bumping

Au Stud Bumping

Lead-free solder printed or coated on substrate

Underfill resin dispense

Underfill resin cure

Courtesy: Amkor
Au Stud Bumping

Amkor test die, 137µm pitch, Au stud bump
SnAg solder, 100x

Amkor Test Die, 300µm pitch, Au stud bump, SnAg solder

IC

2L thin core laminate substrate
Gold bump
SnAg solder

Cu trace, Ni/Au plate
Auto++ 1/50

Conductive Adhesives

- Isotropic
  - Stud bump
    - Matsushita
Stud Bump Assembly

PASTE TRANSFER APPLICATOR

Stud Bump Assembly

SAMPLE TR83
FLIP CHIP BOND

15KV 0.80KX_10U0635
Issues: Assembly

- Conductive adhesive
  - Isotropic
    - Placement accuracy
    - Speed
    - Requires underfill

Conductive Adhesives

- Polymer bump
- Polymer Flip Chip
  - Smart cards
  - Low temperature processing

(Courtesy: Polymer Flip Chip Corp)
Bumping: Conductive Adhesive

- Polymer Bump
  - Zincate/Electroless Ni/Pd UMB
  - Polyimide passivation screen printed and cured (optional)
  - Silver-filled epoxy or thermoplastic bump stencil printed and cured

Conductive Adhesives

- Anisotropic
  - Chip-on-glass
  - Displays

Die | Adhesive | Glass Substrate
---|---|---
ACF
Conducting particle
Electroless Ni/Au Plated Bumps for Anisotropic Adhesive

(Courtesy of Fraunhofer Institute for Reliability and Microintegration FhG-IZ)

Anisotropic

(Courtesy: Amkor)
Issues: Assembly

- Anisotropic
  - Substrate topology
  - Placement speed (bonding time)
  - Conductivity & repeatability

Thermo-compression

- Gold bumps
  - Electroplated
  - Wire stud bumped
- Specialty application
  - RF/μWave
  - High temperature
  - Optical
Issues: Assembly

- Thermo-compression
  - Bond time
  - Bond force
  - Bond temperature
  - Underfill may be required

Issues

- Solder based
  - Bumping
  - Substrates
  - Assembly
  - Reliability
Issues : Solder Bumping

- Additional wafer processing
- Pad pitch
  - Wire bond pads <100μm
- Redistribution
- Die shrink
- Cost
- Testing

Die Shrink
Under Bump Metallurgy

- Under-bump-metallurgy (UBM) is a solderable terminal on a bare IC.
- It serves as a transition between the aluminum IC metallization and the solder bump.

Requirements for UBM are:
- Low electric contact resistance
- Good adhesion to passivation and aluminum IC metallization
- Effective diffusion barrier
- Solderable layer with proper thickness
- Protecting IC metallization from the environment
Solder Bumping: Under Bump Metallurgy (UBM)

- Vacuum Deposition
  - Cr/Cr-Cu/Cu/Au
  - Al/Ni-V/Cu
  - Ti-W/Ni/Pd/Au
- Electroless Plating
  - Zincate/electroless Ni/electroless Au
    - Low cost option (maskless)

Vacuum UBM Process

1. Passivation
2. Deposition of UBM by Evaporation or Sputtering
3. Apply and Image Photoresist
4. Etch UBM/Strip Resist
Electroless Ni/Au UBM Process

1. Wafer backside coat
2. Al clean
3. Rinse
4. Zincate
   - Zincate-process
     - Activation of the Al using a zincate solution
       - Sodium hydroxide $\rightarrow$ dissolves the aluminum oxide
       - Zinc oxide $\rightarrow$ zinc deposition
5. Rinse
6. Electroless Ni plate
7. Rinse
8. Immersion Au plate
9. Rinse
   - Remove coating (optional)
As-received Aluminum

After Zincating

Courtesy: IC Interconnect
Uneven Zincating

Uniform Zincating

Courtesy: IC Interconnect
After Ni Plating

Nickel Plating
After Thick Ni/Au Plating

Design Rules

- Vary from bumping process to process
  - Electroplating allows tightest pitch
- Most recommend no corner bumps except as non-electrical orientation bumps for pick & place vision system
- Ink dots commonly ‘disappear’ during bumping - need electronic wafer map
Design Rules: Vacuum Deposited

- **UBM** - Under Bump Metallurgy
- **Die Passivation** (not shown in top view for clarity)
- **Final Metal Pad**
- **Passivation Opening** opening is passivation layer to metal pad
- **Silicon Wafer** (not shown in top view for clarity)

**Rule 1.** \( H_{\text{max}} = \frac{1}{2}(\text{Pitch} - \text{PO} - 10\mu\text{m}) \)

**Rule 2.** \( \text{Pitch min} = \text{PO} + 2h + 10\mu\text{m} \)

**Rule 3.** Minimum Passivation Opening (PO) = 25um

Design Rules: Electroless Plated

- **H** = plated nickel height
- **PO** = passivation opening
- **Pitch** = Center-to-center spacing between pads
- **WEB** = Pitch - PO

**Rule 1.** \( H_{\text{max}} = \frac{1}{2}(\text{Pitch} - \text{PO} - 10\mu\text{m}) \)

**Rule 2.** \( \text{Pitch min} = \text{PO} + 2h + 10\mu\text{m} \)

**Rule 3.** Minimum Passivation Opening (PO) = 25um
Redistribution

- Allows ICs with peripheral pad pitches of <150µm to be bumped & assembled cost effectively
- Enables development of common footprints. Particularly useful for memory applications.
- Decouples die shrinks from the footprint. Flip chip footprint can be designed in anticipation of future shrinks
Redistribution

- Wider pitch allows wider UBM structures and taller bumps which provides improved thermal cycle fatigue life, underfill flow and tolerance of board flatness variations.
- Relief to substrate technology escape routing and use of simpler less costly substrates.
- Assembly, cleaning, and underfill processing is enhanced.
- Potential of bump to bump shorting during reflow is reduced.

Redistribution

- Larger bumps provide improved current carrying characteristics and reduce electro-migration.
Bumping: Redistribution

- **Dielectrics**
  - Polyimide
    - Common die passivation
    - Higher moisture absorption
    - Can be photoimageable
  - Benzocyclobutene
    - Lower moisture absorption
    - Can be photoimageable

Bumping: Redistribution

- **Conductors**
  - Al
  - Ti/Cu/Ni
  - Al/Ni-V/Cu
  - Electroless Cu
Example Redistribution Process

- Coat with Polyimide 1
- Via 1 mask
- Deposit adhesion and plating seed layers (Ti and Cu)
- Metal 1 mask
- Plate metal (Cu and Ni)
- Strip resist
- Etch seed and adhesion layers
- Coat with Polyimide 2
- Via 2 mask
- Deposit bump adhesion and plating seed layers

Coat with Polyimide 1

After via 1 through polyimide 1

2-3um
After Metal 1 deposition, etch and strip

- 0.1um Ti
- 3-4um Cu
- 0.5um Ni

After Via 2 through Polyimide 2

- 50um
Ti/Cu seed deposition, mask

Electroplate Solder
After mask /seed removal

Reflow
Solder Bumping Formation

- Evaporation through shadow mask
- Electroplating
- Stencil printing
- Laser solder ball melting
- Solder jetting
- Thermo-compression of solder wire bonding
  - Under bump metallurgy may not be necessary

Evaporation Process

(a) Wafer clean
(b) Evaporation of UBM through metal mask
(c) Evaporation of high Pb solder through mask.
(d) Reflow to form solder ball
(e) Deposition of a Sn cap is a variation on the process

Evaporative Solder Bumping Process

(Courtesy: Flip Chip Technologies)
Shadow Mask

Evaporation of Solder Metals Through a Metal Mask

Electroplated Bumps

- **Common Alloys**
  - SnPb eutectic
  - High Pb (>90%)
  - SnCu
  - SnAg

(Courtesy: K&S Flip Chip Division)
Electroplated Bump

Reflowed Electroplated Bump

(Courtesy: FhG-IMZ)
Stencil Printing Process

- **Common Alloys**
  - SnPb eutectic
  - High Pb (>90%)
  - SnAgCu

---

Paste Types

<table>
<thead>
<tr>
<th>Type</th>
<th>None Larger Than (um)</th>
<th>Less Than 1% Larger Than (um)</th>
<th>80% Minimum Between (um)</th>
<th>10% Maximum Less Than (um)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>160</td>
<td>150</td>
<td>150-75</td>
<td>20</td>
</tr>
<tr>
<td>2</td>
<td>80</td>
<td>75</td>
<td>75-45</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>50</td>
<td>45</td>
<td>45-25</td>
<td>20</td>
</tr>
<tr>
<td>4</td>
<td>40</td>
<td>38</td>
<td>38-20</td>
<td>20</td>
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<tr>
<td>5</td>
<td>30</td>
<td>25</td>
<td>25-15</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
<td>15</td>
<td>15-5</td>
<td>5</td>
</tr>
</tbody>
</table>
After Paste Printing

(Courtesy: IC Interconnect)

After Reflow

(Courtesy: IC Interconnect)
After Reflow

(Laser Solder Ball Melting)

(Laser Solder Ball Melting)

Solder Ball Singulator

YAG Laser

Nitrogen
Solder Jetting

(Courtesy: MicroFab)
Issues: Substrates

- Wiring density
- Vias
- Solder mask registration
- Electrical test
- Surface finish

Traditional Laminate Substrates

- Low I/O count density
- Issues
  - Wiring density
  - Plugged vias
  - Solder mask resolution/registration
**Traditional Laminate Substrates**

- Single row Perimeter I/O
  - Wiring pitch must match die I/O
  - Solder mask registration critical

**Solder Mask Registration**

Solder mask shift = Distorted solder joints or shorts
More difficult to underfill
Solder Mask Misalignment

Other Pad Design Options

Uneven solder wettable area = Uneven flip chip gap or thinned solder joints
Easier to underfill with fluxing underfill
Traditional Laminate Substrates

- Two row perimeter/low density area array
  - I/O pitch of outer row must allow 1 line route between, or
  - Plugged or tented vias

Two Row Perimeter
Two Row Perimeter

Solder Mask Issues
- +0.001 -0.002” typical registration tolerance
  - Depends on design and bump pitch
- Resolution (solder mask opening) determines wettable area
  - Opening too small = ball does not touch metal
  - Opening too small = fine pitch shorts
  - Opening too large = decreased gap height
Solder Mask Issues

- Solder mask thickness over Cu < 10μm
- Positive edge slope
  - Improves underfill process

Other Design Issue

- Copper should be thin to improve underfill flow without voids
High Density Interconnect (HDI)

- Fine Pitch Perimeter
- Area Array

High Density Interconnect

- Non-reinforced dielectric layers
  - Liquid or dry film
    - Photoimaged vias
    - Laser drilled vias
    - Plasma etched vias
- Reinforced dielectric layers
  - Laminate
    - Laser drilled vias
Laser Drilled (non-reinforced)

Source: DuPont

Laser Drilled (reinforced)

(Courtesy - Hadco)
**Photo Via**

(Courtesy - DuPont)

**SLC Substrate**

1. Coat liquid dielectric 1
2. Soft cure
3. Photoimage & develop
4. Cure
5. Electroless Cu plate & image
6. Coat liquid dielectric 2
7. Soft cure
8. Photoimage & develop
9. Cure
10. Drill PTH
11. Electroless Cu plate & image
12. Solder mask
Substrate Technologies

Sequential Bonded Solid Vias (ALIVH)

Substrate Technologies

Laser Blind Vias
Wiring & Vias

Dog Bone Design

As pitch gets finer, area for vias decreases. Also requires soldermask.

Wiring & Vias

Via in Pad
No soldermask

Issues:
- Volume of solder in via
- Trapped void
Option: Filled via
Via in Pad Design

Photos courtesy of Jabil Circuit, Inc.

Surface Finish

- Electroless Ni/Immersion Au
  - <1% by volume Au in solder joint
- Organic surface protectant (OSP)
  - May not require solder mask
  - Solderability
- Palladium
  - Expensive
- Silver
  - Recommended for high temperature/high current use
- Tin
  - Limited solderability with multiple refloows
    - Intermetallic formation and oxidation
A word of caution...

- The gold plating volume within the solder joint should be less than 3% and preferably less than 1% to avoid embrittlement of the joint and intermetallic formation.
- Gold thickness will depend on solder volume
- Current industry issue with Electroless Ni/Immersion Au.
  - Low occurrence rate of failures in mechanical shock related to the immersion gold process

Solder Ball with Crack at Pad Interface

Courtesy: Bruce Houghton Celestica
Electroless Ni/Immersion Au

- Root cause (current theory): nickel is attacked or excessively corroded in the gold bath.
  - Somewhat design dependent
  - Somewhat chemistry dependent
  - Phosphorous content in Ni ???????

Traditional SMT machines do not use vision for part pick-up
- Vision occurs after pick-up
  - May include on-the-fly laser centering
- Initial part location tolerance important for die to be picked in center

Must consider bump up or bump down packaging
- If bump up, Pick & Place must have die flipping capability
- Wafer is bump-up
Packaging Options

- Waffle packs
- Tape & Reel
- Wafer
  - Care must be used with ejector pins to avoid microcracks in backside of silicon die
  - After underfill, backside of die is in tension and microcracks can lead to die facture

Flux Type

- Tacky
  - To hold chip in place while moving down assembly line
- No-clean
  - Preferred (most common)
  - Compatibility with underfill
    - Dispense and flow
    - Reliability
- No (Low)-Residue
Flux Type

- **Clean**
  - Solvent cleaning
    - Very small gap
      - Solvent penetration
      - Removal of solvent from gap
    - Centrifuge
    - Vapor
    - Ultrasonics
  - **Evaluation**
    - Quartz die
    - Phosphors in flux
    - Die shear
    - Improved reliability

Flux Application

<table>
<thead>
<tr>
<th>Option</th>
<th>Flux</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dip</td>
<td>Med. viscosity, No-clean or solvent clean</td>
<td>Increases placement cycle time</td>
</tr>
<tr>
<td>Spray</td>
<td>Low viscosity, No (low) residue</td>
<td>Flux applied over entire chip site including non-soldering areas</td>
</tr>
<tr>
<td>Print</td>
<td>Med. viscosity, No-clean or solvent clean</td>
<td>High throughput for boards/panels with many flip chip die</td>
</tr>
<tr>
<td>Flood Dispense</td>
<td>Low viscosity, No (low) residue</td>
<td>Flow of flux substrate topology dependent</td>
</tr>
</tbody>
</table>
Flux Dipping Process

Doctor blade
Dip flip chip balls into flux

Flux Wetting
Example of Soldermask Misalignment & Poor Wetting

Flux Residue
Industry Placement Requirements for Fine Pitch Components

Requirements insist the die to be no more than 20% off the center of the pad.

Courtesy: Siemens
Solder Inspection: X-Ray

Different solder ball diameters and small voids
Voids

Bridging
Origin of Voids

- In ball as formed during bumping
- Flux entrapment during reflow
  - Flux
  - Reflow profile

Underfill

- Purpose
  - Couples silicon die to substrate
  - Reduces shear stresses on solder joints
    - Structure warps with temperature change
- Key Requirements
  - Adhesion
  - CTE match to solder
  - High Tg
  - High Modulus
Modulus & CTE
Flip Chip on Laminate - FEA Models

ABAQUS

PEEQ Contours

Encapsulant A

CTE (x10^-6/°C)
74

E (GPa)
3.5

Encapsulant B

CTE (x10^-6/°C)
40

E (GPa)
5.9

Encapsulant C

CTE (x10^-6/°C)
23

E (GPa)
9.4

Underfill Options

- Capillary Flow
- Fluxing
- Transfer molded
- Wafer applied
Capillary Underfill

Capillary Flow
Capillary Flow

\[ t = \frac{3\mu L^2}{h\gamma \cos \theta} \]

t = flow time
\( \mu \) = absolute viscosity
L = distance traveled
h = gap height
\( \gamma \) = surface tension
\( \theta \) = wetting angle

Assumes:
1. Newtonian Fluid
2. Ignores Solder balls
Capillary Flow

- Traditional underfills
  - Slower underfill times
  - Fillet dispense
  - Long cure cycle
  - Higher filler content
- Fast flow/Snap cure
  - Fast dispense and flow
  - Self-filleting
  - Short cure cycle
  - Lower filler content

Processing

- Dehydration
  - May not be necessary with capillary flow underfills if underfilled immediately after reflow
    - Reflow drives off moisture
- Dispense
  - Underfill
  - Fillet formation
    - Not necessary with fast flow materials
- Cure
- Rework
Dispensing

- Material flows faster near solder balls
- Develop dispense pattern to eliminate voids
- Pattern must be developed for each new die and substrate design

Dispense Patterns

- Line Pattern
- Dot Pattern
- “L” Pattern

Fillet dispense if necessary
Flow Lines


Underfill Flow: Quartz Die

Self-filleting of Fast Flow Material
Voids

Void-free
Filler Separation (Settling)

Dispense Volume

- Volume control in dispensing important
- Fillet volume varies to compensate for variations in gap height
Curing

- Batch
  - Traditional underfill
- In-line Vertical Ovens
  - Traditional underfill
- In-line Horizontal Ovens
  - Snap cure underfill

Snap Cure

![Graph showing temperature over time](image-url)
Rework

- Relatively easy prior to underfill
  - Hot air rework station
- After underfill
  - Thermally reworkable underfills being developed
    - Hot air
    - Backside conduction
    - Mechanical removal of underfill residue

Rework (Initial)

(Courtesy: Loctite)
Rework (After Die Removal)

(Courtesy: Loctite)

Rework (After Clean-up)

(Courtesy: Loctite)
Process Automation

(Courtesy: Loctite)

Process Automation

(Courtesy: Loctite)
No-Flow Underfills

- Replaces flux application with underfill dispense
- Eliminates capillary underfill dispense and flow time
- May eliminate post reflow cure
- Eliminates flux-underfill interactions
  - No-clean
No-flow fluxing underfills

- Dehydration/Solder mask curing - Voids
- Still requires dispensing
- Solder wetting
- Shelf life
- Fillet formation
- Placement speed - Voids
- Reflow profile sensitive
- May still need post reflow cure or modified reflow profile
- Many do not contain fillers (<20%)

Effect of Filler

Solder ball prevented from touching the pad
Reflow Profile Sensitivity

- It is desirable that the underfill cure in single reflow cycle
- The reflow profile for fluxing underfill should be similar to a typical SMT reflow profile.
- This would enable mixture of DCA and other SMCs on a board to be reflowed at the same time

FB250 test vehicles assembled
- Sufficient amount of fluxing underfill
- Placement force: 6N
- Placement acc.: 0.1*g
- 94-98% underfill cured in one reflow cycle
- However, assembly yield was less than 40%
Reflow Profile Sensitivity

- Poor solder wetting was evident from cross-sections
- Die did not collapse completely
- It was confirmed that the problem was not due to
  - Low placement force
  - Die floating

Reflow Profile Sensitivity

- DSC analysis of fluxing underfill indicated
  - 150-160°C onset temperature of underfill curing
  - Curing reaction peaks at 200-220°C
- High soak temperature 165-180°C used in reflow cycle caused underfill gelation before solder reflow
Reflow Profile Sensitivity

- Modified reflow profile
  - Soak temperature: 140-155°C
  - Rapid ramp to peak reflow temperature
- FB250 test vehicles assembled
- 100% assembly yield obtained with good solder wetting

Placement DOE

- Taguchi’s $L_9(3^4)$ design
- Controllable factors
  - Placement acceleration
  - Placement force
  - Placement dwell time
  - Interactions
- Response Variable
  - Assembly yield
  - Placement voids
Test Vehicle

- PB8 2x2 die
  - 200μm pitch
  - 5mm die size

Finger Design

Levels

Siemens F5 Pick & place System

<table>
<thead>
<tr>
<th>Controllable Factor</th>
<th>Level 1</th>
<th>Level 2</th>
<th>Level 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A: Placement Force</td>
<td>1N</td>
<td>3N</td>
<td>5N</td>
</tr>
<tr>
<td>B: Placement Dwell Time</td>
<td>0s</td>
<td>1.5s</td>
<td>3s</td>
</tr>
<tr>
<td>C: Placement Acceleration</td>
<td>0.1g</td>
<td>1.3g</td>
<td>2.6g</td>
</tr>
</tbody>
</table>
### Test Results

- **Assembly Yield: 100%**

<table>
<thead>
<tr>
<th>Run No.</th>
<th>DOE factors</th>
<th>Samples (Voids)</th>
<th>n_{db}</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
<td>B</td>
<td>AxB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>3</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

### Placement Voids

- Quartz die also used to verify voids due to placement, not reflow
Results

- Variable A (placement force)
  - strong factor
- Variable C (placement acceleration)
  - moderate factor
- Variable B (placement dwell time)
  - weak factor
- The interaction between A and B is not significant

Optimum Parameters for Reducing Placement Voids

- Placement force at level 3 (5N),
- Placement dwell time at level 1 (0s)
- Placement acceleration at level 3 (2.6g).
Why maximum placement speed?

Placement with Optimized Parameters
Placement with Optimized Parameters
Voids

- Moisture
- Outgassing of incomplete cured solder mask
- Placement
- Board design

For area array, via-in-pad without solder mask is better
- Smoother board surface
- Openings in solder mask provide opportunity for air entrapment during dispense and compression flow of underfill
Molded

- Pick Die
- Flux
- Place Die
- Reflow

Transfer Mold

Molding

- Flip chip-in-package or module (SIP)
- Requires finer particle size than traditional molding compounds
  - Increased cost
- Requires vacuum or other means to eliminate void entrapment under the die
- Depending on mold design, direct contact to silicon backside for thermal transfer may be not be possible
Wafer Applied Underfill

Bumped Wafer

Underfill Coated Wafer

Assembly

Underfill Processing for Flip Chips

Current Process Flow

Solder Print

Addition to SMT Line

Place SMT parts

Solder reflow

Additions to SMT Line

Underfill Dispense

Underfill Cure

Wafer Applied Underfill Process Flow

Solder Print

Place SMT parts

Solder reflow
**Wafer Applied Underfill Assembly Process Flow**

1. **Dice Wafer**
2. **Coat Material**
3. **Tape & Reel or Tray Die**
4. **Pick up Package / Tack Surface**
5. **Place Package**
6. **Reflow Solder & Cure Encapsulant**
7. **Electrical Test Package & Repair if Necessary**

**Assembly Results on Optimal Coating**

Assembly on coated die with optimal coating:
- Good solder joint formation
- Optimal underfill volume
Wafer applied underfills

- Same concept as No-Flow underfill except applied at wafer level forming a solid film
- Eliminates dispensing
- May eliminate post reflow cure
- May be reworkable

➡️ At developmental stage

Reliability
Issues: Reliability

- Underfill delamination
- Solder fatigue (cyclic loading)
  - Thermal cycling
  - Power cycling
  - Substrate flexing
- Creep (constant loading - stress relaxation)
- Corrosion

Issues: Reliability

- Die fracture
- Silicon Cratering
- Excessive IMC Formation
- Electromigration
- Alpha Particles
Issues: Reliability

- Solder based
  - Underfill
    - Flux
    - Solder mask
    - Die passivation
    - Defects
    - Adhesion
    - Autoclave and Humidity
    - JEDEC Exposure

Test Methods

<table>
<thead>
<tr>
<th>Failure Mechanism</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder fatigue</td>
<td>Thermal Cycling</td>
</tr>
<tr>
<td>Corrosion</td>
<td>Autoclave 85C/85RH Bias Life (&lt;=10 mil pitch)</td>
</tr>
<tr>
<td>Excessive IMC Formation</td>
<td>High Temp Storage</td>
</tr>
<tr>
<td>Electromigration</td>
<td>Hi Temp Op-Life</td>
</tr>
<tr>
<td>Silicon Cratering</td>
<td>Die/Bump Shear</td>
</tr>
</tbody>
</table>
Reliability Test Monitoring

- It is critical that tests be monitored in-situ.
- Failures at high temperature are not failures at room temperature for 100’s of cycles.

Thermal Shock

![Graph showing percent failures against number of cycles for different conditions (E, I, K, C, D, H)]
Failure Mode

Thermal cycling

Flux
Delamination

![Image of delamination samples]

![Image of delamination chart with stress levels]

Delamination
Delamination

Board Cracking
Shorting

Cross Section

Flat Section (Die polished away)
Under force, time and temperature (junction temp = 165°C), a solder joint can experience creep. Underfill greatly minimizes solder creep.
Silicon Cratering

Die Fracture

Courtesy: Delphi Delco Electronics
High Temperature Exposure

- Without current
  - Intermetallic formation
  - UBM consumption
- With current
  - Intermetallic formation
  - Electromigration
  - UBM consumption

Intermetallic Formation

- Primary factors influencing UBM reliability are:
  - Metallurgy
  - UBM thickness
  - Bump alloy
  - Assembly processes
  - Service temperature
  - PWB surface finish
UBM Diffusion versus Dissolution

- **Hi Temp Storage**
  - Solid State Diffusion
  - Solder
  - Ni<sub>3</sub>Sn<sub>4</sub>
  - Ni

- **Number of Reflows**
  - Dissolution
  - Molten Solder
  - Ni

Effect of Multiple Reflows (Dissolution) on Ball Shear Strength

![Graph showing the effect of multiple reflows on ball shear strength.](image)

- **Mean**
- **1 Std Dev**
- **1 Std Dev**

Slide from Frank Stepniak - Delphi Deleo Electronics

Courtesy: K&S Flip Chip Division
IMC Formation After 3000 Hours Of Storage At 150°C (63Sn/Pb on organic)

Intermetallic Growth Structure Diffusion

Diffusion fastest along grain boundaries

Loss of adhesion
Intermetallic Formation

- Excessive Intermetallic Compound (IMC) can cause failures due to:
  - Embrittlement
  - Delamination
  - Dewetting

63Sn/Pb Electromigration Example

- Dark material is Pb, Bump Temperature of 150C

Pictures from Shih-Yeh Delphi Delco Electronics
Alpha Particles

- An alpha particle is the nucleus of a helium atom (He $^{4+}$).
- Alpha particles are emitted through the radioactive decay of radioactive impurities or isotopes in the packaging material.
- A high energy alpha particle (8MeV) could generate up to $2.5 \times 10^6$ electron-hole pairs and cause soft errors in a sensitive semiconductor device.

Alpha Particles

- The main source of alpha particles in flip chip packaging is lead (Pb) containing bump alloys.
- Trace amounts of thorium (Th), uranium (U), polonium (Po), and lead isotopes (Pb 214 & Pb 210) are the primary sources of alpha particles in the (Pb 206) and its alloys.
- Solutions:
  - low alpha emission Pb ($<0.02$ count/hr/cm$^2$)
  - Pb-free/Bi-free bump alloys
Summary - Flip Chips

- Solder based (eutectic) is the most common flip chip technology today.
- Technology is growing in both package and board assembly.
  - Flip chip-in-package growing faster
- Substrate density/cost remains a major issue.
- Alternates to capillary underfill process being explored.

Future

- Growing interested in 3-D folded flex with thinned silicon die and flip chip assembly

[Diagram showing 3-D folded flex with thinned silicon die and flip chip assembly]
Future