

# SN5450, SN7450

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

SDLS112 – DECEMBER 1983 – REVISED MARCH 1988

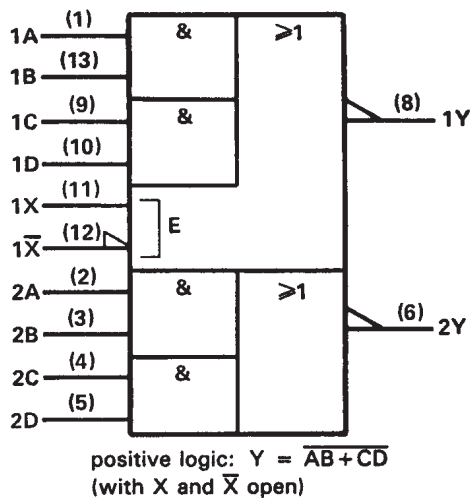
- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent 2-wide 2-input AND-OR-INVERT gates with one gate expandable. They perform the Boolean function  $Y = \overline{AB + CD}$  with X and  $\overline{X}$  left open.

The SN5450 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7450 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### logic symbol†

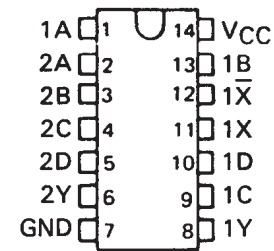


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

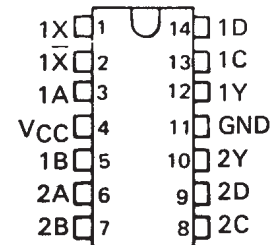
SN5450 . . . J PACKAGE  
SN7450 . . . N PACKAGE

(TOP VIEW)

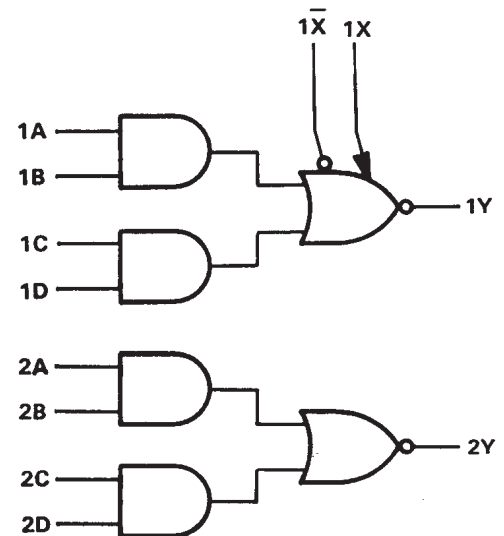


SN5450 . . . W PACKAGE

(TOP VIEW)



### logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

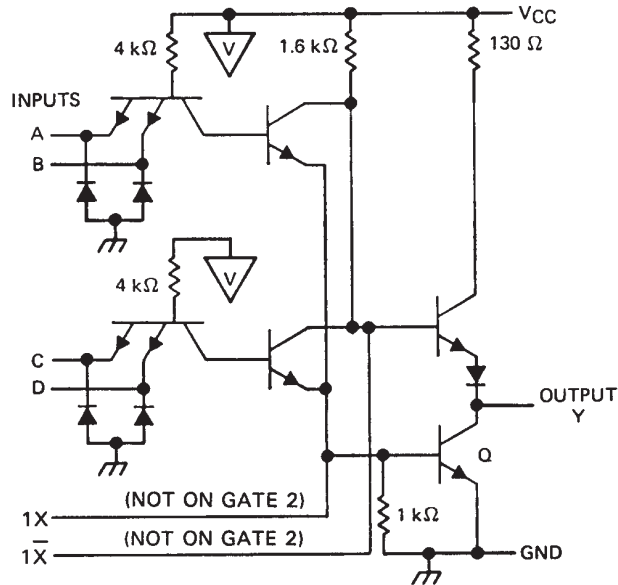
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## schematic (each AND-OR-INVERT gate)



Resistor values shown are nominal.  
If expander is not used, leave X and  $\bar{X}$  open.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature range: SN5450 .....	-55 °C to 125 °C
SN7450 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN5450, SN7450

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

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### recommended operating conditions

	SN5450			SN7450			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5450			SN7450			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2.4 V			40			40	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>IL</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20		-55	-18		-55	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		4	8		4	8	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, See Note 2		7.4	14		7.4	14	mA
I <sub>X</sub> ¶	V <sub>XX</sub> = 0.4 V, I <sub>OL</sub> = 16 mA			-2.9			-3.1	mA
V <sub>BE(Q)</sub> ¶	I <sub>X</sub> + I <sub>X</sub> = 0.41 mA, R <sub>XX</sub> = 0, I <sub>OL</sub> = 16 mA			1.1				V
	I <sub>X</sub> + I <sub>X</sub> = 0.62 mA, R <sub>XX</sub> = 0, I <sub>OL</sub> = 16 mA						1	
V <sub>OH</sub> ¶	I <sub>X</sub> = 0.15 mA, I <sub>X</sub> = -0.15 mA, I <sub>OH</sub> = -0.4 mA	2.4	3.4					V
	I <sub>X</sub> = 0.27 mA, I <sub>X</sub> = -0.27 mA, I <sub>OH</sub> = -0.4 mA				2.4	3.4		
V <sub>OL</sub> ¶	I <sub>X</sub> + I <sub>X</sub> = 0.3 mA, R <sub>XX</sub> = 138 Ω, I <sub>OL</sub> = 16 mA		0.2	0.4				V
	I <sub>X</sub> + I <sub>X</sub> = 0.43 mA, R <sub>XX</sub> = 130 Ω, I <sub>OL</sub> = 16 mA					0.2	0.4	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

¶ Using expander inputs, V<sub>CC</sub> = MIN, T<sub>A</sub> = MIN, except typical values.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Y	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF Expander pins open		13	22	ns
t <sub>PHL</sub>					8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
JM38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN7450N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7450N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SNJ5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ5450W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ5450W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN5450, SN7450 :**

- Catalog: [SN7450](#)
- Military: [SN5450](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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