3

High-Performance Analog Circuits

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3.1 Broadband Bipolar Networks

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3.1.1 Introduction

Numerous textbooks have presented excellent treatments of the design and analysis of broadband bipolar amplifiers. This chapter is concerned with techniques for integrated circuit amplifiers, and is written mainly as a tutorial aimed at the practicing engineer.

For broadband polar design, it is first important to identify the key difference between lumped and distributed design techniques. Basically when the signal wavelengths are close to the dimensions of the integrated circuit, then characteristic impedances become significant, lines become lossy, and we essentially need to consider the circuit in terms of transmission lines. At lower frequencies where the signal

wavelength is much larger than the dimensions of the circuit, the design can be considered in terms of lumped components, allowing some of the more classical low-frequency analog circuit techniques to be applied. At intermediate frequencies, we enter the realms of hybrid lumped/distributed design. Many radio-frequency (RF) designs fall into this category, although every day we see new technologies and circuit techniques developed that increase the frequency range for which lumped approaches are possible. In broadband applications, integrated circuits (ICs) are generally designed without the use of special microwave components, so broadband techniques are very similar to those employed at lower frequencies. However, several factors still have to be considered in RF design: all circuit parasitics must be identified and included to ensure accurate simulation; feedback can generally only be applied locally as phase shifts per stage are significant; the cascading of several local feedback stages is difficult since alternating current (ac) coupling is often impractical; the NPN bipolar transistor is the main device used in silicon, since it has potentially a higher f_t than PNP bipolar or MOSFET devices; active PNP loads are generally avoided due to their poor frequency and noise performance and so resistive loads are used instead.

The frequency performance of an RF or broadband circuit will depend on the frequency capability of the devices used, and no amount of good design can compensate for transistors with an inadequate range. As a rule, designs are kept as simple as possible, since at high frequencies all components have associated parasitics.

3.1.2 Miller's Theorem

It is important to describe at the outset a very useful approximation that will assist in simplifying the high-frequency analysis of some of the amplifiers to be described. The technique is known as Miller's theorem and will be briefly discussed here. A capacitor linking input to output in an inverting amplifier results in an input-referred shunt capacitance that is multiplied by the voltage gain of the stage, as shown in Figure 3.1. This increased input capacitance is known as the Miller capacitance.

It is straightforward to show that the input admittance looking into the inverting input of the amplifier is approximately $Y_{in} = j\omega C_f(1 + A)$. The derivation assumes that the inherent poles within the amplifier are at a sufficiently high frequency so that the frequency response of the circuit is dominated by the input of the amplifier. If this is not the case, then Miller's approximation should be used with caution as it will be discussed later. From the preceding model, it is apparent that the Thévenin input signal sources see an enlarged capacitance to ground. Miller's approximation is often a useful way of simplifying circuit analysis by assuming that the input dominant frequency is given by the simple low-pass *RC* filter in Figure 3.1. However, the effect is probably one of the most detrimental in broadband amplifier design, affecting both frequency performance and/or stability.

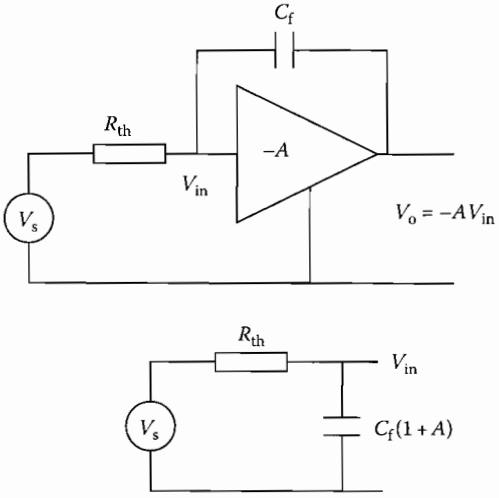


FIGURE 3.1 Example of the Miller effect.

3.1.3 Bipolar Transistor Modeling at High Frequencies

In this section, we consider the high-frequency small-signal performance of the bipolar transistor. The section assumes that the reader has some knowledge of typical device parameters, and has some familiarity with the technology. For small-signal analysis, the simplified hybrid-π model shown in Figure 3.2 is used,

where

r_b is the base series resistance
r_c is the collector series resistance
r_π is the dynamic base–emitter resistance
r_o is the dynamic collector–emitter resistance

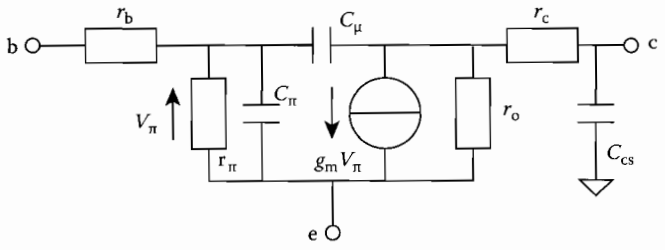


FIGURE 3.2 Hybrid π model of BJT.

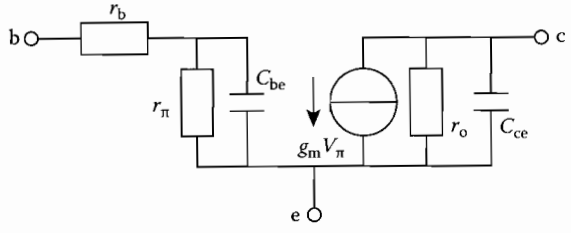


FIGURE 3.3 Simplified Miller-approximated hybrid π model of BJT.

C_π is the base–emitter junction capacitance
C_μ is the collector–base junction capacitance
C_{cs} is the collector–substrate capacitance
g_m is the small-signal transconductance

At low frequencies, the Miller approximation allows the hybrid-π model to be simplified to the circuit shown in Figure 3.3, where the net input capacitance now becomes $C_{be} = C_\pi + C_\mu (1 - A_v)$, the net output capacitance becomes $C_{ce} = C_\mu(1 - 1/A_v)$, where A_v is the voltage gain given by $A_v = (V_{ce}/V_{be}) \approx -g_m R_1$ where R_1 is the collector load resistance. r_c and C_{cs} have been neglected. Thus, $C_{be} \approx C_\pi + g_m R_1 C_\mu$ and $C_{ce} \approx C_\mu$. The output capacitance C_{ce} is often neglected from the small-signal model. The approximation $A_v = -g_m R_1$ assumes that $r_\pi \gg r_b$, and that the load is purely resistive. At high frequencies, however, we cannot neglect the gain roll-off due to C_π and C_μ, and even at frequencies as low as 5% of f_t the Miller approximation can introduce significant errors.

A simplified hybrid-π model that takes the high-frequency gain roll-off into account is shown in Figure 3.4. C_μ is now replaced by an equivalent current source $sC_\mu(V_\pi - V_{ce})$.

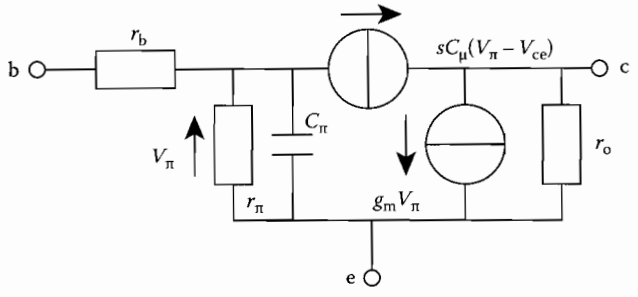


FIGURE 3.4 Simplified high-frequency model.

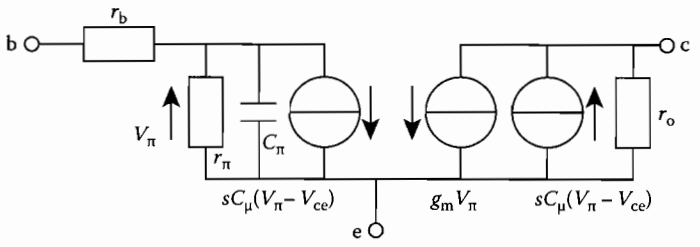


FIGURE 3.5 Split current sources.

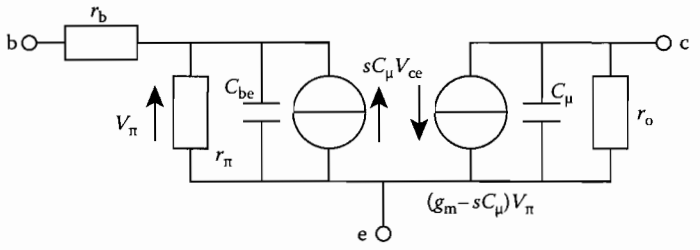


FIGURE 3.6 Modified equivalent circuit.

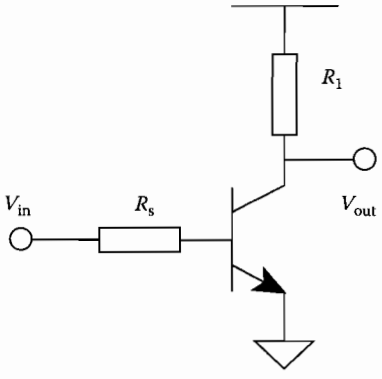


FIGURE 3.7 CE amplifier.

A further modification is to split the current source between the input and output circuits as shown in Figure 3.5.

Finally, the input and output component terms can be rearranged leading to the modified equivalent circuit shown in Figure 3.6, which is now suitable for broadband design. From Figure 3.6, the transconductance $(g_m - sC_\mu)$ shows the direct transmission of the input signal through C_μ. The input circuit current source $(sC_\mu V_{ce})$ shows the feedback from the output to the input via C_μ. Depending on the phase shift between V_{ce} and V_{be}, this feedback can cause high-frequency oscillation. At lower frequencies, $sC_\mu \ll g_m$ and $V_{ce}/V_\pi \approx -g_m R_1$, which is identical to the Miller approximation. The model of Figure 3.6 is the most accurate for broadband amplifier design, particularly at high frequencies.

3.1.4 Single-Gain Stages

Consider now the high-frequency analysis of single-gain stages.

3.1.4.1 Common-Emitter (CE) Stage

Figure 3.7 shows a CE amplifier with load R_1 and source R_s. External biasing components are excluded from the circuit.

First analysis using the Miller approximation yields the small-signal high-frequency model shown in Figure 3.8,

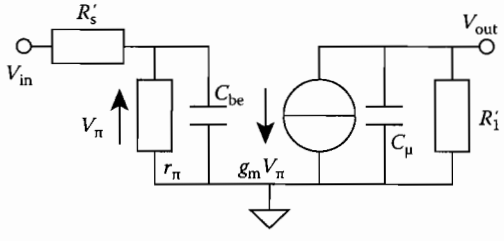


FIGURE 3.8 High-frequency model of the CE.

where

$$R_{1'} = (R_1 \| r_0), \quad R_{s'} = R_s + r_b \quad \text{and} \quad C_{be} = C_\pi + g_m R_{1'} C_\mu$$
$$\frac{V_\pi}{V_{in}} = \left(\frac{r_\pi}{r_\pi + R_{s'}}\right)\left(\frac{1}{1 + s(r_\pi \| R_{s'})C_{be}}\right) \tag{3.1}$$
$$\frac{V_{out}}{V_\pi} = \frac{-g_m R_{1'}}{1 + sC_\mu R_{1'}}$$

and thus

$$\frac{V_{out}}{V_{in}} = -\left(\frac{g_m R_{1'} r_\pi}{r_\pi + R_{s'}}\right)\left(\frac{1}{(1 + sC_\mu R_{1'})(1 + s(r_\pi \| R_{s'})C_{be})}\right) \tag{3.2}$$

This approximate analysis shows

- "Ideal" voltage gain $= -g_m R_1$
- Input attenuation caused by $R_{s'}$ in series with r_π
- Input circuit pole p_1 at $s = 1/C_{be}(r_\pi/R_{s'}) \approx 1/C_{be}R_{s'}$
- Output attenuation caused by r_0 in parallel with R_1
- Output circuit pole p_2 at $s = 1/C_\mu R_{1'}$

The input circuit pole is generally dominant, and thus the output pole p_2 can often be neglected. With a large load capacitance C_1, $p_2 \approx 1/C_1 R_{1'}$, and the gain and phase margin will be reduced. However, under these conditions the Miller approximation will no longer be valid, since the gain roll-off due to the load capacitance is neglected.

If we now consider analysis using the broadband hybrid-π model of Figure 3.6, then the equivalent model of the CE now becomes that shown in Figure 3.9, where

$$C_{be} = C_\pi + C_\mu, \quad R_{s'} = R_s + r_b \quad \text{and} \quad R_{1'} = R_1 \| r_0$$

From the model, it can be shown that

$$\frac{V_{out}}{V_\pi} = \frac{-(g_m - sC_\mu)R_{1'}}{1 + sC_\mu R_{1'}} \tag{3.3}$$

$$(V_{in} - V_\pi)/R_{s'} + sC_\mu V_{out} = V_\pi/r_\pi + sC_{be}V_\pi \tag{3.4}$$

and

$$V_{in} r_\pi + V_{out} sC_\mu r_\pi R_{s'} = V_\pi(r_\pi + R_{s'})(1 + sC_{be}(r_\pi \| R_{s'})) \tag{3.5}$$

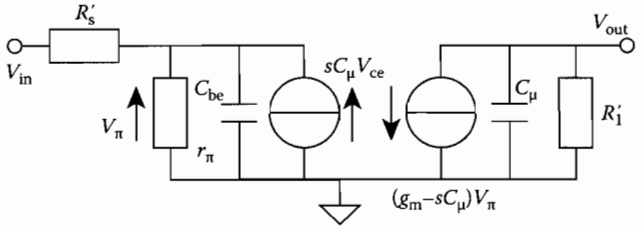


FIGURE 3.9 Equivalent circuit model of the CE.

Rearranging these equations yields

$$\frac{V_{out}}{V_{in}} = -\left(\frac{g_m R_{l'} r_\pi}{r_\pi + R_{s'}}\right) \times \left(\frac{1 - sC_\mu/g_m}{(1 + sC_{be}R_{s'})(1 + sC_\mu R_{l'}) + sC_\mu g_m R_{l'} R_{s'} - s^2 C_\mu^2 R_{s'} R_{l'}}\right) \tag{3.6}$$

This analysis shows that there is a right-hand-plane (RHP) zero at $s = 1/(C_\mu r_e)$, which is not predicted by the Miller approximation. Assuming $R_\pi \gg R_{s'}$ and $C_\pi \gg C_\mu$, the denominator can be written as

$$1 + s\left(R_{s'}\left(C_\pi + C_\mu g_m R_{l'}\right) + C_\mu R_{l'}\right) + s^2 C_\mu C_\pi R_{l'} R_{s'} \tag{3.7}$$

which can be described by the second-order characteristic equation

$$1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2 \tag{3.8}$$

By comparing coefficients in Equations 3.7 and 3.8, the sum of the poles is the same as that obtained in Equation 3.2 using the Miller approximation, but the pole product $p_1 p_2$ is greater. This means that the poles are farther apart than predicted by the Miller approximation. In general, the Miller approximation should be reserved for analysis at frequencies of operation well below f_t, and for situations where the capacitive loading is not significant. The equivalent circuit of Figure 3.9 therefore gives a more accurate result for high-frequency analysis. For a full understanding of RF behavior, computer simulation of the circuit including all parasitics is essential.

Since the CE stage provides high current and voltage gain, oscillation may well occur. Therefore, care must be taken during layout to minimized parasitic coupling between the input and output. The emitter should be at ground potential for ac signals, and any lead inductance from the emitter to ground will generate phase-shifted negative feedback to the base, which can result in instability.

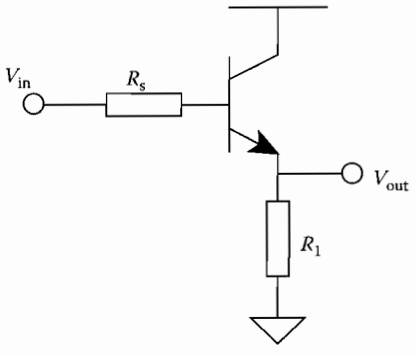


FIGURE 3.10 Common-collector amplifier.

3.1.4.2 Common-Collector (CC) Stage

The CC or emitter follower shown in Figure 3.10 is a useful circuit configuration since it generally serves to isolate a high-gain stage from a load. The high-frequency performance of this stage must be good enough not to degrade the frequency performance or stability of the complete amplifier. An equivalent high-frequency small-signal model of the CC is shown in Figure 3.11.

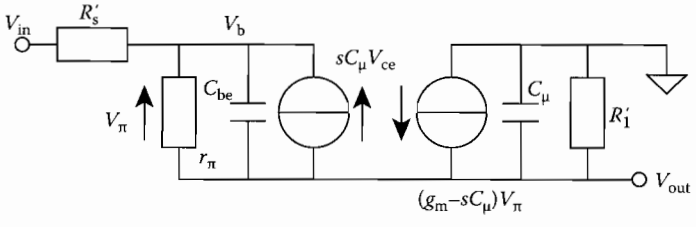


FIGURE 3.11 Equivalent circuit of the CC.

The following set of equations can be derived from Figure 3.11:

$$(V_{in} - V_b)/R_{s'} = V_\pi/r_\pi + sC_{be}V_\pi + sC_\mu V_{out}, \quad V_b = V_{out} + V_\pi \tag{3.9}$$

and

$$V_\pi/r_\pi + sC_{be}V_\pi + sC_\mu V_{out} + (g_m - sC_\mu)V_\pi - sC_\mu V_{out} - V_{out}/R_{1'} = 0 \tag{3.10}$$

Rearranging these equations yields

$$\frac{V_{out}}{V_{in}} = \frac{R_{1'}(1 + g_m r_\pi + sC_\pi r_\pi)}{(R_{s'} + r_\pi)(1 + s(R_{s'} \| r_\pi)C_{be}) + R_{1'}(1 + sC_\mu R_{s'})(1 + g_m r_\pi + sC_\pi r_\pi)} \tag{3.11}$$

The preceding expression can be simplified by assuming $R_\pi \gg R_{s'}$, $g_m r_\pi \gg 1$, $C_\pi \gg C_\mu$ to,

$$\frac{V_{out}}{V_{in}} = \left(\frac{r_\pi}{r_\pi + R_{s'}}\right)\left(\frac{1 + sC_\pi/g_m}{(1 + sC_\mu R_{s'})(1 + sC_\pi/g_m) + (1 + sC_\pi R_{s'})/g_m R_{1'}}\right) \tag{3.12}$$

This final transfer function indicates the presence of a left-half-plane zero at $s = (g_m/C_\pi) = \omega_t$. The denominator can be rewritten as approximately

$$(1 + 1/g_m R_{1'}) + s(C_\mu R_{s'} + C_\pi/g_m + C_{be}R_{s'}/g_m R_{1'}) + s^2 C_\mu C_\pi R_{s'}/g_m \tag{3.13}$$

which simplifies to

$$1 + s(C_\pi r_e + C_\mu R_{s'} + (C_\mu + C_\pi)r_e R_{s'}/R_{1'}) + s^2 C_\mu C_\pi R_{s'} R_{1'} \tag{3.14}$$

Assuming a second-order characteristic form of $1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2$, if $p_1 \ll p_2$, the above reduces to $1 + s/p_1 + s^2/p_1 p_2$. If $(R_{s'}/R_{1'}) \ll 1$, then $p_1 \approx 1/(C_\pi r_e)$, and this dominant pole will be approximately canceled by the zero. The frequency response will then be limited by the nondominant pole $p_2 \approx 1/C_\mu R_{s'}$.

The frequency response of a circuit containing several stages is thus rarely limited by the CC stage, due to this dominant pole-zero cancellation. For this analysis to be valid, $R_{s'} \ll R_{1'}$. As $R_{s'}$ increases the poles will move closer together, and the pole-zero cancellation will degrade. In practice, the CC stage is often used as a buffer, and is thus driven from a high source resistance into a low value load resistance.

A very important parameter of the common-collector stage is output impedance. It is generally assumed that the output impedance of a CC is low, also that there is good isolation between a load and the amplifying stage, and that any amount of current can be supplied to the load. Furthermore, it is assumed that capacitive loads will not degrade the frequency performance since the load will be driven by an almost short circuit. While this may be the case at low frequencies, it is a different story at high frequencies. Consider the following high-frequency analysis. We first assume that the small-signal model shown in Figure 3.12 is valid.

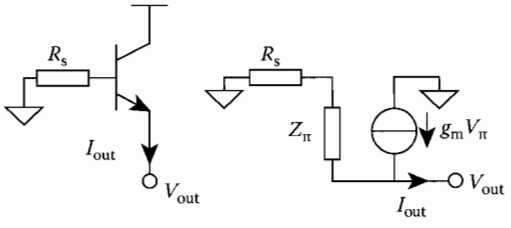


FIGURE 3.12 Equivalent circuit of the CC output stage.

From the Figure 3.12, the output impedance can be approximated as

$$\frac{V_{out}}{I_{out}} = \frac{Z_\pi + R_{s'}}{1 + g_{in}Z_\pi} \tag{3.15}$$

where $Z_\pi = (r_\pi \| C_{be})$ and $R_{s'} = R_s + r_b$. At very low frequencies ($\omega \to 0$):

$$R_{out} = \frac{r_\pi + R_{s'}}{1 + g_m r_\pi} \approx 1/g_m + R_{s'}/g_m r_\pi \approx r_e + R_{s'}/\beta \qquad (3.16)$$

At very high frequencies ($\omega \to \infty$):

$$R_{out} = \frac{1/sC_{be} + R_{s'}}{1 + g_m/sC_{be}} \approx R_{s'} \qquad (3.17)$$

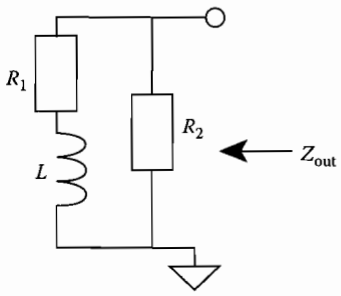


FIGURE 3.13 Equivalent high-frequency model of CC output stage.

If $r_e > R_{s'}$, then the output impedance decreases with frequency, that is, Z_{out} is capacitive. If $R_{s'} > r_e$, then Z_{out} increases with frequency, and so Z_{out} appears inductive. It is usual for an emitter follower to be driven from a high source resistance, thus the output impedance appears to be inductive and can be modeled as shown in Figure 3.13, where

$$R_1 = r_e + R_{s'}/\beta, \quad R_2 = R_{s'}, \quad L = R_{s'}/\omega_t$$

The inductive behavior of the CC stage output impedance must be considered in broadband design since any capacitive loading on this stage could result in peaking or instability. The transform from base resistance to emitter inductance arises because of the 90° phase shift between base and emitter currents at high frequencies, due principally to C_π. This transform property can be used to advantage to simulate an on-chip inductor by driving a CC stage from a high source resistance. Similarly, by loading the emitter with an inductor, we can increase the effective base series resistance $R_{s'}$ without degrading the noise performance of the circuit. A capacitive load will also be transformed by 90° between the base and emitter; for example, a capacitive loading on the base can look like a negative resistance at the emitter.

3.1.4.3 Common-Base (CB) Stage

The CB amplifier shown in Figure 3.14 offers the highest frequency performance of all the single-stage amplifiers. When connected as a unity gain current buffer, the CB stage operates up to the f_t of the transistor.

Using the simplified hybrid π model of Figure 3.3, it follows that

$$\frac{I_{out}}{I_{in}} \approx \frac{\beta}{\beta + 1} \quad \text{where} \quad \beta = \frac{\beta_o}{1 + s/\omega_o} \qquad (3.18)$$

$$\frac{I_{out}}{I_{in}} \approx \frac{a_o}{1 + s/\omega_t} \quad \text{where} \quad a_o = \beta_o/(\beta_o + 1) \quad \text{and} \quad \omega_t = \beta_o \omega_o \qquad (3.19)$$

The CB stage thus provides wideband unity current gain. Note that the input impedance of the CB stage is the same as the output impedance of the CC stage, and thus can appear inductive if the base series resistance is large.

In many situations, the CB stage is connected as a voltage amplifier, an example of this being the current-feedback amplifier, which will be discussed in a later section. Consider the following high-frequency analysis of the CB stage being employed as a voltage gain amplifier. Figure 3.15 shows the circuit together with a simplified small-signal model. From the equivalent model, the gain of the circuit can be approximated as

$$\frac{V_{out}}{V_{in}} = \frac{kR_1}{R_s}\left(\frac{1 - sC_\mu/g_m}{1 + s(C_\pi/g_m)(kR_{s'}/R_s)}\right) \qquad (3.20)$$

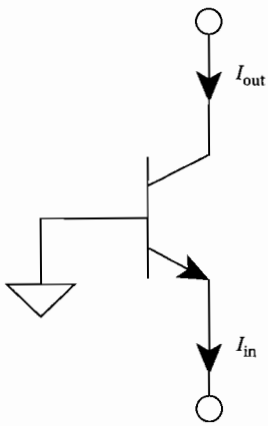


FIGURE 3.14 CB configuration.

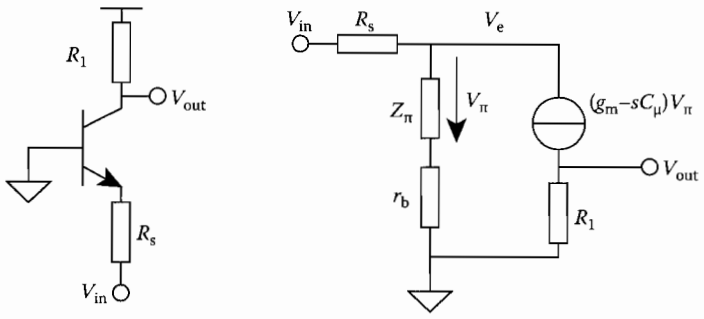


FIGURE 3.15 CB stage as a voltage amplifier.

where

$$R_{s'} = R_s + r_b, \quad \text{and} \quad k \approx \frac{R_s}{R_s + 1/g_m}$$

If $R_s \gg 1/g_m$, then $k \approx 1$ and so

$$\frac{V_{out}}{V_{in}} = \frac{R_1}{R_s}\left(\frac{1 - sC_\mu/g_m}{1 + s(C_\pi/g_m)(1 + r_b/R_s)}\right) \tag{3.21}$$

Thus, it can be seen that the circuit has an RHP zero at $s = 1/(r_e\ C_\mu)$, since $r_e = 1/g_m$ and a pole at $1/C_\pi r_e(1 + r_b/R_s) = \omega_t/(1 + r_b/R_s)$. Note that in the case of a current source drive ($R_s \gg r_b$), the pole is at the ω_t of the transistor. However, this does assume that the output is driven into a short circuit. Note also that there is an excellent isolation between the input and output circuits, since there is no direct path through C_μ and so no Miller effect.

3.1.5 Neutralization of C_μ

Many circuit techniques have been developed to compensate for the Miller effect in amplifiers and hence extend the frequency range of operation. The CE stage provides the highest potential power gain, but the bandwidth of this configuration is limited since the amplified output voltage effectively appears across the collector–base junction capacitance resulting in the Miller capacitance multiplication effect. This bandwidth limiting due to C_μ can be overcome by using a two-transistor amplifying stage such as the CE–CB cascode stage or the CC–CE cascade. Consider now a brief qualitative description of each in turn. The circuit diagram of the CE–CB cascode is shown in Figure 3.16.

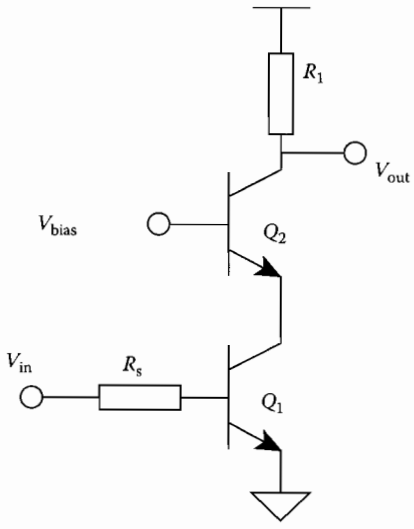


FIGURE 3.16 CE–CB cascode.

The CE transistor Q_1 provides high current gain of approximately β and a voltage gain of $A_{v1} \approx -g_{m1}R_1 = -g_{m1}r_{e2}$, which in magnitude will be close to unity. Therefore, the Miller multiplication of C_μ is minimized, and the bandwidth of Q_1 is maximized. The CB transistor Q_2 provides a voltage gain $A_{v2} \approx R_1/r_{e2}$. The total voltage gain of the circuit can be approximated as $A_v \approx -g_{m1}R_1$, which is equal to that of a single CE stage. The total frequency response is given by the cascaded response of both stages. Since both transistors exhibit wideband operation, then the dominant poles of each stage may be close in frequency. As a result, the total phase shift through the cascode

configuration is likely to be greater than that obtained with a single device, and care should be taken when applying negative feedback around the pair.

Consider now the CC–CE stage of Figure 3.17. In this case, voltage gain is provided by the CE stage transistor Q_2 and is $A_{v2} \approx -g_{m2}R_1$. This transistor is being driven from the low-output impedance of Q_1 and so the input pole frequency of this device ($\approx 1/C_{be2}R_{s2}$) is maximized. The CC stage transistor Q_1 is effectively a buffer that isolates C_μ of Q_2 from the source resistance R_s. The low-frequency voltage gain of this circuit is reduced when compared with a single-stage configuration because the input signal effectively appears across two base–emitter junctions.

The two-transistor configurations help to maintain a wideband frequency response by isolating the input and output circuits. In integrated circuit design, another method of neutralizing the effect of C_μ is possible when differential gain stages are used.

For example, Figure 3.18 shows a section of a differential input amplifier. If the inputs are driven differentially, then the collector voltages V_{c1} and V_{c2} will be 180° out of phase. The neutralization capacitors C_n thus inject a current into the base of each transistor that is equal and opposite to that caused by the intrinsic capacitance C_μ. Consequently, the neutralization capacitors should be equal to C_μ in order to provide good signal cancellation, and so they may be implemented from the junction capacitance of two dummy transistors with identical geometries to Q_1 and Q_2 as shown in Figure 3.19.

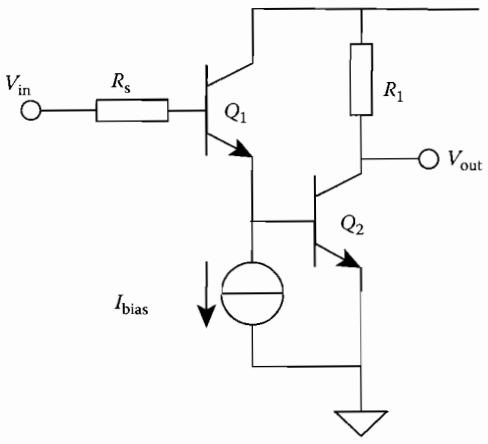


FIGURE 3.17 CC–CE stage.

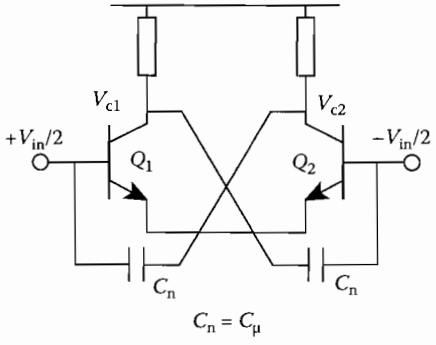


FIGURE 3.18 Differential gain stage.

3.1.6 Negative Feedback

Negative feedback is often employed around high-gain stages to improve the frequency response. In effect, the gain is reduced in exchange for a wider, flatter bandwidth. The transfer function of a closed-loop system can be written

$$H(s) = \frac{A(s)}{1 + A(s)B(s)} \tag{3.22}$$

where $A(s)$ is the open-loop gain and $B(s)$ is the feedback fraction. If the open-loop gain $A(s)$ is large, then $H(s) \approx 1/B(s)$. In RF design, compound or cascaded stages can produce excessive phase shifts that result in instability when negative feedback is applied. To overcome this problem, it is generally accepted to apply local negative feedback around a

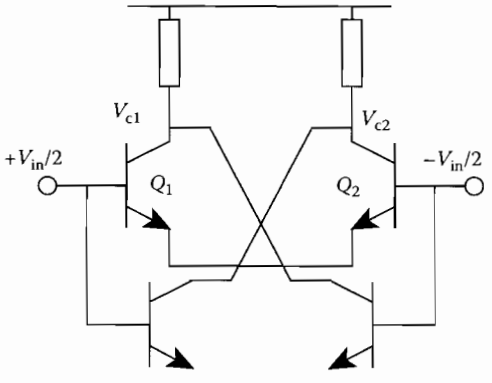


FIGURE 3.19 Implementation of neutralization capacitors.

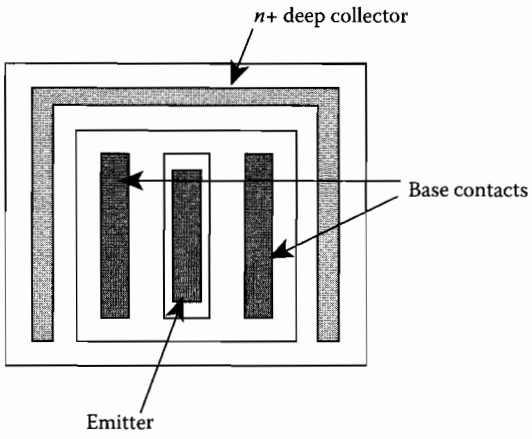


FIGURE 3.20 Stripe geometry.

single stage only. However, the open-loop gain of a single stage is usually too low for the approximation $H(s) = 1/B(s)$ to hold.

3.1.7 RF Bipolar Transistor Layout

When laying out RF transistors, the aim is to

- Minimize C_μ and C_π
- Minimize base width to reduce the forward transit time t_∂ and thus maximize ∂_t
- Minimize series resistance r_b and r_c

To minimize junction capacitance, the junction area must be reduced; however, this will tend to increase the series resistance. Transistors are generally operated at fairly high currents to maximize ∂_t. However, if the emitter gets too crowded, then the effective value of β will be reduced. The requirements given above are generally best met by using a stripe geometry of the type shown in Figure 3.20.

The stripe geometry maximizes the emitter area-to-periphery ratio, which reduces emitter crowding while minimizing the junction capacitance. The length of the emitter is determined by current-handling requirements. The base series resistance is reduced by having two base contacts and junction depths are minimized to reduce capacitance. The buried layer, or deep collector, reduces the collector series resistance. High-power transistors are produced by paralleling a number of transistors with interleaving "fingers," as shown in Figure 3.21. This preserves the frequency response of the stripe geometry while increasing the total current-handling capability.

3.1.8 Bipolar Current-Mode Broadband Circuits

Recently there has been strong interest in applying so-called current-mode techniques to electronic circuit design. Considering the signal operating parameter as a current and driving into low-impedance nodes has allowed the development of a wealth of circuits with broadband properties. Many of the following circuit and system concepts date back several years; it is progress in integrated circuit technology that has given a renewed impetus to "practical" current-mode techniques.

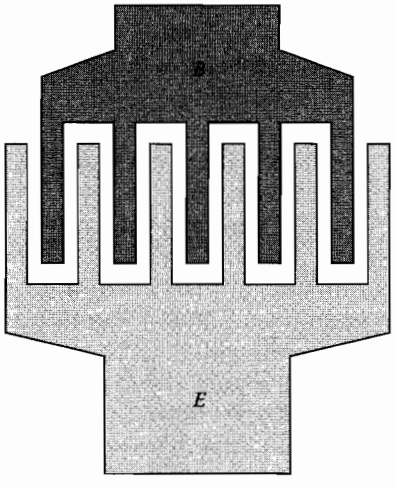


FIGURE 3.21 Transistor layout with interleaving fingers.

The NPN bipolar transistor, for example, is used predominantly in analog IC design because electron mobility is greater than hole mobility in silicon. This means that monolithic structures are typically built on P-type substrates, because vertical NPN transistors are then relatively easy to construct and to isolate from each other by reverse biasing the substrate.

Fabricating a complementary PNP device on a P-type substrate is less readily accomplished. An N type substrate must be created locally and the PNP device placed in this region. Early bipolar processes created PNP devices as lateral transistors and engineers dealt with their inherently poor, low-frequency characteristics by keeping the PNP transistors out of the signal path whenever possible.

However, high-speed analog signal-processing demands symmetrical silicon processes with fully complementary BJTs.

Newer, advanced processes have dielectrically isolated transistors rather than reversed-biased pn junction isolation. These processes are able to create separate transistors, each situated in a local semiconductor region. Then, both PNP and NPN devices are vertical and their performance characteristics are much more closely matched.

Dielectric isolation processes have revolutionized high-speed analog circuit design and have been key in making high-performance current-conveyor and current-feedback op-amp architectures practical. In the following sections, we will briefly review the development of the current-conveyor and current-feedback op-amp.

3.1.8.1 Current Conveyor

The current conveyor is a versatile broadband analog amplifier that is intended to be used with other circuit components to implement many analog signal-processing functions. It is an analog circuit building block in much the same way as a voltage op-amp, but it presents an alternative method of implementing analog systems that traditionally have been based on voltage op-amps. This alternative approach leads to new methods of implementing analog transfer functions, and in many cases the conveyor-based implementation offers improved performance when compared to the voltage op-amp-based implementation in terms of accuracy, bandwidth, and convenience. Circuits based on voltage op-amp are generally easy to design since the behavior of a voltage op-amp can be approximated by a few simple design rules. This is also true for current conveyors, and once the appropriate design rules are understood, the application engineer is able to design conveyor-based circuits just as easily.

The first-generation current conveyor (CCI) was proposed by Smith and Sedra in 1968 [1] and the more versatile second-generation current conveyor (CCII) was introduced by the same two authors in 1970 [2], as an extension of the CCI. The CCII, is without doubt the more valuable and adaptable building block of the two, and we will concentrate mostly on this device. Figure 3.22a shows the voltage–current describing matrix for the CCII, while Figure 3.22b shows the schematic normally used for the CCII with the power supply connections omitted.

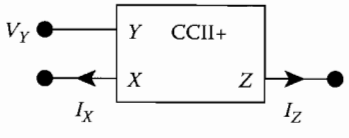
The voltage at the low-impedance input node X follows that at the high-impedance input node Y, while the input current at node X is mirrored or "conveyed" to the high-impedance output node Z. The $\pm$ sign indicates the polarity of the output current with respect to the input current; by convention, a positive sign indicates that both the input and output currents simultaneously flow into or out of the device, thus Figure 3.22b illustrates a CCII+. For the CCI, the input current at node X was reflected to input Y, that is the two inputs had equal currents. In the case of the second-generation conveyor input, Y draws no current, and this second generation, or CCII formulation, has proved to be much more adaptable and versatile than its first-generation predecessor. Because of the combined voltage and current following properties, CCIIs may be used to synthesize a number of analog circuit functions that are not so easily or accurately realizable using voltage op-amps.

Some of these application areas are shown in Figure 3.23. As current-conveyors become more readily available and circuits designers become more familiar with the versatility of this device, it is certain that further ingenious uses will be devised.

The ideal transistor and the current-conveyor. So far a transistor-level realization of the CCII has not been discussed. The current–voltage transfer relationship for the CCII+ is given by

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

(a)



(b)

FIGURE 3.22 The CCII current conveyor. (a) I–V describing matrix. (b) Schematic.

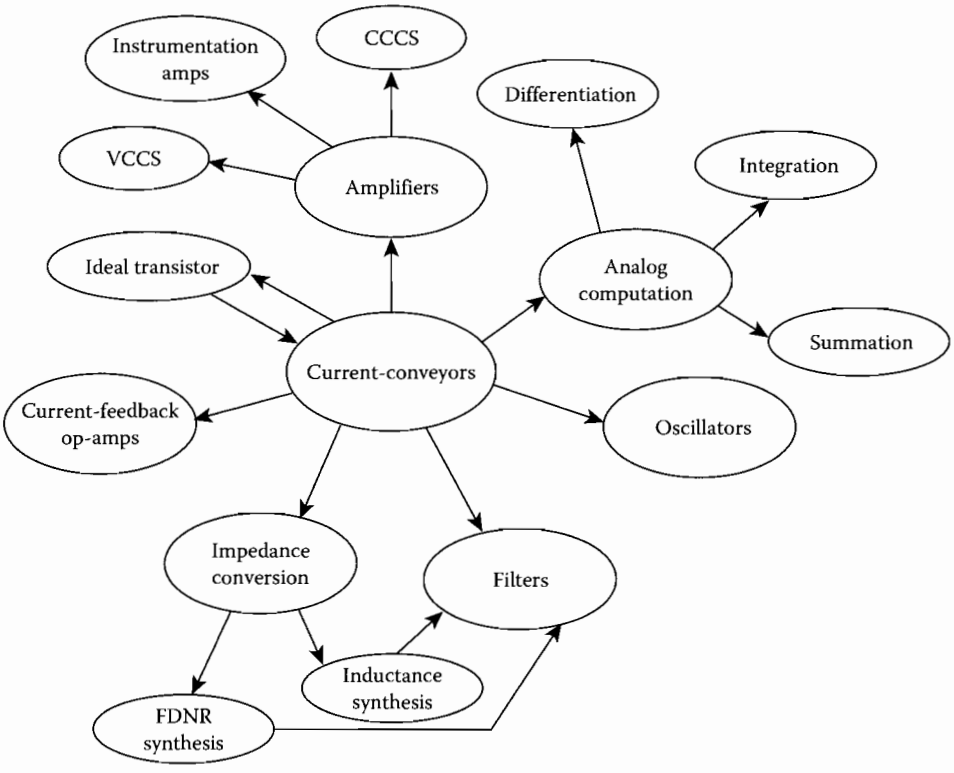


FIGURE 3.23 Current-conveyor applications.

$$V_X = V_Y, \quad I_Y = 0, \quad \text{and} \quad I_Z = I_X \tag{3.23}$$

These equations show that a simple voltage-following action exists between input node Y and output node X, and that there is a simple current-following action between input node X and output node Z. Also, these characteristic equations tell us that the impedance relationship for the ideal current conveyor is

$$Z_{\text{in}Y} = \infty, \quad Z_X = 0, \quad \text{and} \quad Z_{\text{out}Z} = \infty \tag{3.24}$$

Figure 3.24 shows a schematic representation of a CCII—built with a single BJT and on reflection it is clear that the current conveyor is effectively an ideal transistor, with infinite β and infinite g_m.

Driving into the base of a BJT gives almost unity voltage gain from input base to output emitter, with high input impedance and low-output impedance, and driving into the emitter of a BJT gives almost unity current gain from emitter input to collector output, with low input impedance and high output impedance. Drawing the comparison further, the high-input-impedance Y node corresponds to the base (or gate) of a transistor, the low-input-impedance X node corresponds to the emitter (or source) of a transistor, and the high-output-impedance Z node corresponds to the collector (or drain) of a transistor. Clearly, one transistor cannot function alone as a complete current conveyor since an unbiased single transistor at best can only handle unipolar signals and the high-accuracy unity voltage and unity current gain required for a high-performance current conveyor cannot be obtained. However, the generic relationship between the current conveyor and an ideal transistor is valid, and it provides valuable insight into the development and operation of monolithic current conveyors described in the next section.

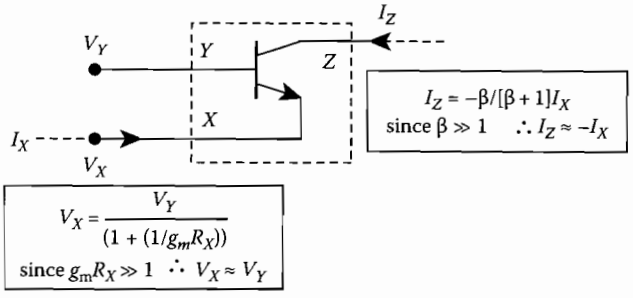


FIGURE 3.24 Single BJT CCII–.

Supply-current sensing. Many of the current-conveyor theories and applications have been tested out in practice using "breadboard" conveyor circuits, due to the lack of availability of a commercial device. Some researchers have built current conveyors from matched transistor arrays, but the most common way of implementing a fairly high-performance current conveyor has been based on the use of supply-current sensing on a voltage op-amp [3,4], as shown in Figure 3.25. The high-resistance op-amp input provides the current-conveyor Y node, while the action of negative feedback provides the low-resistance X node. Current-mirrors in the op-amp supply leads copy the current at node X to node Z.

Using this type of architecture, several interesting features soon became apparent. Consider the two examples shown in Figure 3.26. In Figure 3.26b, R_s represents the output resistance of the current source. The open-loop gain of an op-amp can generally be written

$$\frac{V_{out}}{V_{in}} = \frac{A_o}{1 + j(f/f_o)} \tag{3.25}$$

where A_o is the open-loop direct current (dc) gain magnitude and ∂_o is the open-loop -3 dB bandwidth. Since $A_o \gg 1$, the transfer function of the voltage follower of Figure 3.26a can be written as

$$\frac{V_{out}}{V_{in}} \approx \frac{1}{1 + j(f/GB)} \tag{3.26}$$

where $GB = A_o \partial_o$. From Equation 3.26, the -3 dB bandwidth of the closed-loop voltage follower is equal to the open-loop gain-bandwidth product or GB of the op-amp. If the op-amp is configured instead to give a closed-loop voltage gain K, it is well known that the closed-loop bandwidth correspondingly reduces by the factor K.

The transfer function for the current-follower circuit of Figure 3.26b, as shown in Ref. [4], is given by

$$\frac{I_{out}}{I_{in}} \approx \lambda \frac{1 + j(f/GB)}{1 + j(f/kGB)} \tag{3.27}$$

where λ is the current transfer ratio of the current mirrors and $k = (R_s + r_o/A_o)/(R_s + r_o)$, and r_o represents the output resistance of the op-amp. Since $A_o \gg R_s \gg r_o$, then $K \approx 1$, and the pole and zero in Equation 3.27 almost

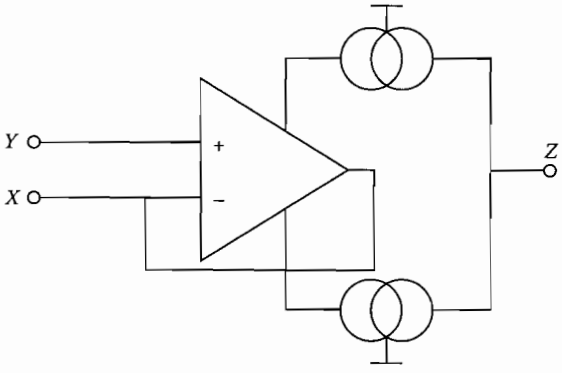


FIGURE 3.25 Supply-current sensing on a voltage op-amp.

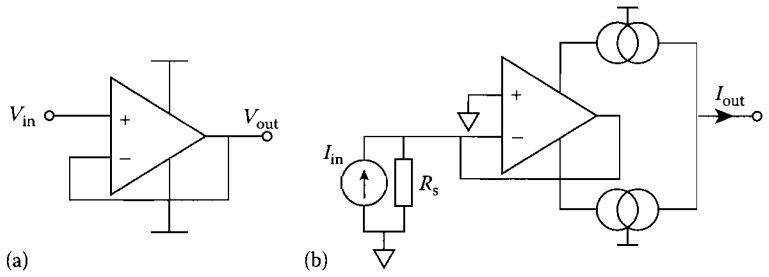


FIGURE 3.26 (a) Voltage follower. (b) Current follower.

cancel. The current-follower circuit thus operates well above the gain-bandwidth product *GB* of the op-amp, and the −3 dB frequency of this circuit will be determined by higher frequency parasitic poles within the current mirrors.

This "extra" bandwidth is achieved because the op-amp is being used with input and output nodes held at virtual ground. The above example is generic in the development of many of the circuits that follow. It demonstrates that reconfiguring a circuit topology to operate with current signals can often result in a superior frequency performance.

First-generation current conveyors. Smith and Sedra's original paper presenting the first-generation CCI current conveyor showed a transistor-level implementation based on discrete devices, shown in Figure 3.27. Assuming that transistors Q_3–Q_5 and resistors R_1–R_3 are matched, then to first order the currents through these matched components will be equal. Transistors Q_1 and Q_2 are thus forced to have equal currents, and equal V_{be}s. Input nodes *X* and *Y* therefore track each other in both voltage and current. In practice, there will be slight differences in the collector currents in the different transistors, due to the finite β of the devices. These differences can be reduced, for example, by using more elaborate current mirrors. The polarity of the output current at node *Z* can be inverted easily by using an additional mirror stage, and the entire circuit can also be inverted by replacing NPN transistors with PNPs, and vice versa. Connecting two complementary current conveyors, as shown in Figure 3.28, results in a class *AB* circuit capable of bipolar operation. Note that in practice this circuit may require additional components to guarantee start-up.

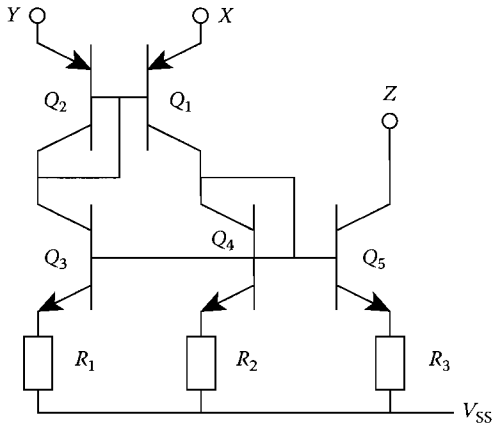


FIGURE 3.27 First-generation current conveyor.

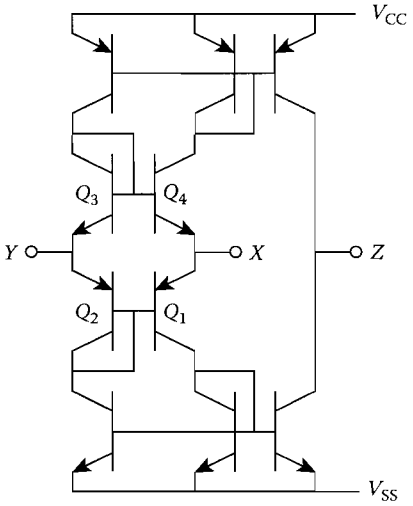


FIGURE 3.28 Class *AB* current conveyor.

An integrated current conveyor based on the architecture shown in Figure 3.27 is commercially available as the PA630 [5], and the basic topology of this device is shown in Figure 3.29. An NPN Wilson mirror (Q_1–Q_3) and a PNP Wilson mirror (Q_4–Q_6) are used to provide the current and voltage following properties between inputs X and Y, similar to the circuit of Figure 3.27. Taking a second output from the PNP current mirror to provide the Z output would destroy the base-current compensation scheme of the Wilson mirror. Therefore, a second NPN Wilson mirror (Q_7–Q_9) is used to perform a current-splitting action and so the combined emitter current of Q_7 and Q_8 is divided in two, with one half being shunted via Q_9 to the supply rail, and the other half driving an output PNP Wilson mirror (Q_{10}–Q_{12}). This results in an output current at node Z that to first order is virtually equal to that at the X and Y inputs. Q_{13} is included to ensure that the device always starts up when turned on. The complete architecture of the PA630 CCI also includes frequency compensation to ensure stability, and modified output current mirrors that use the "wasted" collector current of Q_9 to effectively double the output resistance at node Z. A full description of the architecture and operation of this device can be found in Ref. [6].

The current-conveyor architecture shown in Figure 3.29 includes both NPN and PNP transistors in the signal path, and thus the bandwidth and current-handling capability of this device will be poor if only lateral PNPs are available. The development of complementary bipolar processes, with vertical PNP as well as NPN transistors, has made possible the implementation of high-performance integrated circuit current conveyors.

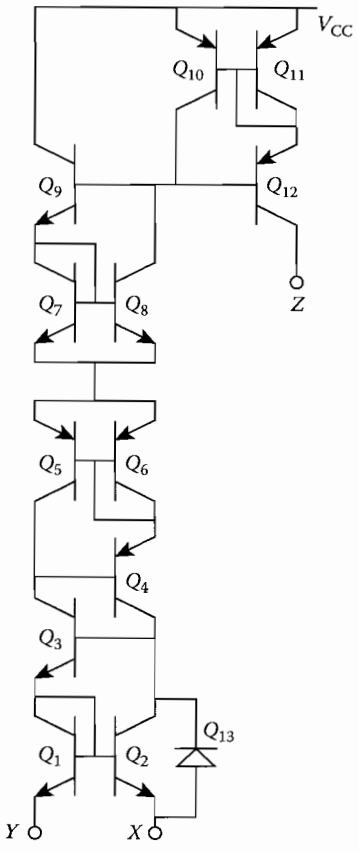


FIGURE 3.29 Simplified PA630 current conveyor.

Second-generation current conveyors. A CCII can also be simply implemented on a complementary bipolar process, by replacing the diode at the CCI Y input with a transistor, and taking the input from the high resistance base terminal, as shown in Figure 3.30a. This can be extended to a class *AB* version, as shown in Figure 3.30b. Referring to Figure 3.30b, transistors Q_1–Q_4 act as a voltage buffer that transfers the voltage at node Y to node X. The current source and sink ($I_{B1} = I_{B2} = I_B$) provide the quiescent bias current for these input transistors. Any input current (I_x) at node X is split between Q_2 and Q_3, and is copied by current mirrors CM_1 and CM_2 to the output node Z. This CCII architecture forms the basis of the commercially available CCII01 current conveyor [7]. As we shall see later, it is also used as the basic input stage of the current-feedback op-amp, which has emerged as a high-speed alternative to the more conventional voltage op-amp [8].

The simple CCII architecture of Figure 3.30b will clearly exhibit a quiescent voltage offset between nodes X and Y due to the mismatch between the V_{be}s of the NPN and PNP transistors Q_1/Q_2 and Q_3/Q_4, as

$$\begin{aligned} V_Y - V_X &= V_{BE}(p) - V_{BE}(n) \\ &= V_T \ln\left(I_{sp}/I_{sn}\right) \end{aligned} \tag{3.28}$$

where I_{sp} and I_{sn} are the reverse saturation currents of the PNP and NPN transistors, respectively, and V_T is the thermal voltage. This process-dependent voltage offset can be reduced by including additional matching diodes in the input stage, as shown in Figure 3.31. Referring to this diagram,

$$\begin{aligned} V_Y - V_X &= V_{BE}(Q_1) + V_{D_2} - V_{BE}(Q_2) - V_{D_1} \\ V_Y - V_X &= [V_{BE}(Q_1) - V_{D_1}] - [V_{BE}(Q_2) - V_{D_2}] \end{aligned} \tag{3.29}$$

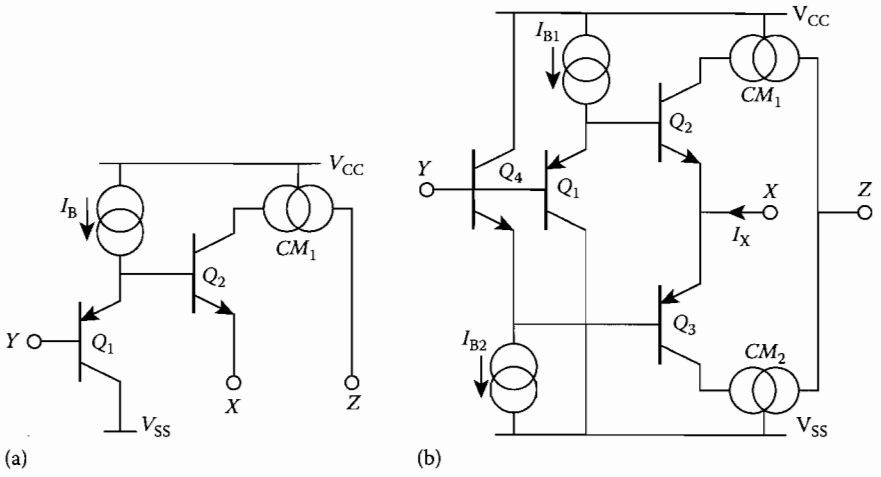


FIGURE 3.30 (a) Class *A* CCII. (b) Class *AB* CCII.

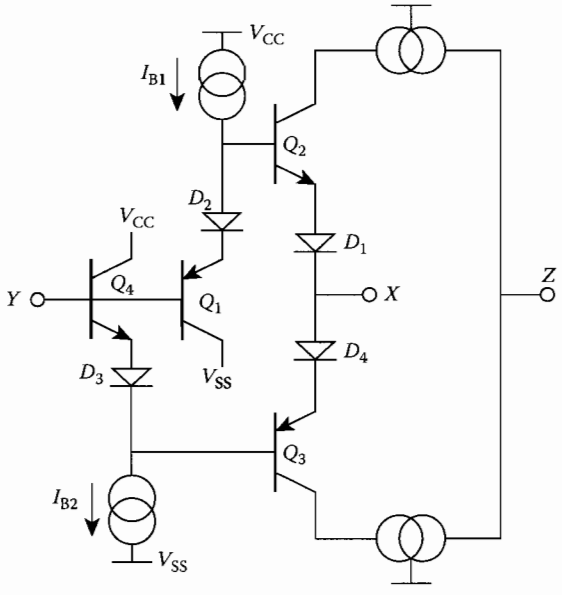


FIGURE 3.31 CCII with input matching diodes.

Inclusion of these diodes clearly reduces the quiescent input voltage offset, provided that D_1 is matched to Q_1, D_2 is matched to Q_2, etc. However, the addition of diodes D_1 and D_2 has several disadvantages. First, the input voltage dynamic range of the circuit will be reduced by the forward voltage across the additional diode. Second, the small-signal input resistance seen looking into node X will be double that for the basic architecture given in Figure 3.30b. This nonzero input resistance at node X (R_x) will compromise the performance of the current conveyor, especially in applications where a nonzero input voltage is applied at node Y. The effect of the small-signal input resistance R_x is to produce a signal-dependent voltage offset V_d between nodes X and Y, where

$$V_d = R_x I_x \tag{3.30}$$

Since the value of R_x is determined by the small-signal resistance $(r_{e2} + r_{d2})$ in parallel with $(r_{e3} + r_{d3})$, its value could be reduced by increasing the value of the quiescent bias current I_B. However, an increase in bias current will lead to an increase in the total power consumption, as well as a possible increase in offsets, and so is certainly not an ideal solution. Further techniques for CCII implementation are discussed in Ref. [14].

The previous conveyor is typical of commercial conveyor architectures [7], which are generally built on a high-speed dielectric isolation (fully complementary) bipolar process. Such devices feature an equivalent slew rate of some 2000 V/μs and a bandwidth of around 100 MHz.

Until high-performance current conveyors are widely available, these devices will continue to be used in research laboratories rather than in the applications arena. Process technologies and design techniques

have now advanced to the stage where the implementation of an integrated current conveyor is both desirable and viable, and a whole host of applications are waiting for its arrival.

3.1.8.2 Current-Feedback Operations Amplifier

In this section, the design and development of a high-gain wide-bandwidth transimpedance or current-feedback operational amplifier is considered. The design of conventional operational amplifiers has remained relatively unchanged since the introduction of the commercial operational amplifier in 1965. Recently, a new amplifier architecture, called a current-feedback operational amplifier, has been introduced. This amplifier architecture is basically a transimpedance amplifier, or a current-controlled voltage source, while the classical voltage-feedback operational amplifier is a voltage-controlled voltage source.

The current-feedback operational amplifier has two major advantages, compared to its voltage-feedback counterpart. First, the closed-loop bandwidth of the current-feedback amplifier is larger than that of classical voltage-feedback design for comparable open-loop voltage gain. Second, the current-feedback operational amplifier is able to provide a constant closed-loop bandwidth for closed-loop voltage gains up to about 10. A further advantage of the current-feedback architecture is an almost unlimited slew rate due to the class-*AB* input drive, which does not limit the amount of current available to charge up the compensation capacitor as is the case in the conventional voltage-feedback op-amp. This high-speed performance of the current-feedback operational amplifier is extremely useful for analog signal-processing applications within video and telecommunication systems.

The generic relationship between the CCII+ and the current-feedback op-amp is extremely close and several of the features offered by the CCII are also present in the current-feedback op-amp. The basic structure of the current-feedback op-amp is essentially that of a CCII+ with the Z node connected directly to an output voltage follower, as shown in Figure 3.32. Any current flowing into the low-impedance inverting input is conveyed to the gain node (Z_T), and the resulting voltage is buffered to the output. Z_T is thus the open-loop transimpedance gain of the current-feedback op-amp, which in practice is equal to the parallel combination of the CCII+ output impedance, the voltage buffer input impedance and any additional compensation capacitance at the gain node. Generally, in current-feedback op-amps, the gain node is not connected to an external pin, and so the Z node of the CCII+ cannot be accessed.

Current-feedback op-amp architecture. In the following sections, we review the basic theory and design of the current-feedback op-amp and will identify the important features and mechanisms that result in broadband performance. We will begin by reviewing the voltage-feedback op-amp and comparing it with the current-feedback op-amp in order to see the differences clearly.

A schematic of the classical voltage-feedback op-amp comprising a long-tail pair input stage is shown in Figure 3.33a, which contrasts a typical current-feedback architecture, which is shown in Figure 3.33b. In both circuits, current mirrors are represented by two interlocking circles with an arrow denoting the input side of the mirror.

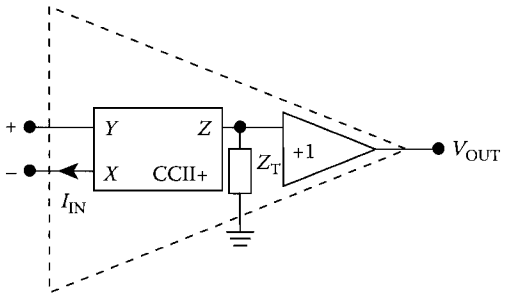


FIGURE 3.32 Current-feedback op-amp structure.

The current-feedback op-amp of Figure 3.33b shows that the noniverting input is a high-impedance input that is buffered to a low-impedance inverting terminal via a class *AB* complementary common-collector stage (Q_1, Q_2, D_1, D_2). Note that this classical input buffer architecture is used here for simplicity. In practice, a higher performance topology such as that described in Figure 3.31 would more likely be employed. The noninverting input is a voltage input; this voltage is then buffered to the inverting low-impedance current input to which feedback is applied. In contrast, both the noninverting and

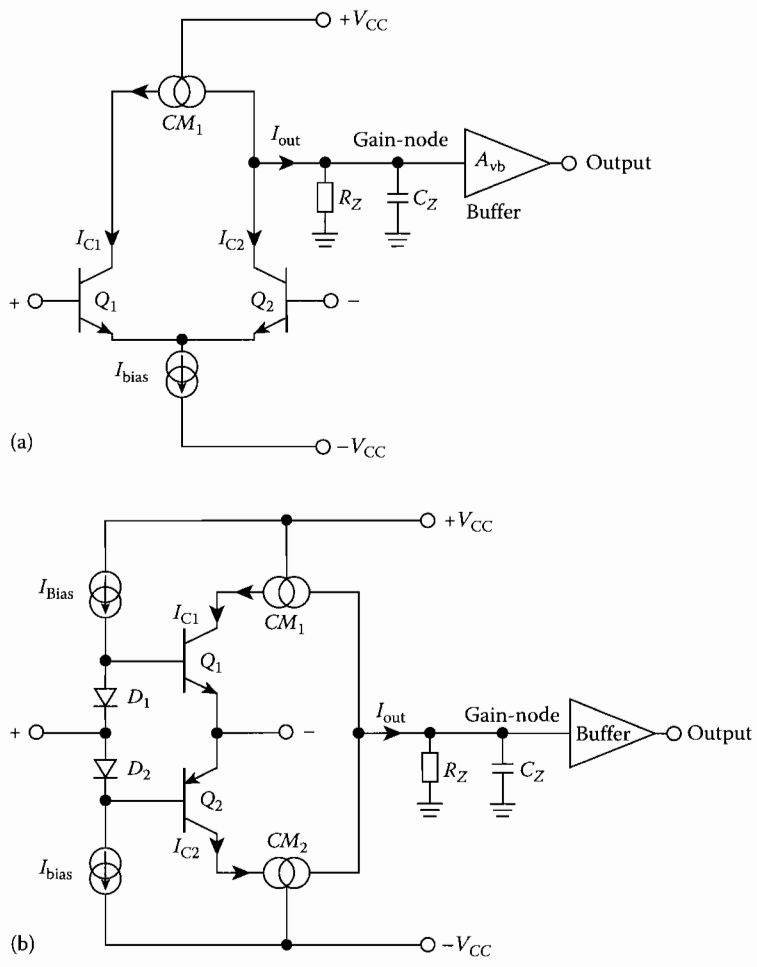


FIGURE 3.33 (a) Simplified classic voltage-feedback op-amp architecture. (b) Typical current-feedback op-amp architecture.

inverting input of the voltage-feedback op-amp are high-impedance voltage inputs at the bases of transistors Q_1 and Q_2.

In both architectures, the collector currents of Q_1 and Q_2 are transferred by the current mirror to a high-impedance node represented by resistance R_Z and capacitance C_Z. This voltage is then transferred to the output by voltage buffers that have a voltage gain A_{vb}, providing the necessary low-output impedance for current driving. In the case of the current-feedback op-amp, the output buffer is usually the same topology as the input buffer stage shown in the Figure 3.33b, but with slightly higher output current bias levels and larger output devices to provide an adequate output drive capability. Ideally, the bias currents I_{CQ1} and I_{CQ2} will be canceled at the gain node giving zero offset current.

Differential-mode operation of the current-feedback op-amp. A schematic diagram of the current-feedback op-amp with a differential input voltage applied at the noninverting and inverting input is shown in Figure 3.34.

The positive input voltage is applied to the base of transistor Q_1 (NPN) via D_1, and the negative input voltage is applied to the emitter of Q_1, causing the V_{BE} of Q_1 to increase and the V_{BE} of Q_2 to

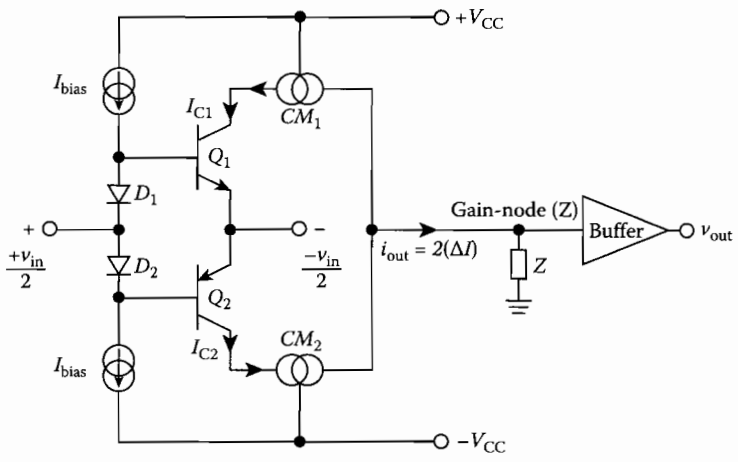


FIGURE 3.34 Current-feedback op-amp with differential input voltage applied.

reduce. I_{C1} will therefore increase by an amount ΔI and so I_{C2} will decrease by the same amount $-\Delta I$. A net current of $2\Delta I$ is therefore sourced out of the high-impedance node (Z) giving rise to a positive voltage ($2\Delta IZ$). This voltage is then buffered to the output.

With negative feedback applied around the current-feedback op-amp, the low-impedance inverting input will sense the current "feedback" from the output via the feedback network. This feedback current flowing into the inverting input is given by

$$i_{in-} = I_{C2} - I_{C1} \tag{3.31}$$

The difference between the collector current I_{C1} and I_{C2}, i_{in-}, will thus be driven into gain node Z, giving rise to the output voltage

$$V_{out} = Zi_{in-} \tag{3.32}$$

It is clear that the output voltage is dependent on the current that flows into the inverting input, hence the amplifier has a high open-loop transimpedance gain Z.

Closed-loop noninverting operation of the current-feedback op-amp. A schematic diagram of the current-feedback op-amp connected with negative feedback as a noninverting amplifier is shown in Figure 3.35. For a positive input voltage v_{in}, the output voltage v_{out} will swing in the positive direction and the inverting input current i_{in-} will flow out:

$$i_{in-} = \frac{v_{in-}}{R_1} - \frac{(v_{out} - v_{in-})}{R_2} \tag{3.33}$$

The input stage is simply a voltage follower and so ideally, $v_{in+} = v_{in-} = v_{in}$. Because $v_{out} = Zi_{in-}$, then substituting for v_{in-} and i_{in-} in Equation 3.33 yields

$$\frac{v_{out}}{Z} = \frac{v_{in}}{R_1} - \frac{(v_{out} - v_{in})}{R_2} \tag{3.34}$$

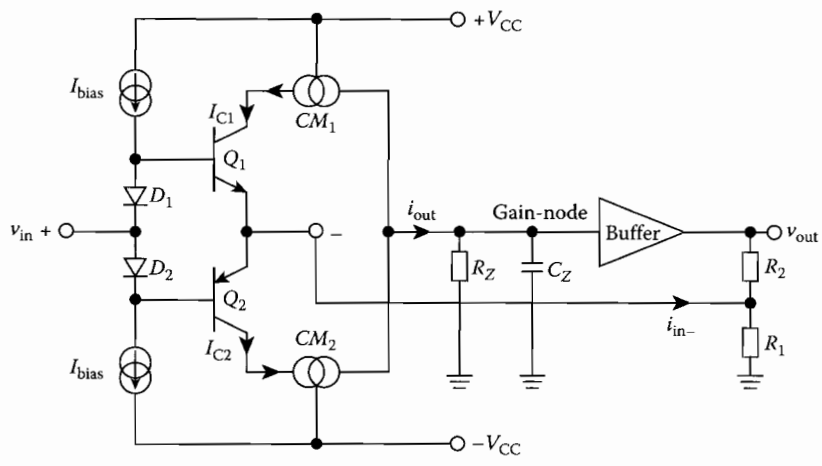


FIGURE 3.35 Noninverting current-feedback op-amp.

rearranging for v_{out}/v_{in}

$$v_{out}\left(\frac{1}{R_2}+\frac{1}{Z}\right)=v_{in}\left(\frac{1}{R_1}+\frac{1}{R_2}\right) \tag{3.35}$$

$$\frac{v_{out}}{v_{in}}=\left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+(R_2/Z)}\right) \tag{3.36}$$

This result shows that the closed-loop noninverting gain of the current-feedback op-amp is similar to that of a classical voltage-feedback op-amp. From Equation 3.36, the open-loop transimpedance gain Z must be as large as possible to give good closed-loop gain accuracy. Since v_{out}/Z represents the error current i_{in-}, then maximizing the Z term will minimize the inverting error current. Note that at this stage it is only the R_2 term in the denominator of the second term in Equation 3.36 that sets the bandwidth of the amplifier; the gain-setting resistor R_1 has no effect on the closed-loop bandwidth.

Closed-loop inverting operation of current-feedback op-amp. A current-feedback op-amp connected as an inverting amplifier is shown in Figure 3.36. The low-impedance inverting input samples the input current and drives the output until the voltage at its terminal is at a virtual ground because of negative feedback. Ideally the closed-loop gain is given by

$$A_{CL}=-\frac{R_2}{R_1} \tag{3.37}$$

From Figure 3.36, application of Kirchhoff's current law to the current i_1, i_{in-}, and i_2 gives

$$i_{in-}+i_2=i_1$$

$$i_{in-}-\frac{v_{out}}{R_2}=\frac{v_{in}}{R_1}$$

because $v_{out}/Z=-i_{in-}$, then

$$-\frac{v_{out}}{Z}-\frac{v_{out}}{R_2}=\frac{v_{in}}{R_1}$$

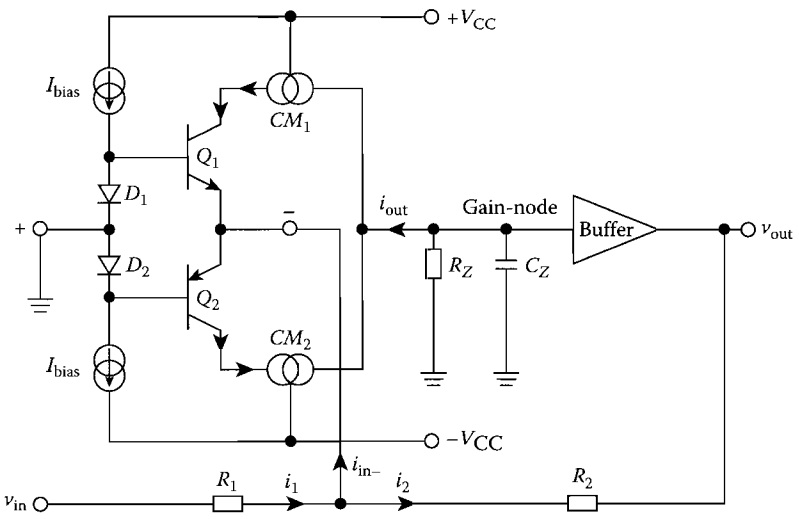


FIGURE 3.36 Inverting current-feedback op-amp amplifier.

which can be rearranged as

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}\left(\frac{1}{1+\frac{R_2}{Z}}\right) \tag{3.38}$$

Again, the high-Z term is required to provide good closed-loop gain accuracy.

More detailed analysis of the current-feedback op-amp. A simplified macromodel of the current-feedback architecture configured as a noninverting amplifier is shown in Figure 3.37. The input stage is represented by a semi-ideal voltage buffer to the inverting input. The output resistance of the input stage buffer R_{inv} is included since it has a significant effect on the bandwidth of the amplifier, as will be shown later. The current that flows out from the inverting terminal i_3 is transferred to the gain node, which is represented by R_Z and C_Z, via a current mirror that has a current gain K. The voltage at the gain node is transferred to the output in the usual way by a voltage buffer, with voltage gain A_{vb}. The net transfer function is given by

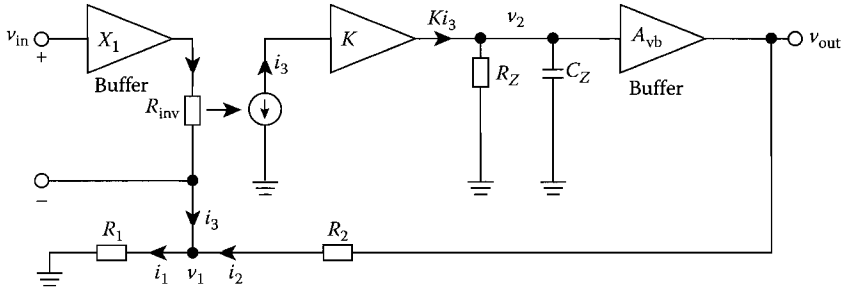


FIGURE 3.37 Inverting amplifier with current-feedback op-amp macromodel.

$$\frac{v_{out}}{v_{in}} = \frac{1 + \dfrac{R_2}{R_1}}{1 + j\omega C_Z \left[\dfrac{R_{inv}\left(1 + \dfrac{R_2}{R_1}\right) + R_2}{A_{vb}K} \right]} \tag{3.39}$$

Hence, the pole frequency is also given by

$$f_{-3dB} = \frac{A_{vb}K}{2\pi C_Z \left[R_{inv}\left(1 + \dfrac{R_2}{R_1}\right) + R_2 \right]} \tag{3.40}$$

(A full derivation of this transfer function is given in Appendix A.)

To compare this result to the classical voltage-mode op-amp architecture, a simplified schematic diagram of the voltage-feedback op-amp configured as a noninverting amplifier is shown in Figure 3.38.

Again from a full analysis, given in Appendix B, the transfer function obtained is

$$\frac{v_{out}}{v_{in}} = \frac{1 + \dfrac{R_2}{R_1}}{1 + j\omega \left[\dfrac{R_z C_Z}{1 + \dfrac{g_m A_{vb} R_Z}{\left(1 + \dfrac{R_2}{R_1}\right)}} \right]} \tag{3.41}$$

The pole frequency is given by

$$f_{-3dB} = \frac{1 + \dfrac{g_m A_{vb} R_Z}{\left(1 + \dfrac{R_2}{R_1}\right)}}{2\pi R_Z C_Z} \tag{3.42}$$

Pole frequency comparison. If one compares the closed-loop pole frequency Equations 3.40 and 3.42 for the current-feedback and voltage-feedback op-amp, respectively, it is clear that the bandwidth of the voltage-feedback op-amp is dependent on the closed-loop gain $(1 + R_2/R_1)$ resulting in the well-known constant gain-bandwidth product $f_{max} = (A_v)_{CL} f_T$. This means that an increase in the closed-loop gain results in a decrease in the bandwidth by the same factor as illustrated in Figure 3.39. In contrast, the pole

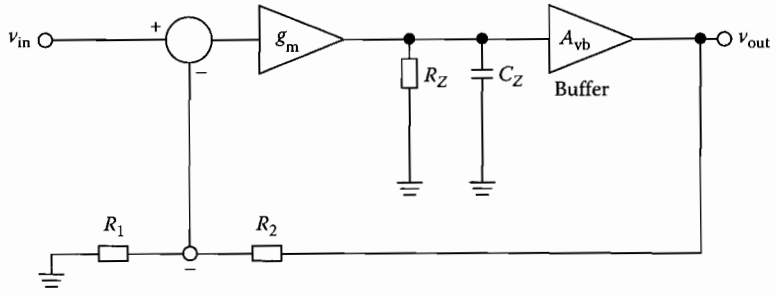


FIGURE 3.38 Noninverting amplifier with voltage-feedback op-amp macromodel.

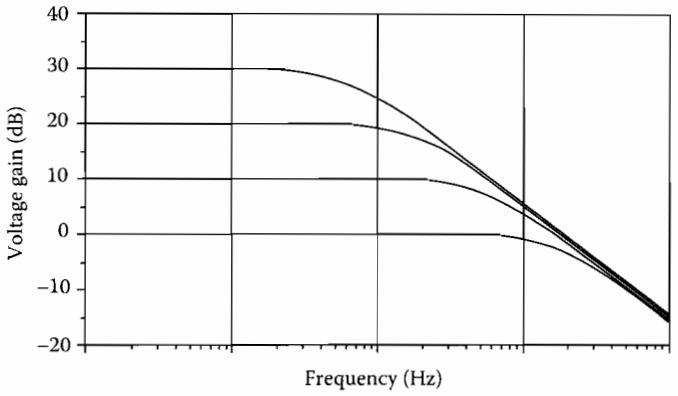


FIGURE 3.39 Frequency response of voltage-feedback op-amp amplifier for various closed-loop gains.

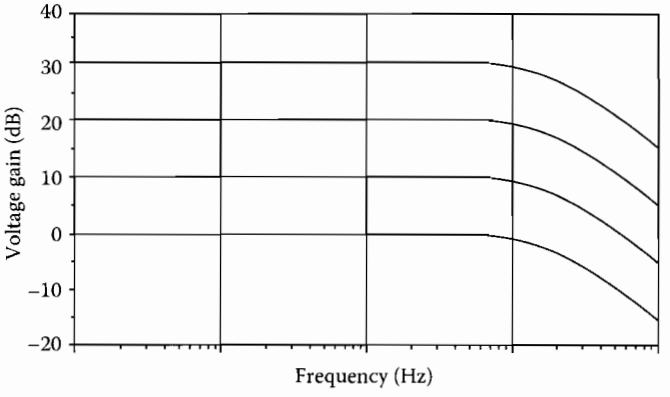


FIGURE 3.40 Frequency response of current-feedback op-amp amplifier for various closed-loop gains.

frequency of the current-feedback op-amp is directly dependent on R_2 and can be set almost independently of the closed-loop gain. Thus, the closed-loop bandwidth is almost independent of closed-loop gain as shown in Figure 3.40, assuming that R_{inv} is close to zero. Intuitively, this is the case since the feedback error current that is set by the feedback resistor R_2 is the current available to charge up the compensation capacitor. However, if one considers Equation 3.40 in some detail it can be seen that for high closed-loop gains and a nonzero R_{inv}, then the R_{inv} term starts to dictate and so the bandwidth will become more dependent on the closed-loop gain.

Slow rate of the current-feedback op-amp. As mentioned earlier, one other advantage of the current-feedback op-amp over the classical voltage-feedback op-amp is the high slew rate performance. For the classical long-tail, or emitter-coupled pair input stage shown in Figure 3.41, the maximum current available to charge up the compensation capacitor C_Z at the gain node is I_{bias}, and this occurs when Q_1 or Q_2 is driven fully on. The resulting transconductance plot shown in Figure 3.42 limits the slew rate of the amplifier.

In contrast, the slew rate of the current-feedback op-amp is virtually infinite, as can be seen from the input stage schematic shown in Figure 3.43. Referring to Figure 3.43, a change in the input voltage ΔV_{in} at $V(+)$ will be copied by the input buffer to $V(-)$. When connected as noninverting amplifier, the current through R_1 will change by $\Delta V_{in}/R_1$, while the current through R_2 will change by $\Delta V_{in}/R_2$, since

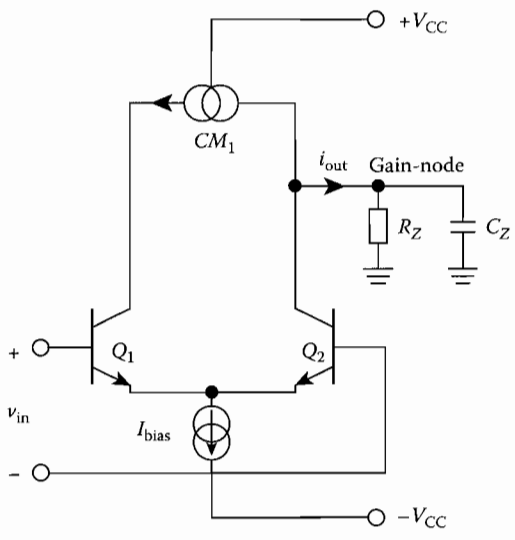


FIGURE 3.41 Long-tail pair input stage.

the output voltage at this point remains stationary. The total change in current through R_1 and R_2 must be supplied by the internal input buffer, and will be $\Delta I(-) = \Delta V_{in}((R_2 + R_1)/(R_2 \times R_1))$. This large input error current causes a rapid change in the output voltage, until V_{out} is again at the value required to balance the circuit once more, and reduce $I(-)$ to zero. The larger the input voltage slew rate, the larger the change in input error current, and thus the faster the output voltage slew rate. Current-feedback op-amps theoretically have no slew-rate limit. A typical current-feedback op-amp will exhibit a slew rate of between 500 and 2000 V/μS.

An analysis of this input stage (see Appendix C) shows that the transconductance follows a sinh(x) type function, as shown in Figure 3.44. In theory, this characteristic provides nearly unlimited slew-rate capability [9]. However, in practice a maximum slew rate will be limited by the maximum current drive into the gain node, which depends on the power dissipation of the circuit, the ability of power supply to deliver sufficient current, and the current-handling capability of the current mirrors.

Wideband and high-gain current-feedback op-amp. Previously, we have shown that the bandwidth of the current-feedback op-amp is almost independent of the closed-loop gain setting. Therefore, the closed-loop gain-bandwidth GB increases linearly with the closed-loop gain. However, the bandwidth of the practical current-feedback op-amp starts decreasing with high gain as a result of the finite inverting-input impedance [10], as shown by Equation 3.40. This is because for high gain, $R_{inv}(1 + R_2/R_1) > R_2$, and so the $R_{inv}(1 + R_2/R_1)$ term dominates the expression for closed-loop bandwidth, resulting in a direct conflict between gain and bandwidth.

At low gains when $R_2 > R_{inv}(1 + R_2/R_1)$, the closed-loop pole frequency is determined only by the compensation capacitor and the feedback resistor R_2. Thus, the absolute value of the feedback resistor R_2 is important, unlike the case of the voltage-feedback op-amp. Usually, the manufacturer species a minimum value of R_2 that will maximize bandwidth but still ensure stability. Note that because of the

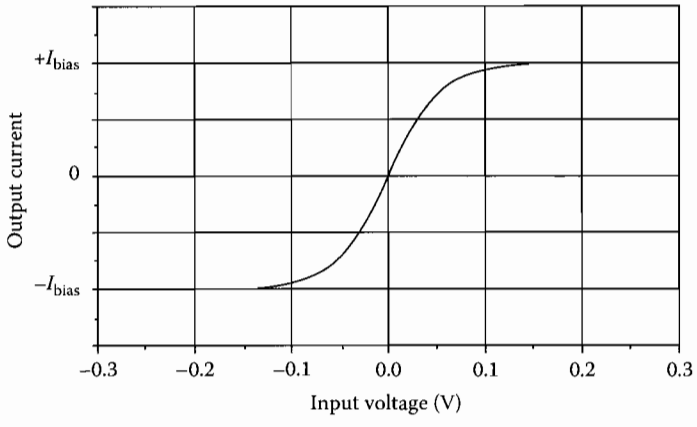


FIGURE 3.42 Long-tail pair input transconductance.

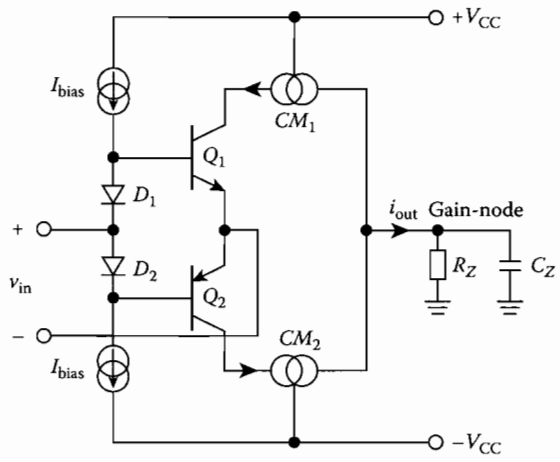


FIGURE 3.43 Current-feedback op-amp input stage.

inherent architecture a very high bandwidth can be achieved with the current-feedback design for a given value of R_2.

In practice, for gains higher than about 10, the $R_{inv}(1+R_2/R_1)$ term in Equation 3.40 becomes dominant and the amplifier moves toward constant gain-bandwidth product behavior. The *GB* can be increased by reducing R_2 [11] but this will compromise stability and/or bandwidth, or alternatively, C_Z can be reduced. The latter option is limited since the minimum value of C_Z is determined by the device parameters and layout parasitics. Two possible ways of improving the high-gain constant bandwidth capability of the current-feedback op-amp can be seen by inspection of Equation 3.40. Either the K factor, which represents current gain in the current mirrors at the Z-node can be increased from unity to increase the bandwidth as it rolls off with high gain, or the inverting input impedance of the amplifier should be reduced toward zero. In the following section we consider the design of a suitable broadband variable-gain current-mirror circuit with a possible application being to improving the maximum bandwidth capability of current-feedback op-amps.

Basic current mirror. A typical current-feedback op-amp circuit is shown in Figure 3.45. It includes a complementary common-collector input stage (Q_1–Q_4) and a similar output buffer (Q_5–Q_8), with linking cascode current mirrors setting the Z-node impedance (Q_{12}–Q_{14}, Q_9–Q_{11}). The cascoded mirror provides unity current gain. Any attempt to increase the current gain via emitter degeneration usually results in much poorer current-mirror bandwidth. Consider now the development of a suitable broadband, variable gain current mirror.

A schematic diagram of a simple Widlar current mirror and its small-signal equivalent circuit are shown in Figures 3.46 and 3.47, respectively. For simplicity, we will assume that the impedance of the diode-connected transistor Q_1 is resistive and equal to R_D. The dc transfer function of the mirror is derived in Appendix D and is given by

$$\frac{I_{out}}{I_{in}} = \frac{\beta}{\beta + 2} \tag{3.43}$$

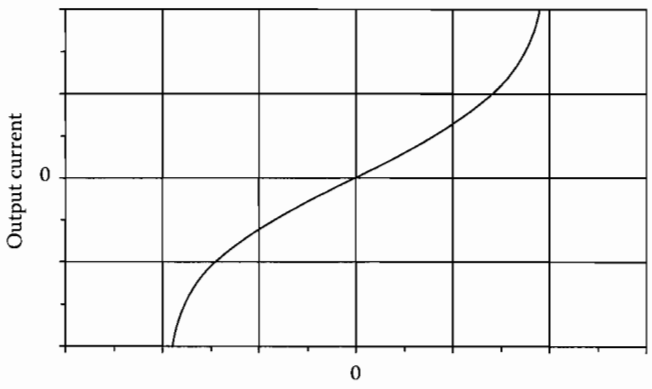


FIGURE 3.44 Input-stage transconductance of the current-feedback op-amp.

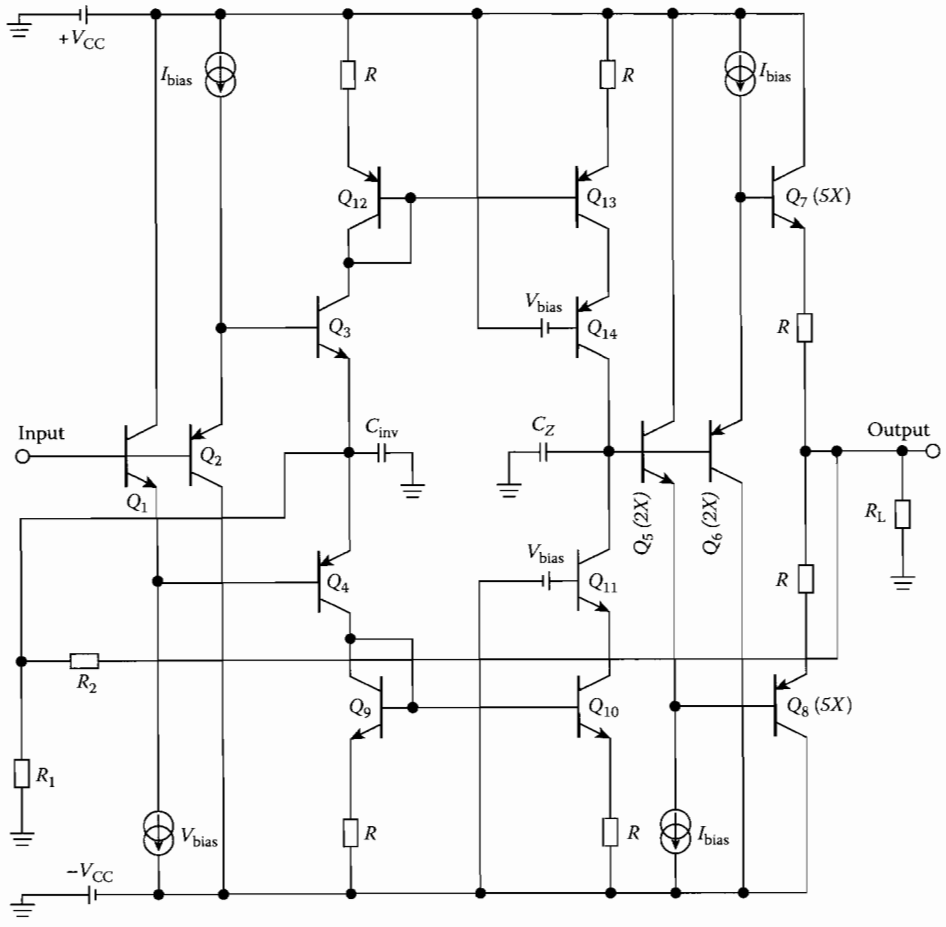


FIGURE 3.45 Transistor-level schematic of a typical current-feedback op-amp. x = Unit transistor area.

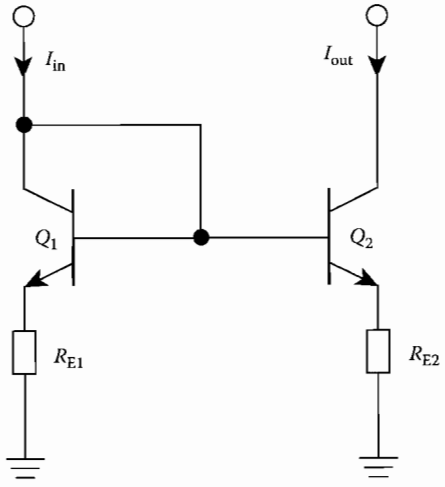


FIGURE 3.46 Simple Widlar current mirror with emitter degeneration.

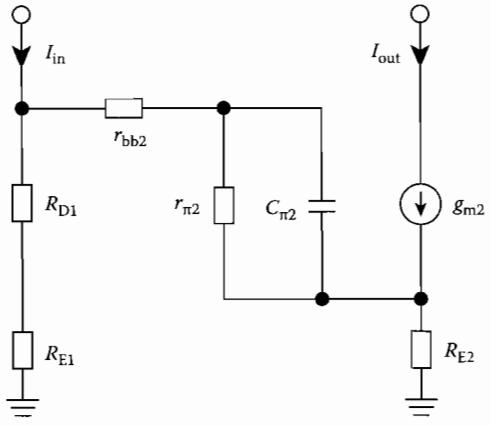


FIGURE 3.47 Small-signal equivalent circuit of Figure 3.46 current mirror.

and the −3 dB bandwidth is given by

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_\pi \left\{ \dfrac{r_{\pi 2}(r_{bb2} + R_D)}{r_\pi + r_{bb2} + R_D} \right\}} \tag{3.44}$$

In order to increase the current gain it is usual to insert an emitter-degeneration resistor R_{E1} in the emitter of Q_1. The dc transfer function, derived in the Appendix E, is then

$$I_{in} R_{E1} = V_T \ln \frac{I_{out}}{I_{in}} \tag{3.45}$$

and the ac small-signal current gain is given by

$$\frac{i_{out}}{i_{in}} = (R_{E1} + R_{D1}) g_{m2} \tag{3.46}$$

where

$$R_{D1} = \frac{I_{in}}{\frac{KT}{q}} \tag{3.47}$$

The −3-dB bandwidth now becomes

$$f_{-3dB} = \frac{1}{2\pi C_{\pi 2} \left\{ \dfrac{r_{\pi 2}(r_{bb2} + R_{D1} + R_{E1})}{r_{\pi 2} + r_{bb2} + R_{D1} + R_{E1}} \right\}} \tag{3.48}$$

It can be seen that increasing R_{E1} to increase the gain results in a reduction in the mirror bandwidth. The method of increasing the area of Q_2 to increase the current gain is not advantageous because the capacitance $C_{\pi 2}$ increases simultaneously, and so again, the bandwidth performance is compromised. We can conclude that this approach, though apparently well founded, is flawed in practice.

Improved broadband current mirror. A current mirror with current gain is shown in Figure 3.48 and the small-signal equivalent circuit is shown in Figure 3.49. In this current mirror Q_1 and Q_2 are connected as diodes in series with R_{E1}. Q_3 is connected as a voltage buffer with the bias current source I_{EQ3}. Q_4 is the output transistor with degeneration resistor R_{E4} for current gain setting. The basic idea is to introduce the CC Q_3 to buffer the output from the input and hence isolate gain setting resistor R_{E4} from the bandwidth determining capacitance of the input. The dc transfer function is given by

$$I_{in} R_{E1} - I_{out} R_{E4} + V_T \ln \frac{I_{in}^2}{I_{CQ3} I_{out}} = 0 \tag{3.49}$$

and the ac small-signal current gain is given by

$$\frac{i_{out}}{i_{in}} = \frac{(R_{E1} + R_{D1} + R_{D2}) g_{m4}}{1 + g_{m4} R_{E4}} \tag{3.50}$$

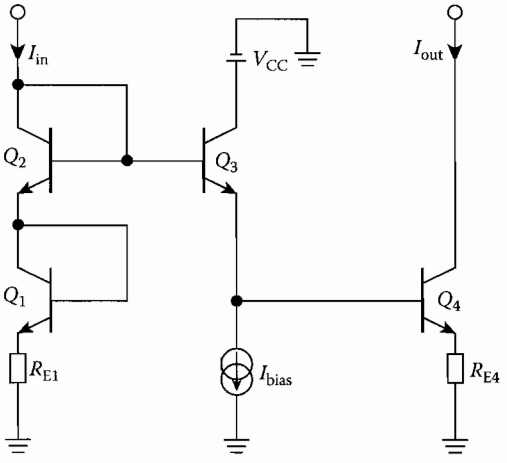


FIGURE 3.48 Improved current mirror with current gain.

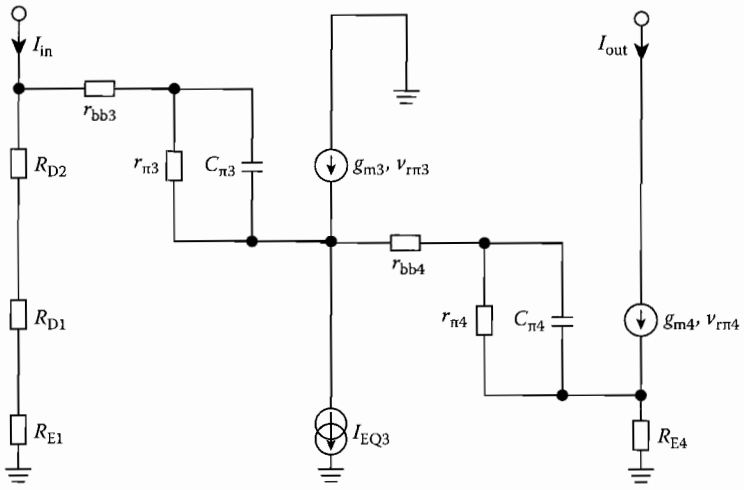


FIGURE 3.49 Equivalent circuit of improved current mirror with current gain.

and the −3 dB bandwidth now becomes

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_{\pi 4}\left(\dfrac{r_{\pi 4}R_x}{r_{\pi 4}+R_x}\right)} \tag{3.51}$$

where

$$R_x = r_{bb4} + \frac{r_{\pi 3} + r_{bb3} + R_{D1} + R_{D2} + R_{E1}}{\beta_3} \tag{3.52}$$

It can be seen clearly that the dominant pole Equation 3.51 of the current mirror with current gain is now only slightly decreased when we increase the current gain by increasing R_{E1}. However, the nondominant pole at the input node is increased, and this will marginally effect the resultant overall stability performance if employed in a current-feedback op-amp. This current mirror with current gain has been employed successfully in current-feedback op-amp design for increased gain-bandwidth capability [12].

Phase linearity. The internal signal path in a current-feedback op-amp is very linear due largely to the symmetrical architecture. Consequently, these devices have a very linear phase response. Furthermore, all the frequency components of a signal are delayed by the same amount when passing through the amplifier, and so the waveform is reproduced accurately at the output. Current-feedback op-amps typically exhibit differential phase error of around ±1° at frequencies of approximately half the bandwidth.

Choosing the value of R_2. From Equation 3.40, we can see that for a fixed value of C_z, a smaller feedback resistor R_2 will give a higher closed-loop bandwidth. It might be expected that the maximum bandwidth would be obtained with the minimum feedback resistance; that is, with $R_2 = 0$. In practice, current-feedback op-amps are generally unstable when their feedback resistance is reduced below a particular value. The reason for this is that the dominant closed-loop pole at frequency of $f \approx 1/2\pi C_z R_2$ must be significantly lower than any nondominant parasitic pole frequency within the op-amp, so that a reasonable gain and phase margin is maintained. If the value of R_2 is reduced, then this dominant pole will move upward in frequency toward the parasitic poles, reducing the gain and phase margin, and eventually leading to instability. Obviously, the "correct" value for R_2 will depend on the internal value of C_z and the location of any parasitic poles within the device. These are the sort of parameters

that are known to the manufacturer, but are generally not listed in a data sheet. Therefore, the manufacturer of a particular device will generally recommend a value of R_2 that guarantees stability, while maintaining a reasonably wide bandwidth. Reducing R_2 below this recommended or optimum value will tend to lead to peaking and instability, while increasing R_2 above the optimum value will reduce the closed-loop bandwidth. If band limiting is required, then a larger value of R_2 than the optimum can be chosen to limit the bandwidth as required.

Since a current-feedback op-amp requires a minimum value of R_2 to guarantee stability, these devices cannot be used with purely capacitive feedback because the reactance of a capacitor reduces at high frequencies. This means that the conventional voltage op-amp integrator cannot be implemented using a current-feedback op-amp.

Practical considerations for broadband designs.

1. *Ground planes.* The purpose of a ground plane is to provide a low-impedance path for currents flowing to ground, since any series impedance in the ground connections will mean that not all ground nodes are at the same potential. In addition, the inductance of a printed circuit track is approximately inversely proportional to the track width, and so the use of thin tracks can result in inductive ground loops, leading to ringing or even oscillations. The use of an unbroken ground plane on one side of the circuit board can minimize the likelihood of inductive loops within the circuit. However, any particularly sensitive ground-connected nodes in the circuit should be grounded as physically close together as is possible.
2. *Bypass capacitors.* Power supply lines often have significant parasitic inductance and resistance. Large transient load currents can therefore result in voltage spikes on the power supply lines, which can couple onto the signal path within the device. Bypass capacitors are therefore used to lower the impedance of the power supply lines at the point of load, and thus short out the effect of the supply line parasitics. The type of bypass capacitor to use is determined by the application and frequency range of interest. High-speed op-amps work best when their power supply pins are decoupled with RF-quality capacitors.

   Manufacturers often recommend using a composite large-small parallel bypass capacitor with something like a 4.7 uF tantalum capacitor on all supply pins, with a parallel 100 nF ceramic to ensure good capacitive integrity at higher frequencies, where the tantalum becomes inductive. However, a note of caution here: This large-small double capacitor technique relies on the large capacitor having sufficiently high ESR so that at resonance the two capacitors do not create a high-Q parallel filter. In surface-mount designs, a single bypass capacitor may well be better than two due to the inherent high-Q of surface-mount capacitors.

   All bypass capacitor connections should be minimized, since track lengths will simply add more series inductance and resistance to the bypass path. The capacitor should be positioned right next to the power supply pin, with the other lead connected directly to the ground plane.
3. *Sensitive nodes.* Certain nodes within a high-frequency circuit are often sensitive to parasitic components. A current-feedback op-amp, for example, is particularly sensitive to parasitic capacitance at the inverting input, since any capacitance at this point combines with the effective resistance at that node to form a second nondominant pole in the feedback loop. The net result of this additional pole is a reduced phase margin, leading to peaking and even instability. Clearly, great care must be taken during layout to reduce track lengths, etc., at this node. In addition, the stray capacitance to ground at $V(-)$ can be reduced by putting a void area in the ground plane at this point. If the op-amp is used as an inverting amplifier, then the potential of the inverting input is held at virtual ground, and any parasitic capacitance will have less effect. Consequently, the current-feedback op-amp is more stable when used in the inverting rather than the noninverting configuration.
4. *Unwanted oscillations.* Following the preceding guidelines should ensure that your circuit is well behaved. If oscillations still occur, a likely source is unintentional positive feedback due to poor

layout. Output signal paths and other tracks should be kept well away from the amplifier inputs to minimize signal coupling back into the amplifier. Input track lengths should also be kept as short as possible for this same reason.

3.1.9 Broadband Amplifier Stability

Operational amplifiers are generally designed with additional on-chip frequency compensation capacitance in place. This is done to present the applications engineer with an op-amp that is simple to use in negative feedback, with minimal chance of unstable operation. In theory, all will be well, but for three main reasons, op-amps become unstable in the real world of analog electronic circuit design. This section outlines the three main causes for unstable operation of broadband amplifiers and shows practical ways of avoiding these pitfalls.

3.1.9.1 Op-Amp Internal Compensation Strategy

Before dealing with specific stability problems in broadband amplifiers and how to solve them, we will look briefly at the internal frequency compensation strategy used in op-amp design. Generally, op-amps can be classified into two groups, those with two high-voltage gain stages and those with only one stage. The two-stage design provides high open-loop gain but relatively low bandwidth, while the higher speed signal-stage amplifier provides lower open-loop gain but much higher usable bandwidth. Insight into the internal op-amp architecture and the type of compensation used will give the designer valuable information on how to tame the unstable op-amp.

3.1.9.2 Review of the Classical Feedback System

Analyzing the classical feedback system in Figure 3.50 gives the well-known expression for the closed-loop gain, A_c:

$$A_c = A/[1 + B \cdot A] \tag{3.53}$$

where A is the open-loop gain of the amplifier and B the feedback fraction. $T = B \times A$ is referred to as the loop-gain, and the behavior of T over frequency is a key parameter in feedback system design. Clearly, if $T \gg 1$ or $A \gg A_c$, then the closed-loop gain is virtually independent of the open-loop gain A, thus

$$A_c \approx B^{-1} \tag{3.54}$$

This is the most important and desirable feature of negative feedback systems. However, the system will not necessarily be stable as, at higher frequencies, phase lag in the open-loop gain A may cause the feedback to become positive.

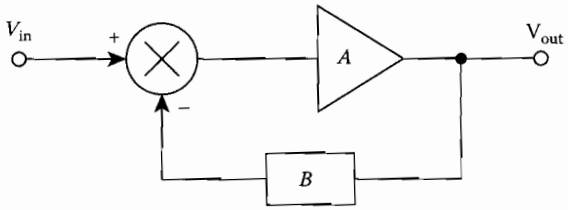


FIGURE 3.50 Classical feedback system.

3.1.9.3 Stability Criteria

Though negative feedback is desirable, it results in potential instability when the feedback becomes positive. The loop-gain T is the best parameter to test whether an amplifier is potentially unstable. The phase margin Φ_M is a common feature of merit used to indicate how far the amplifier is from becoming an oscillator:

$$\Phi_M = 180^\circ + \Phi(|BA| = 1) \tag{3.55}$$

When $\Phi_M = 0°$, the phase of the loop gain, $T = B \times A$ is exactly $-180°$ for $|B \times A| = 1$. The closed-loop gain A_c will become infinite and we have got an oscillator! Clearly, what is required is that $\Phi_M > 0$ and generally the target is to make $\Phi_M \geq 45°$ for reasonably stable performance. However, excessive Φ_M is undesirable if settling time is an important parameter in a particular application.

An op-amp is a general purpose part and so the IC designer strives to produce a maximally versatile amplifier by ensuring that even with 100% feedback, the amplifier circuit will not become unstable. This is done by maintaining a $\Phi_M > 0$ for 100% feedback, that is, when $B = 1$. If the feedback network B is taken to be purely resistive, then any additional phase lag in the loop gain must come from the open-loop amplifier A. Tailoring the phase response of A so that the phase lag is less than 180° up to the point at which $|A| < 1$ or 0 dB ensures that the amplifier is "unconditionally stable"; that is, with any amount of resistive feedback, stable operation is "guaranteed."

Most open-loop op-amps, whether single-stage or two-stage, will exhibit a two-pole response. The separation of these two poles whether at low frequency or high frequency will have a major effect on the stability of the system and it is the op-amp designer's objective to locate these open-loop poles to best advantage to achieve maximum bandwidth, consistent with versatile and stable performance.

3.1.9.4 Two-Stage Op-Amp Architecture

A schematic of the standard two-stage op-amp topology is shown in Figure 3.51. The input differential pair T_1/T_2 provides high gain, as does the second gain stage of T_3/T_4 Darlington pair CE. A high-voltage gain is achieved with this structure, so that output stage is usually a unity voltage gain common-collector output buffer to provide a useful load current drive capability.

The amplifier structure in Figure 3.51 has two internal high-impedance nodes, node X and node Y. These high-impedance nodes are responsible for introducing two dominant poles into the frequency response and their relative location is critical in determining the stability of the amplifier. Each pole contributes a low-pass filter function to the open-loop gain expression of the form

$$[1 + jf/f_P]^{-1} \tag{3.56}$$

Each pole introduces 45° of phase lag at the pole frequency f_P and an additional 45° at $f \approx 10 \times f_P$. With a two-pole amplifier, the open-loop gain A is given by

$$A = A_0/[1 + jf/f_{P1}][1 + jf/f_{P2}] \tag{3.57}$$

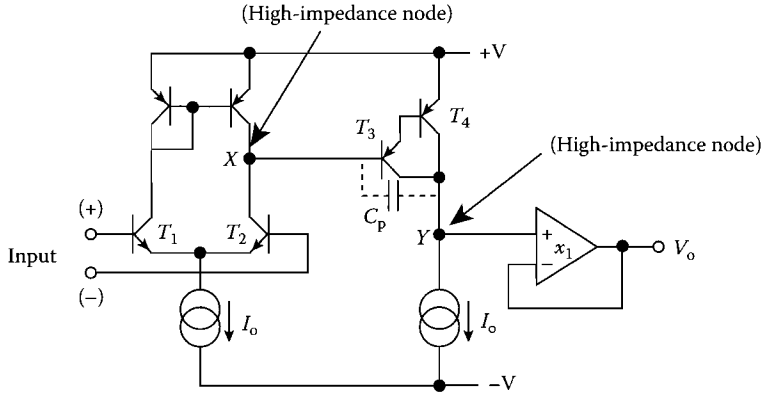


FIGURE 3.51 Architecture of the standard two-stage op-amp.

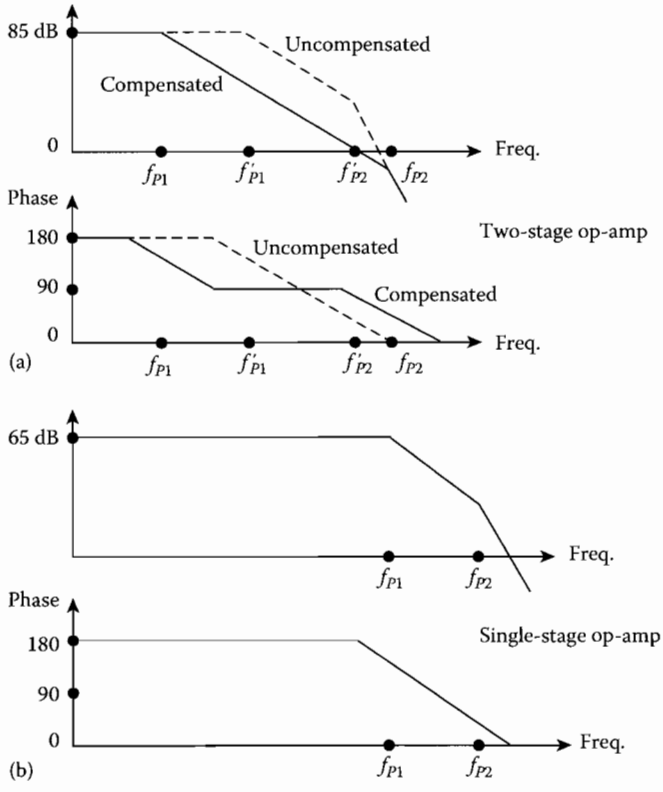


FIGURE 3.52 Pole frequency and phase response for (a) two-stage op-amp and (b) single-stage op-amp.

where A_0 is the dc open-loop gain and f_{P1} and f_{P2} are the two-pole frequencies. A typical plot of A versus f is shown in Figure 3.52a. At low frequencies, where $f \ll f_{P1}$ the gain is flat, and at f_{P1} the gain begins to fall at a rate increasing to −20 dB/decade. The roll-off steepens again at f_{P2} to a final gradient of −40 dB/decade.

It is generally the case that $f_{P1} \ll f_{P2}$ as shown in Figure 3.52a. Turning our attention to the phase plot in Figure 3.52a, at $f = f_{P1}$ the output lags the input by 45°, and as the frequency rises toward f_{P2} the phase lag increases through 135° at f_{P2} to 180° at $f \approx 10 \times f_{P2}$. To ensure unconditionally stable performance, the second pole must be sufficiently far from the first so that the phase margin is large enough.

Figure 3.53 shows curves of the dc value of open-loop gain A_0 versus the ratio N of the pole frequencies ($N = f_{P2}/f_{P1}$) for different values of phase margin. For a given value of $A_0 = 1000$ or +60 dB, the ratio of the pole frequencies must be $N \approx 700$ to obtain a phase margin of 45°.

3.1.9.5 Miller Compensation and Pole Separation

Without any added compensation capacitance, the two open-loop poles of the op-amp are invariably too close to make the amplifier unconditionally stable. The most common compensation method is to add a capacitor between the base and collector of the Darlington pair, shown as C_p in Figure 3.51. This is known as Miller compensation because this strategy makes use of the Miller capacitance multiplication effect discussed earlier. The net result is that the two poles now become significantly far apart, with f_{P1} reducing and f_{P2} increasing, and so the phase margin can be increased to make the op-amp unconditionally stable. However, the penalty of this method is poorer bandwidth and also lower slew rate because of the large capacitance needed, which in practice may be 20 pF or more.

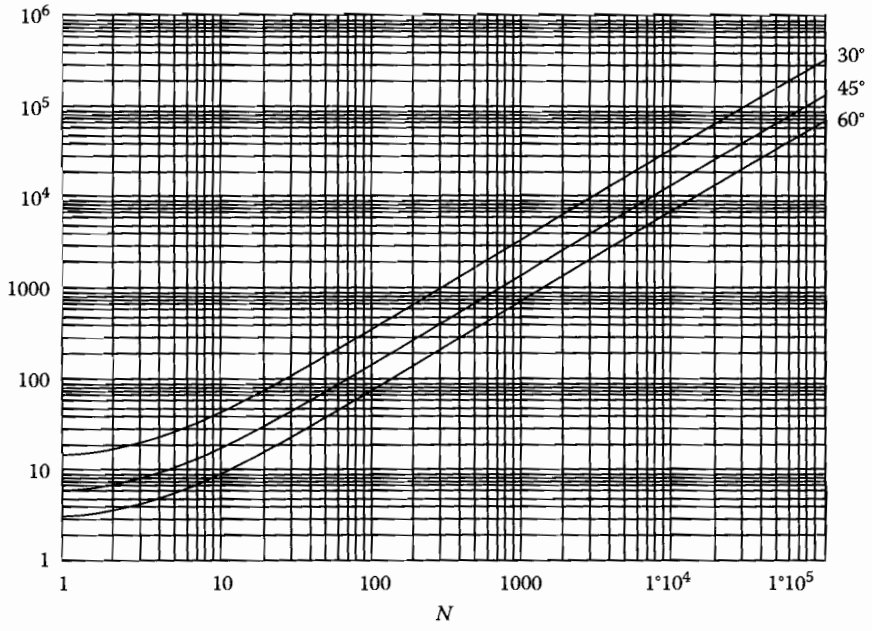


FIGURE 3.53 Low-frequency gain A_0 versus $N\ (=f_{P2}/f_{P1})$ for a two-pole amplifier.

3.1.9.6 Single-Stage Op-Amp Compensation

Figure 3.54 shows a typical simplified circuit schematic of a single-stage op-amp. The input is a differential emitter-coupled pair followed by a folded cascode transistor and an output complementary common-collector buffer. The key difference between this architecture and the two-stage design shown earlier is that X is a low-impedance node, and so the only high-impedance node in the circuit is node Y. Interestingly, the higher frequency nondominant pole of the two-stage amplifier has now become the dominant frequency pole of the single-stage design, as indicated by the second set of curves in Figure 3.52b, which leads to several advantages:

1. The frequency performance off the amplifier is extended. This frequency extension does not lead to a deterioration in phase margin, but simply means that the phase margin problem is shifted up in the frequency domain.

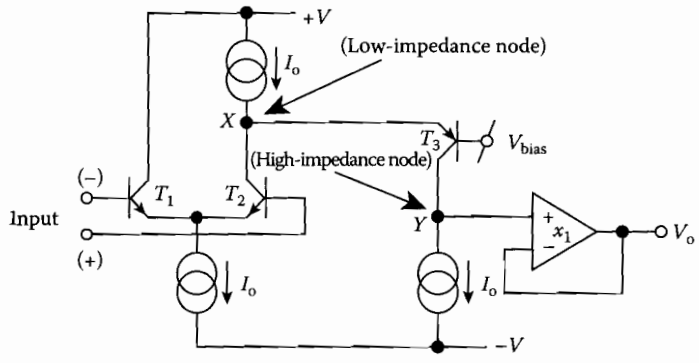


FIGURE 3.54 Architecture of single-stage op-amp.

2. Capacitance at the high-impedance Y node reduces bandwidth, but now improves phase margin.
3. A single value of a few pFs of grounded capacitor at Y will now act as a satisfactory compensation capacitor, unlike the large Miller capacitor required in the two-stage design.
4. The slewing capability of this single-stage structure is very good as a result of the much smaller compensation capacitor.
5. Clearly, it is much more straightforward to develop a stable amplifier for high-frequency applications if it has essentially only one voltage gain stage and so high-frequency op-amp designers generally opt for a single gain stage architecture.

3.1.9.7 Grounded Capacitor Compensation

Typical A_{OL} versus f responses of two single-stage op-amps are shown in Figure 3.55, indicating one high-frequency pole and its proximity to the nondominant pole.

The curves are taken from data for (a) a 2 GHz gain-bandwidth product voltage-feedback op-amp and (b) a 150 MHz current-feedback op-amp. In both cases, the phase characteristics demonstrate the expected 45° lag at the pole frequency, and the slow roll-off in phase at high frequency due to the presence of the very-high-frequency poles.

Both single-stage and two-stage op-amps can be approximated by the two-pole macromodel shown in Figure 3.56. Transconductance G_M and output resistance R_0 represent the gain per stage of $G_M \times R_0$. The difference between the two-stage and single-stage op-amp models is that R_{01} of the single-stage is of the order of $[G_M]^{-1}$ and the dominant compensation capacitor is C_2. C_P in the case of the single stage will

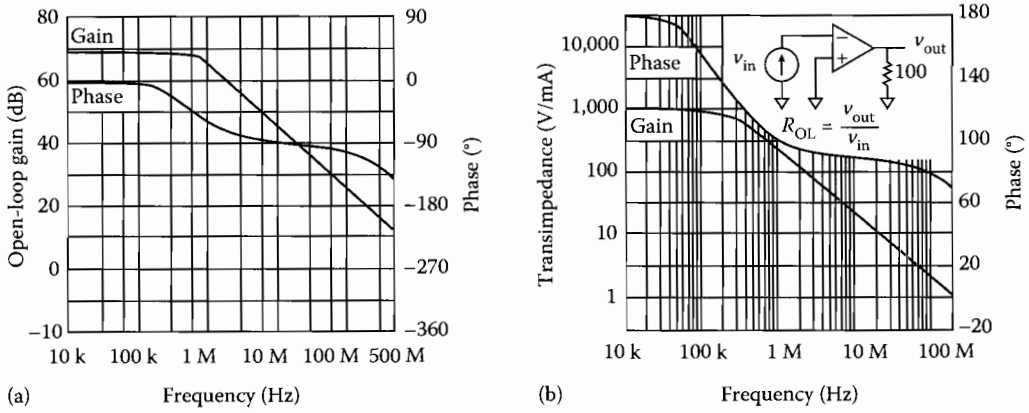


FIGURE 3.55 Single-pole op-amps; open-loop gain and phase frequency characteristics. (a) Voltage feedback. (b) Current feedback.

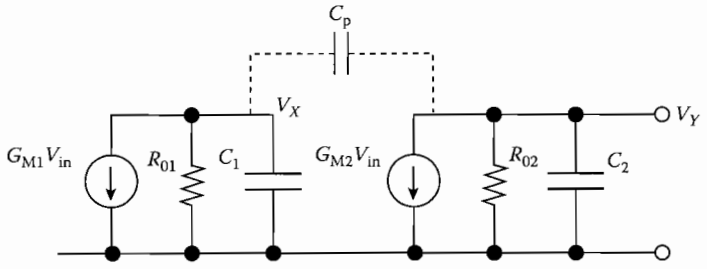


FIGURE 3.56 Partial equivalent circuit of two-pole op-amp.

simply be a feedback parasitic capacitor, while in the case of a two-stage it will be the dominant Miller compensating capacitor. This simple model is an excellent first-cut tool for determining pole locations, and the value of compensation capacitor for a desired bandwidth and stability.

3.1.9.8 High-Frequency Performance

Although the bandwidth in a single-stage design is significantly extended, circuit parasitics become more important. We are confronted with the problem of potential instability, since at higher frequencies the "working environment" of the op-amp becomes very parasitic sensitive; in other words, now op-amp-embedded parasitics cannot be neglected.

An op-amp in closed-loop can be considered at three levels, as shown schematically in Figure 3.57. The inner triangle is the ideal op-amp, internally compensated by the op-amp designer for stable operation using the circuit techniques outlined earlier. High-frequency amplifiers are sensitive to parasitics of the surrounding circuit. The key parasitics within the outer triangle include power supply lead inductance, stray capacitance between power supply pins, and input to ground capacitance. The effect of these parasitics is to destabilize the amplifier, and so the designer is confronted with the task of reestablishing stable operation. The approach needed to achieve this parallels the work of the op-amp designer. The parasitics almost always introduce additional extrinsic nondominant poles, which need to be compensated. The task of compensation cannot be attempte without considering the outer or third level, which includes the closed-loop gain defining components together with the load impedance. Again, stray reactance associated with these components will modify the loop gain, and so to guarantee stable operation of the closed-loop amplifier it is necessary to compensate the complete circuit.

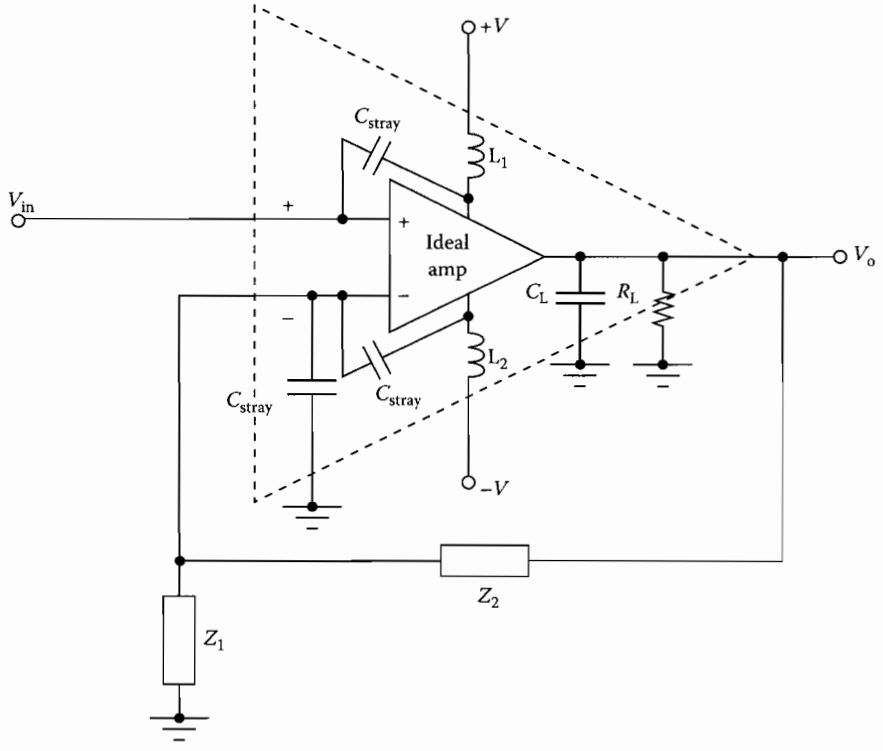


FIGURE 3.57 Real feedback amplifier.

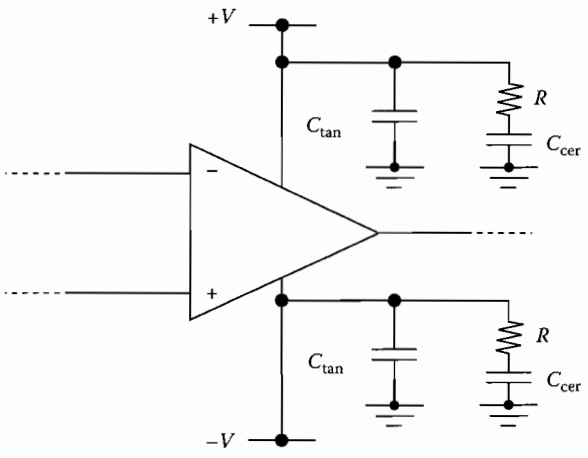


FIGURE 3.58 Supply decoupling circuitry (C_{CER} = ceramic capacitor and C_{TAN} = tantalum).

3.1.9.9 Power Supply Impedance

In this section, we consider the ways in which the impedance of the power supply can affect the frequency response of the amplifier. First, some important rules are

1. There is no such thing as an ideal zero-impedance power supply.
2. Real power supplies have series *R–L* impedance and at high frequencies the inductance matters most.
3. Power supply inductance causes "bounce" on the power supply voltage, generating unwanted feedback via parasitic capacitive links to the inputs. Power supply "bounce" increases with increasing load current.
4. Supply decoupling capacitors act as "short-term local batteries" to maintain power supply integrity, and it is important that they are placed as close as possible to the power supply pins of the op-amp.

Large electrolytic capacitors are fine at low frequencies but are inductive at high frequencies. Figure 3.58 shows commonly used decoupling circuitry. Small-sized tantalum electrolytics are preferred, while a parallel ceramic capacitor with low series inductance takes over the decoupling role at high frequencies. The added series *R* prevents the inductance of the electrolytic resonating with the ceramic capacitor. The waveforms in Figure 3.59 illustrate the benefits of good decoupling.

3.1.9.10 Effects of Resistive and Capacitive Loads

The load presented to an amplifier is likely to have both resistive and capacitive components, as illustrated previously in Figure 3.57. Increasing the load current causes power supply ripple, so good power supply decoupling is vital.

A closed-loop amplifier with voltage-sampled negative feedback results in a very-low output impedance, so it is natural to think that the effects of any load would be shunted out by this low impedance. In reality, the load has an important effect on the amplifier and must not be overlooked. Resistive loads, for example, cause two main effects. First, as a voltage divider with the open-loop output resistance of the op-amp r_0, the open-loop gain is reduced. This effect is small unless the load resistance approaches r_0. Second, the load current is routed to the output pin via the supply pins, and as the load current increases,

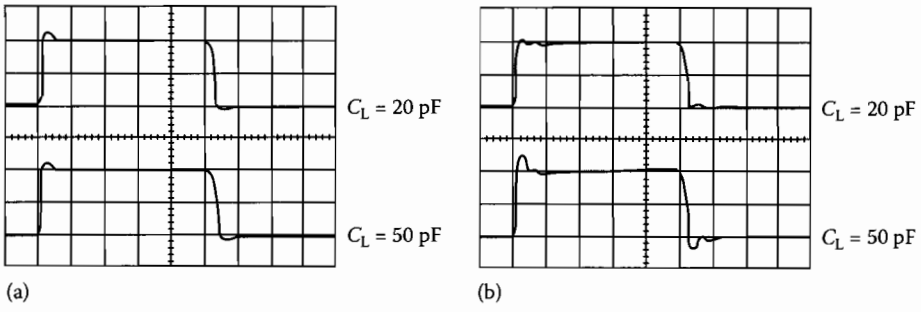


FIGURE 3.59 High-speed voltage buffer: (a) with and (b) without supply decoupling.

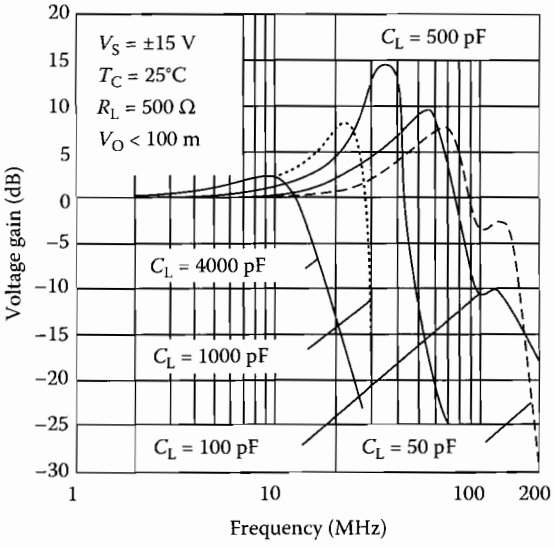


FIGURE 3.60 Load capacitance causes gain peaking.

the supply pin voltage is modulated. This effect is more important, since the integrity of the power supply will be degraded. Again, good supply decoupling is essential to minimize this effect.

Capacitive load current is proportional to the derivative of output voltage, and the maximum capacitive output current demand occurs when dV_{out}/dt is a maximum. Though not directly a stability issue, the designer must remember that a capacitive load demands high-output current at high frequencies and at high amplitude, that is,

$$I_{max} = C_L \cdot 2\pi f_{max} \cdot V_{outpeak} \tag{3.58}$$

Figure 3.60 illustrates the effect of load capacitance on the loop gain.

C_1 together with the equivalent output resistance of the op-amp adds an additional pole into the loop gain of the form

$$V_F/V_{out} = B = 1/[1 + jf/f_L] \quad \text{where } f_L = 1/2\pi r_0 \cdot C_L \tag{3.59}$$

The load resistance has a minor influence on the loop gain compared to the effects of load capacitance by slightly reducing the value of dc open-loop gain by factor K, where $K = R_L/[r_0 + R_L]$, as described above. Since the effective output resistance reduces to $r_{0'} = r_0/R_L$, then f_L changes to $f_{L'} = 1/2\pi r_{0'} C_L$.

3.1.9.11 Neutralizing the Phase Lag

To compensate for high-frequency phase lag, the simplest technique is to add a series resistance R between the output of the op-amp and the load connection point, as shown in Figure 3.61.

The series resistor adds a zero into the V_F/V_{out} equation, which changes to

$$V_F/V_{out} = K \cdot [1 + jf/f_Z]/[1 + jf/f_P] \tag{3.60}$$

where $K = [R + R_L]/[r_0 + R + R_L]$, $f_P = 1/[2\pi(r_0 + R)/R_L \cdot C_L]$ and $f_Z = 1/[2\pi R_{L'}/R \cdot C_L] = f_P \cdot [1 + r_0/R]$, so clearly; $f_P < f_Z$.

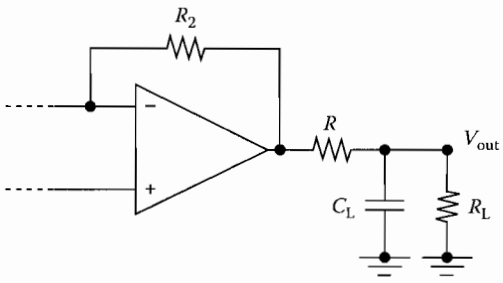


FIGURE 3.61 Load capacitance neutralization.

The phase lag introduced by the pole is compensated by the phase lead of the zero at higher frequencies. The maximum phase lag is limited if the zero is close to the pole, almost eliminating the effects of the load capacitor. Maximum phase lag in V_F/V_{out} occurs at $f = f_M$, where f_M is given by

$$f_M = [f_P \cdot f_Z]^{1/2} = f_P \times (1 + r_0/R)^{1/2} \tag{3.61}$$

and at f_M the phase lag $\Phi = \Phi'$ is given by

$$\begin{aligned} \Phi' &= 90^\circ - 2 \cdot \tan^{-1}[f_M/f_P] = 90^\circ - 2 \cdot \tan^{-1}\left[(1 + r_0/R)^{1/2}\right] \\ \Phi' &\approx -19.5^\circ \quad \text{for} \quad R = r_0 \\ \Phi' &\approx -8.2^\circ \quad \text{for} \quad R = 2 \cdot r_0 \\ \Phi' &\approx -6.4^\circ \quad \text{for} \quad R = 3 \cdot r_0 \end{aligned} \tag{3.62}$$

These values show that the added lag Φ' is not excessive as long as $R > r_0$. The disadvantage with this method is that the series resistor is in direct line with the output current, increasing the output resistance of the amplifier and limiting the output current drive capability. The output impedance also goes inductive at high frequencies.

An alternative way of solving the problem of capacitive load is to view the closed-loop output resistance of the op-amp as being inductive, since the closed-loop output impedance of the op-amp is essentially the open-loop output resistance divided by the loop gain. As the loop gain falls with frequency, the output impedance rises, and thus appears inductive. Adding a load capacitor generates a resonant circuit. The solution is to "spoil" the Q of the resonator, therefore minimizing the added phase lag of C_L.

Adding a so-called series R–C "snubber," as in Figure 3.62, effects a cure. The resistor R is ac coupled by the capacitor at high frequencies and spoils the Q. Effectively, C_L resonates with the inductive output impedance, and at this frequency leaves the R–C snubber as a "new" load. The equivalent circuit is therefore close to the previous compensation method shown in Figure 3.61, but with the added advantage that now the load current is not carried by the series resistance. To select the snubber component values, make $R = 1/2\pi f_0 C$, where f_0 is the resonant frequency, which can simply be determined experimentally from the amplifier without the snubber in place. The value of the series capacitance is a compromise: too big and it will increase the effective load capacitance. Choosing $C = C_L$ works reasonably well in practice.

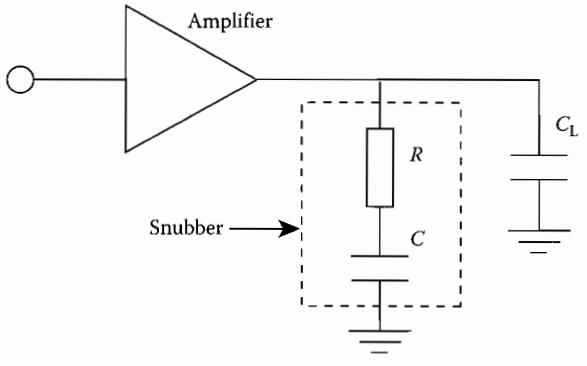


FIGURE 3.62 Snubber cures capacitive load peaking.

3.1.9.12 Inverting Input Capacitance to Ground

With most broadband bipolar op-amps, parasitic capacitance to ground adds an additional pole (and hence phase lag) into the feedback path, which threatens stability. Stray capacitance C_1 at the inverting input pin (shown previously in Figure 3.57) modifies B and adds phase lag in the loop-gain T, compromising stability.

Solving for B with C_1 taken into account will clarify the problem. It is simple to show that

$$B = V_F/V_{out} = Z_1/[Z_1 + Z_2] \tag{3.63}$$

where $Z_1 = R_1/[1 + j\omega R_1 C_1]$ and $Z_2 = R_2$. Substituting, we get

$$B = K/[1 + jf/f_C] \tag{3.64}$$

where $K = R_1\ [R_1 + R_2]$ and $f_C = 1/[2\pi C_1 R_1/R_2]$.

The additional pole at $f = f_C$ will now give the circuit a very undesirable three-pole loop gain, which could cause significant gain peaking, as shown in Figure 3.63. f_C could be made high by choosing relatively low values of $R_1 // R_2$ but the additional pole can be eliminated by adding a feedback capacitor C_2 across resistor R_2 to give pole-zero cancellation.

$$Z_1 = R_1/[1 + j\omega R_1 C_1] \quad \text{and} \quad Z_2 = R_2/[1 + j\omega R_2 C_2] \tag{3.65}$$

If $R_1C_1 = R_2C_2$, then $B = Z_1/[Z_1 + Z_2] = R_1/[R_1 + R_2]$, making B frequency independent. The design equation for C_2 is then

$$C_2 = C_1 \cdot R_1/R_2 \tag{3.66}$$

If the open-loop phase margin Φ_M needs to be increased for the desired value of closed-loop gain, and the inverting capacitance C_1 has its inevitable high-frequency influence, then the optimum solution for C_2 would be to locate the zero on the second pole of the loop-gain response following the procedure given above.

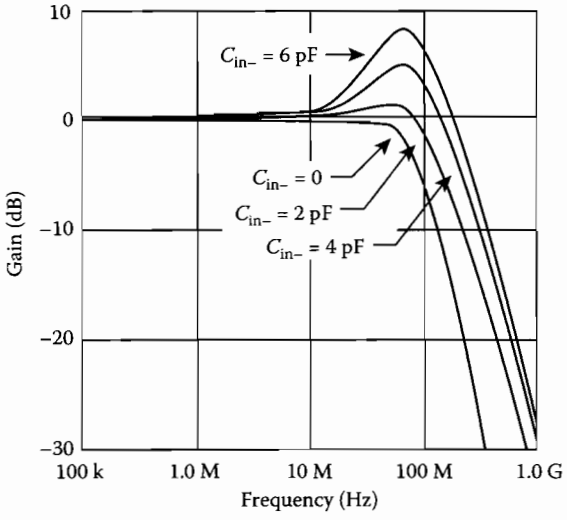
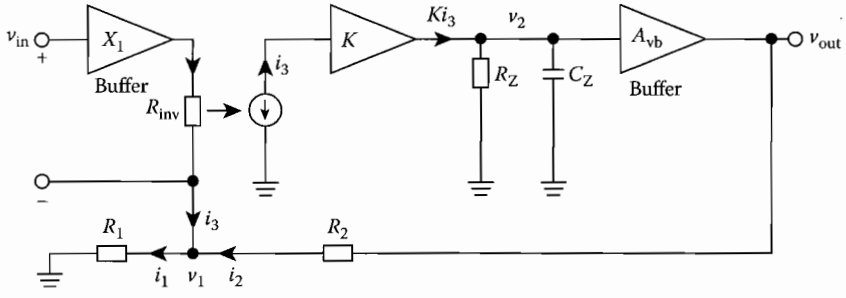


FIGURE 3.63 Stray input capacitance causes gain peaking.

3.1.10 Conclusions

This chapter hopefully serves to illustrate some of the modern techniques the practicing engineer will encounter when designing broadband bipolar amplifiers. It focuses mainly upon key generic building blocks and methodologies for broadband design. Many circuits and design techniques have not been covered, but analysis techniques described should serve as a foundation for the analysis of other broadband designs. Furthermore, comprehensive analytical treatment of many alternative broadband bipolar circuits can be found in the texts [6,13–15].

Appendix A: Transfer Function and Bandwidth Characteristic of Current-Feedback Operational Amplifier



$$-i_1 + i_2 + i_3 = 0 \tag{3.67}$$

$$i_1 = \frac{v_1}{R_1} \tag{3.68}$$

$$i_2 = \frac{v_{out} - v_1}{R_2} \tag{3.69}$$

$$i_3 = \frac{v_{in} - v_1}{R_{inv}} \tag{3.70}$$

$$v_2 = \frac{Ki_3R_Z}{1 + j\omega R_Z C_Z} \tag{3.71}$$

$$v_{out} = A_{vb}v_2 \tag{3.72}$$

Substituting Equations 3.68 through 3.70 into Equation 3.67 yields

$$-\frac{v_1}{R_1} + \frac{v_{out} - v_1}{R_2} + \frac{v_{in} - v_1}{R_{inv}} = 0$$

Rearranging for v_1 gives

$$v_1 = \frac{v_{in}R_2/R_{inv} + v_{out}}{1 + (R_2/R_1) + (R_2/R_{inv})}$$

From Equations 3.71 and 3.72, it is clearly seen that

$$v_{out} = \frac{A_{vb} K i_3 R_Z}{1 + j\omega R_Z C_Z} \tag{3.73}$$

Substituting for i_1 and i_2 from Equations 3.68 and 3.69 into Equation 3.67 gives

$$i_3 = v_1 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{v_{out}}{R_2}$$

Substitute for v_1:

$$i_3 = \left[\frac{v_{in} R_2 / R_{inv} + v_{out}}{1 + (R_2/R_1) + (R_2/R_{inv})} \right] \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{v_{out}}{R_2}$$

Substitute for i_3 from Equation 3.73:

$$\frac{v_{out}(1 + j\omega R_Z C_Z)}{A_{vb} K R_Z} = \left\{ \left[\frac{v_{in} R_2 / R_{inv} + v_{out}}{1 + (R_2/R_1) + (R_2/R_{inv})} \right] \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{v_{out}}{R_2} \right\}$$

rearranging

$$v_{out} \left[\frac{(1 + j\omega R_Z C_Z)}{A_{vb} K R_Z} - \frac{(1/R_1 + 1/R_2)}{1 + (R_2/R_1) + (R_2/R_{inv})} + \frac{1}{R_2} \right] = \frac{(v_{in} R_2 / R_{inv})(1/R_1) + (1/R_2)}{1 + (R_2/R_1) + (R_2/R_{inv})}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\frac{R_{inv}(1 + (R_2/R_1) + (R_2/R_{inv}))(1 + j\omega R_Z C_Z)}{A_{vb} K R_Z} - R_{inv}((1/R_1) + (1/R_2)) + \frac{R_{inv}(1 + (R_2/R_1) + (R_2/R_{inv}))}{R_2}}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K R_Z} + \frac{(R_{inv}(1 + (R_2/R_1)) + R_2) j\omega R_Z C_Z}{A_{vb} K R_Z} + 1}$$

Factorize the denominator

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[1 + \frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K R_Z} \right] \left[1 + \frac{\frac{(R_{inv}(1 + (R_2/R_1)) + R_2) j\omega R_Z C_Z}{A_{vb} K R_Z}}{1 + \frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K R_Z}} \right]}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[1 + \frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K R_Z} \right] \left[1 + j\omega C_Z \left\{ \frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K + \frac{R_{inv}(1 + (R_2/R_1)) + R_2}{R_Z}} \right\} \right]}$$

If we assume that R_Z is very large, then

$$\frac{R_{inv}(1 + (R_2/R_1)) + R_2}{R_Z} \approx 0$$

and the transfer function becomes

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{1 + j\omega C_Z \left[\frac{R_{inv}(1 + (R_2/R_1)) + R_2}{A_{vb} K} \right]}$$

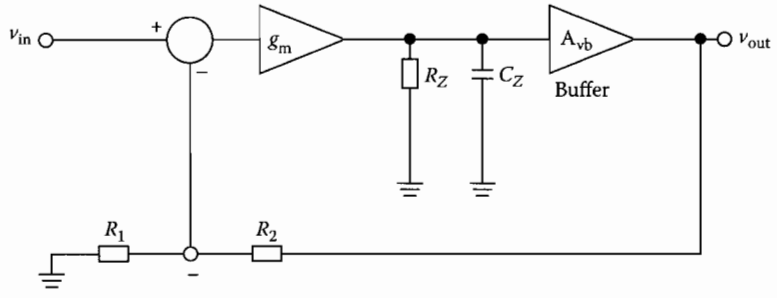
The pole frequency is given by

$$f_{-3\text{ dB}} = \frac{A_{vb}K}{2\pi C_Z[R_{inv}(1 + (R_2/R_1)) + R_2]}$$

The gain-bandwidth product is given by

$$GBW = \frac{A_{vb}K[1 + (R_2/R_1)]}{2\pi C_Z[R_{inv}(1 + (R_2/R_1)) + R_2]}$$

Appendix B: Transfer Function and Bandwidth Characteristic of Voltage-Feedback Operational Amplifier



$$v_{out} = \left(v_{in} - \frac{R_1}{R + R_2 v_{out}}\right)\frac{g_m R_Z A_{vb}}{1 + j\omega R_Z C_Z}$$

$$v_{out}\left[1 + \frac{R_1 g_m A_{vb} R_Z}{(R_1 + R_2)(1 + j\omega R_Z C_Z)}\right] = v_{in}\frac{g_m A_{vb} R_Z}{1 + j\omega R_Z C_Z} \tag{3.74}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m A_{vb} R_Z/(1 + j\omega R_Z C_Z)}{1 + \frac{R_1 g_m A_{vb} R_Z}{(R_1 + R_2)(1 + j\omega R_Z C_Z)}}$$

Multiply the numerator and denominator by $(1 + j\omega R_Z C_Z)/g_m\, A_{vb}\, R_Z$

$$\frac{v_{out}}{v_{in}} = \frac{1}{\frac{1 + j\omega R_Z C_Z}{g_m A_{vb} R_Z} + \frac{R_1}{(R_1 + R_2)}}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[\frac{1 + j\omega R_Z C_Z}{g_m A_{vb} R_Z}\right][1 + (R_2/R_1)] + 1}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\frac{1 + (R_2/R_1)}{g_m A_{vb} R_Z} + \frac{j\omega R_Z C_Z(1 + (R_2/R_1))}{g_m A_{vb} R_Z} + 1}$$

get $1 + [1 + (R_2/R_1)/g_m\, A_{vb}\, R_Z]$ out of the denominator

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[1 + \frac{1+(R_2/R_1)}{g_m A_{vb} R_Z}\right]\left[1 + \frac{\frac{j\omega R_Z C_Z (1+(R_2/R_1))}{g_m A_{vb} R_Z}}{1 + \frac{1+(R_2/R_1)}{g_m A_{vb} R_Z}}\right]}$$

multiply the denominator bracket by $g_m A_{vb} R_z/[1 + (R_2/R_1)]$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[1 + \frac{1+(R_2/R_1)}{g_m A_{vb} R_Z}\right]\left[1 + \frac{j\omega R_Z C_Z (1+(R_2/R_1))}{g_m A_{vb} R_Z + (1+(R_2/R_1))}\right]}$$

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{\left[1 + \frac{1+(R_2/R_1)}{g_m A_{vb} R_Z}\right]\left[1 + \frac{j\omega R_Z C_Z}{\frac{g_m A_{vb} R_Z}{1+(R_2/R_1)}}\right]}$$

assuming that $g_m A_{vb} R_Z$ is much larger than $1 + R_2/R_1$, then

$$\frac{v_{out}}{v_{in}} = \frac{1 + (R_2/R_1)}{1 + j\omega\left[\frac{R_Z C_Z}{1 + \frac{g_m A_{vb} R_Z}{1+(R_2/R_1)}}\right]}$$

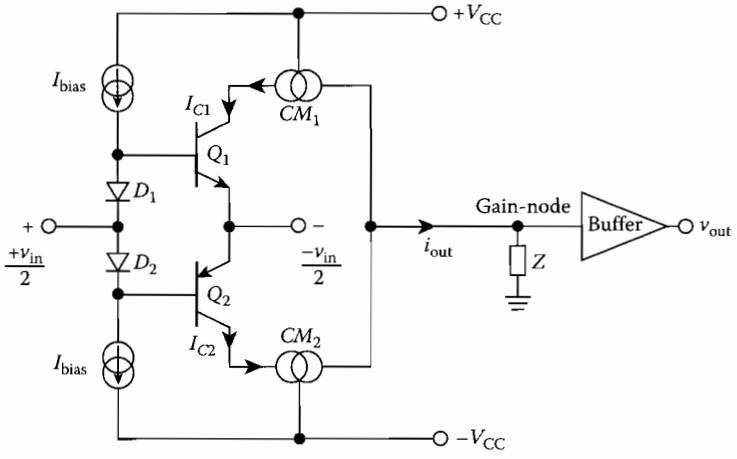
The pole frequency is given by

$$f_{-3\text{ dB}} = \frac{1 + \frac{g_m A_{vb} R_Z}{1+(R_2/R_1)}}{2\pi R_Z C_Z}$$

The gain-bandwidth product is given by

$$GBW = \frac{(1 + (R_2/R_1))\left[1 + \frac{g_m A_{vb} R_Z}{(1+(R_2/R_1))}\right]}{2\pi R_Z C_Z}$$

Appendix C: Transconductance of the Current-Feedback Op-Amp Input Stage



$$v_{in} = v_1 - v_2$$

$$i_{out} = I_{CI} - I_{C2}$$

$$I_{C1} = I_{S1} e^{\frac{v_{BE1}}{v_T}}$$

$$I_{C2} = I_{S2} e^{\frac{v_{BE2}}{v_T}}$$

$$V_{BE1} = V_{DQ1} + v_{in}$$

$$V_{BE2} = v_{in} - V_{DQ2}$$

$$I_{C1} = I_{S1} e^{\left(\frac{V_{DQ1}}{V_T} + \frac{v_{in}}{v_T}\right)}$$

$$I_{C2} = I_{S2} e^{\left(\frac{V_{DQ1}}{V_T} - \frac{v_{in}}{v_T}\right)}$$

$$I_{C1} = I_{CQ1} e^{\frac{v_{in}}{v_T}}$$

$$I_{C2} = I_{CQ2} e^{-\frac{v_{in}}{v_T}}$$

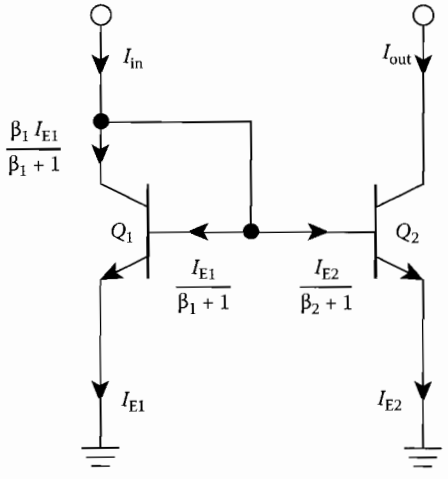
Assuming matched transistors then, $I_{CQ1} = I_{CQ2} = I_{CQ}$

$$i_{out} = I_{C1} - I_{C2} = I_{CQ}\left[e^{+\left(\frac{v_{in}}{v_T}\right)} - e^{-\left(\frac{v_{in}}{v_T}\right)}\right]$$

$$\frac{i_{out}}{I_{CQ}} = y = [e^x - e^{-x}] = 2\sinh(x)$$

where $x = +v_{in}/V_T$.

Appendix D: Transfer Function of Widlar Current Mirror



$$I_{in} = I_{E1} + \frac{I_{E2}}{\beta_2 + 1}$$

$$I_{in} = \frac{I_{E1}(\beta_2 + 1) + I_{E2}}{\beta_2 + 1}$$

$$I_{out} = \beta_2 I_{B2}$$

$$I_{out} = \frac{\beta_2 I_{E2}}{\beta_2 + 1}$$

$$\frac{I_{out}}{I_{in}} = \frac{(\beta_2 I_{E2})(\beta_2 + 1)}{(\beta_2 + 1)[I_{E1}(\beta_2 + 1) + I_{E2}]}$$

$$\frac{I_{out}}{I_{in}} = \frac{\beta_2 I_{E2}}{I_{E1}(\beta_2 + 1) + I_{E2}}$$

$$\frac{I_{out}}{I_{in}} = \frac{1}{\frac{I_{E1}(\beta_2 + 1)}{I_{E2}\beta_2} + \frac{1}{\beta_2}}$$

For

$$\frac{I_{E1}}{I_{E2}} = \frac{I_{S1}\left(\frac{\beta_1 + 1}{\beta_1}\right) e^{\frac{v_{BE1}}{V_T}}}{I_{S2}\left(\frac{\beta_2 + 1}{\beta_2}\right) e^{\frac{v_{BE2}}{v_T}}}$$

Then, as $V_{BE1} = V_{BE2}$,

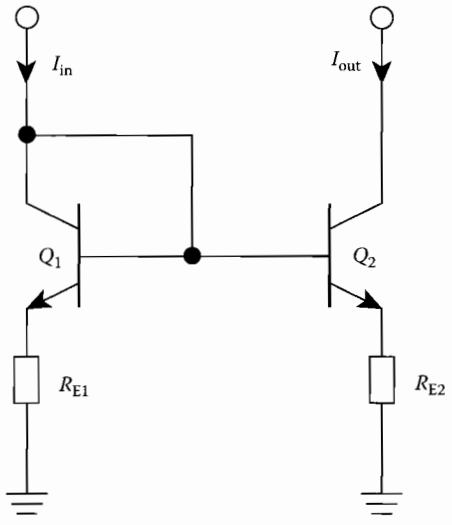
$$\frac{I_{E1}}{I_{E2}} = \frac{I_{S1}(\beta_1 + 1/\beta)}{I_{S2}(\beta_2 + 1/\beta_2)}$$

$$\frac{I_{out}}{I_{in}} = \frac{1}{\frac{I_{S1}(\beta_1 + 1)}{I_{S2}\beta_1} + \frac{1}{\beta_2}}$$

Assume $\beta_1 = \beta_2 = \beta$, $I_{S1} = I_{S2}$. Then

$$\frac{I_{out}}{I_{in}} = \frac{\beta}{\beta + 2}$$

Appendix E: Transfer Function of Widlar Current Mirror with Emitter Degeneration Resistors



Assuming that $\beta \gg 1$, then

$$V_{BE1} + I_{in}R_1 = V_{BE2} + I_{out}R_2$$

$$I_{out} = \frac{I_{in}R_1}{R_2} + \frac{(V_{BE1} - V_{BE2})}{R_2}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} + \frac{(V_{BE1} - V_{BE2})}{I_{in}R_2}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} + \frac{V_T \ln\left(\frac{I_{in}}{I_{S1}}\frac{I_{S2}}{I_{out}}\right)}{I_{in}R_2}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} + \frac{V_T(\ln(I_{in}/I_{out}) + (\Delta V_{BE}/V_T))}{I_{in}R_2}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} + \frac{V_T(\ln(I_{in}/I_{out}))}{I_{in}R_2} + \frac{\Delta V_{BE}}{I_{in}R_2}$$

Assuming that the term $V_T[\ln(I_{in}/I_{out})]/I_{in}R_2$ is small compared with the other terms, then

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} + \frac{\Delta V_{BE}}{I_{in}R_2}$$

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3.2 Bipolar Noise

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Bipolar transistors and other electronic devices generate inherent electrical noise. This limits the device operation at a small-signal range. There are a few different sources of noise, such as thermal noise, shot noise, generation–recombination, $1/f$ (flicker noise), and $1/f^2$ noise, burst noise or random telegraph signal noise (RTS noise), and avalanche noise [1,6].

3.2.1 Thermal Noise

Thermal noise is created by random motion of charge carriers due to the thermal excitation [1]. This noise is sometimes known as the Johnson noise. In 1905 Einstein presented his theory of fluctuating movement of charges in thermal equilibrium. This theory was experimentally verified by Johnson in 1928. The thermal motion of carriers creates a fluctuating voltage on the terminals of each resistive element. The average value of this voltage is zero, but the power on its terminals is not zero. The internal noise voltage source or current source is described by Nyquist equation

$$\overline{v_n^2} = 4kTR\Delta f, \quad \overline{i_n^2} = \frac{4kT\Delta f}{R} \tag{3.75}$$

where

k is the Boltzmann constant
T is absolute temperature
$4kT$ is equal to 1.61×10^{-20} V · C at room temperature

The thermal noise is proportional to the frequency bandwidth Δf. It can be represented by the voltage source in series with resistor R, or by the current source in parallel to the resistor R. The maximum noise

power can be delivered to the load when $R_L = R$. In this case maximum noise power in the load is $kT\Delta f$. The noise power density $dP_n/df = kT$, and it is independent of frequency. Thus, the thermal noise is the white noise. The RMS noise voltage and the RMS noise current are proportional to the square root of the frequency bandwidth Δf. The thermal noise is associated with every physical resistor in the circuit. In a bipolar transistor, the thermal noise is generated mainly by series base, emitter, and collector resistances.

Spectral density of the equivalent voltage and currant thermal noise are given by

$$S_{vR} = 4kT_kR \tag{3.76}$$

or

$$S_{iG} = 4kT_kG \tag{3.77}$$

These spectral noise densities are constant up to 1 THz and it is proportional to temperature and to resistance of elements and as such can be used to indirectly measure:

- The device temperature
- Series distributed resistances of bipolar transistors (primarily base resistance)
- Quality of contacts and connections

3.2.2 Shot Noise

Shot noise is associated with a discrete structure of electricity and the individual carrier injection through the *pn* junction. In each forward biased junction, there is a potential barrier which can be overcome by the carriers with higher thermal energy. This is a random process and the noise current is given by

$$\overline{i_n^2} = 2qI\Delta f \tag{3.78}$$

Spectral density of the shot noise is temperature independent and it is proportional to the junction current:

$$S_{is} = 2qI \tag{3.79}$$

where

q is the electron charge
I is the forward junction current

Shot noise is usually considered as a current source connected in parallel to the small-signal junction resistance. The measurement of shout noise in modern nanoscale devices is relatively difficult since measured values of current are in the range of 100 fA.

Shot noise has to be proportional to the current and any deviation from this relation can be used to evaluate parasitic leaking resistances. It can be used for diagnosis of photodiodes, Zener diodes, avalanche diodes, and Schottky diodes.

3.2.3 Generation–Recombination Noise

The generation–recombination noise is caused by the fluctuation of number of carriers due to existence of the generation–recombination centers. Variation of number of carriers leads to changes of device conductance. This type of noise is function of both temperature and biasing conditions. The spectral density of the generation–recombination noise is described by

$$\frac{S_{g-r}(f)}{N^2} = \frac{(\overline{\Delta N})^2}{N^2} \cdot \frac{4\tau}{1 + (2\pi f \cdot \tau)^2} \tag{3.80}$$

where

$(\overline{\Delta N})^2$ is the variance of the number of carriers N

τ is the carrier lifetime

Spectral density is constant up to the frequency $f_{g-r} = 1/(2\pi\tau)$, and after that is decreasing proportionally to $1/f^2$.

In the case when there are several types of generation–recombination centers with different carrier life time the resultant noise spectrum will be a superposition of several distributions described by Equation 3.80. Therefore the spectral distribution of noise can be used to investigate various generation–recombination centers. This is an alternative method to deep level transient spectroscopy (DLTS) to study generation–recombination processes in semiconductor devices.

3.2.4 *1/f* Noise

The $1/f$ noise is the dominant noise in the low-frequency range and its spectral density is proportional to $1/f$. This noise is present in all semiconductor devices under biasing. This noise is usually associated with material failures or with imperfection of a fabrication process. Most of research results conclude that this noise exists even for very low frequencies up to 10^{-6} Hz (frequency period of several weeks). This noise is sometimes used to model fluctuation of device parameters with time. There are two major models of $1/f$ noise:

- Surface model developed by McWhorter in 1957 [7]
- Bulk model developed by Hooge in 1969 [8]

The simplest way to obtain $1/f$ characteristics is to superpose many different spectra of generation–recombination noises, where free carriers are randomly trapped and released by centers with different life times. This was the basic concept behind McWhorter model where it was assumed that

- In the silicon oxide near the silicon surface there are uniformly distributed trap centers
- Probability of the carrier penetration to trap centers is decreasing exponentially with the distance from the surface.
- Time constants of trap centers increases with the distance from the surface
- Trapping mechanisms by separate centers are independent

The resulted noise spectral density is given by

$$S_{1/f} \propto (\overline{\Delta N})^2 \int_{\tau_1}^{\tau_2} \frac{1}{\tau} \frac{4\tau}{1 + \omega\tau^2} \cdot d\tau = (\overline{\Delta N})^2 \cdot \frac{1}{f} \quad \text{for } 1/\tau_2 \ll \omega \ll 1/\tau_1 \tag{3.81}$$

The spectral density is constant up to frequency $f_2 = 1/(2\pi\tau_2)$, then is proportional to $1/f$ between f_2 and $f_1 = 1/(2\pi\tau_1)$, from frequency f_1 is proportional to $1/f^2$. The McWhorter model is primarily used for MOS devices.

For bipolar transistor Hooge bulk model is more adequate. In this noise model Hooge uses in the carrier transport two scattering mechanisms of carries: scattering on the silicon lattice and scattering on impurities. He assumed that only scattering on the crystal lattice is the source of the $1/f$ noise, while scattering on the impurities has no effect on noise level. All imperfections of the crystal lattice leads to large $1/f$ noise.

The noise spectral density for the Hooge model is

$$S_{1/f} = \frac{\alpha_H \cdot I^\beta}{f^\gamma \cdot N} \tag{3.82}$$

where
$\alpha_H = 2 \cdot 10^{-3}$ is the Hooge constant [8]
β and γ are material constants
N is the number of carriers

Later [9] Hooge proposed to use α_H as variable parameter, which in the case of silicon devices may vary from $5 \cdot 10^{-6}$ to $2 \cdot 10^{-3}$.

The $1/f$ noise is increasing with the reduction of device dimensions and as such is becoming a real problem for devices fabricated in nanoscale. The level of $1/f$ noise is often used as the measure of the quality of devices and its reliability. Devices fabricated with well-developed technologies usually have much smaller level of $1/f$ noise. The $1/f$ noise (flicker noise) sometimes is considered to be responsible for the long term device parameter fluctuation.

3.2.5 Noise $1/f^2$

The noise $1/f^2$ is a derivative of $1/f$ noise and it is observed mainly in metal interconnections of integrated circuits. It has become more evident for very narrow connections where there is a possibility of electromigration due to high current densities. In aluminum the electromigration begins at current densities of 200 $\mu A/\mu m^2$ and noise characteristics changes from $1/f^2$ to $1/f^\gamma$, where $\gamma > 2$. Also the noise level increases proportionally to the 3rd power of the biasing current:

$$S_{1/f^2}(f) = \frac{C \cdot J^\beta}{f^\gamma \cdot T} \cdot \exp(-E_a/k \cdot T) \tag{3.83}$$

where
$\beta \geq 3$, $\gamma \geq 2$
C is experimentally found constant
E_a activation energy of the electromigration
$k = 8.62 \cdot 10^{-5}$ eV/K is the Boltzmann constant

The degeneration of metallic layer is described by

$$v_d \propto J^n \exp(-E_a/k \cdot T) \tag{3.84}$$

Since Equations 3.83 and 3.84 have a similar character therefore the $1/f^2$ noise can be used as the measure of the quality of metal interconnections. This is a relatively fast and accurate method to estimate reliability of metal interconnections.

3.2.6 Burst Noise—RTS Noise

The burst noise is another type of noise at low frequencies [3,4]. Recently this noise is described as RTS noise. With given biasing condition of a device the magnitude of pulses is constant, but the switching time is random. The burst noise looks, on an oscilloscope, like a square wave with the constant magnitude, but with random pulse widths (see Figure 3.64). In some cases the burst noise may have not two but several different levels.

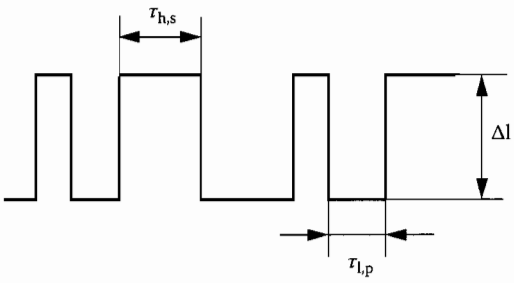

FIGURE 3.64 Example of RTS noise waveform.

Spectral density of the RTS noise has similar form like generation–recombination noise:

$$S_{RTS} = C\frac{4 \cdot (\Delta I)^2}{1 + (2\pi f / f_{RTS})^2} \tag{3.85}$$

where

$$C = \frac{1}{(\overline{\tau_l} + \overline{\tau_h}) \cdot f_{RTS}^2}$$

$f_{RTS} = \frac{1}{\tau} = \frac{1}{\overline{\tau_l}} + \frac{1}{\overline{\tau_h}} = \frac{\overline{\tau_l} + \overline{\tau_h}}{\overline{\tau_h} \cdot \overline{\tau_l}}$ is the corner frequency, below this frequency spectrum of the RTS noise is flat

$\overline{\tau_l}$ is the average time of pulses at low level

$\overline{\tau_h}$ is the average time of pulses at high level

$$\overline{\tau_l} = \frac{1}{P}\sum_{i=1}^{P} \tau_{l,p}$$

$$\overline{\tau_h} = \frac{1}{S}\sum_{j=1}^{S} \tau_{h,s}$$

The intensity of the RTS noise depends on the location of the trap center with the reference to the Fermi level. Only centers in the vicinity of Fermi levels are generating the RTS noise. These trapping centers, which are a source for RTS noise, are usually the result of silicon contamination with heavy metals or lattice structure imperfections.

In the SPICE program the burst noise is often approximated by

$$\overline{i_n^2} = K_B \frac{I_D^{A_B}}{1 + \left(\frac{f}{f_{RTS}}\right)^2} \Delta f \tag{3.86}$$

where K_B, A_B, and f_{RTS} are experimentally chosen parameters, which usually vary from one device to another. Furthermore, a few different sources of the burst noise can exist in a single transistor. In such a case, each noise source should be modeled by separate Equation 3.85 with different parameters (usually different corner frequency f_{RTS})

Kleinpenning [10] showed that RTS noise exists with devices with small number of carriers, where a single electron can be captured by a single trapping center. RTS noise is present in submicrometer MOS transistors and in bipolar transistors with defected crystal lattice. It is present in modern SiGe transistors.

This noise has significant effect at low frequencies. It is function of temperature, collector current, induced mechanical stress, and also radiation. In audio amplifiers the burst noise sounds as random shoots, which are similar to the sound associated with making popcorn. Obviously, bipolar transistors with large burst noise must not be used in audio amplifiers and in other analog circuitry. The burst noise was often observed in epiplanar bipolar transistors with large β coefficients. It is now assumed that devices fabricated with well developed and established technologies do not generate the RTS noise. This is unfortunately not true for modern nanotransistors and devices fabricated with other than silicon materials.

3.2.7 Avalanche Noise

The avalanche noise is another noise component, which can be found in bipolar transistors. For large reverse voltages on the collector junction, the collector current can be multiplied by the avalanche

phenomenon. Carriers in the collector–base junctions gain energies in high electrical field, then lose this energy during collision with the crystal lattice. If the energy gained between collisions is large enough, then during collision another pair of carriers (electron and hole) can be generated. This way the collector current can be multiplied. This is a random process and obviously the noise source is associated with the avalanche carrier generation. The magnitude of the avalanche noise is usually much larger than any other noise component. Fortunately, the avalanche noise exists only in the *pn* junction biased with a voltage close to the breakdown voltage. The avalanche phenomenon is often used to build the noise sources [5].

Spectral density of the avalanche noise is frequency independent

$$S_I(f) = \frac{2qI}{(2\pi f \cdot \tau)^2} \tag{3.87}$$

where I is an average value of the reverse biasing current.

3.2.8 Noise Characterization

Many different methods are used in literature for noise characterization. Sometimes the noise is characterized by an equivalent noise resistance, sometimes by an equivalent noise temperature, sometimes by an equivalent RMS noise voltage or current or sometimes by a noise figure.

3.2.8.1 Equivalent Noise Voltage and Current

The equivalent noise voltage or current is the most commonly used method for modeling the noise in semiconductor devices. The equivalent diagram of the bipolar transistor, including various noise components, is shown in Figure 3.65. The noise components are given by

$$\overline{i_B^2} = \frac{4kT\Delta f}{r_B}, \quad \overline{i_E^2} = \frac{4kT\Delta f}{r_E}, \quad \text{and} \quad \overline{i_C^2} = \frac{4kT\Delta f}{r_C} \tag{3.88}$$

$$\overline{i_C^2} = 2qI_C\Delta f \tag{3.89}$$

$$\overline{i_B^2} = 2qI_B\Delta f + K_F\frac{I_B^{A_F}}{f}\Delta f + K_B\frac{I_B^{A_B}}{1+(f/f_B)^2}\Delta f \tag{3.90}$$

Thermal noise is associated with physical resistors only, such as base, emitter, and collector series resistances. The small-signal equivalent resistances, such as r_π and r_o, do not exhibit thermal noise.

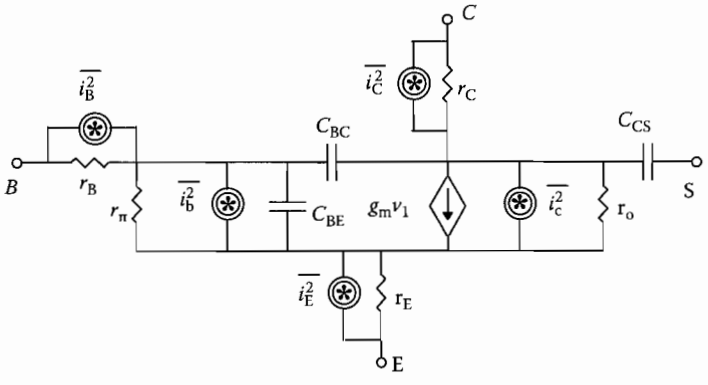

FIGURE 3.65 Equivalent diagram of the bipolar transistor which includes noise sources.

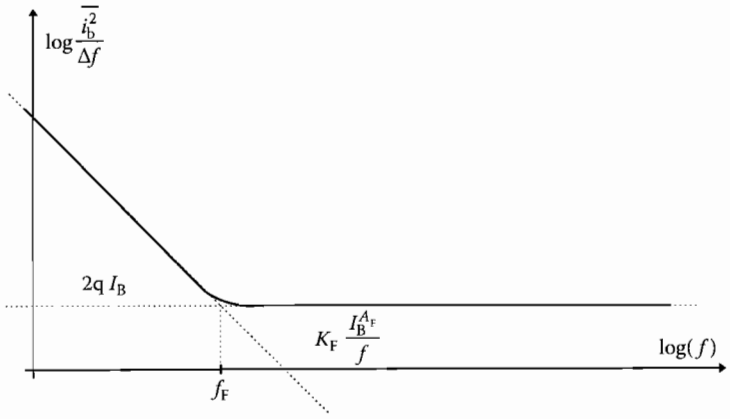

FIGURE 3.66 Bipolar transistor noise as a function of frequency.

The shot noise is associated with both collector and base currents. It was found experimentally that the $1/f$ noise and the burst noise are associated with the base current. The typical noise characteristic of a bipolar transistor is shown in Figure 3.66. The corner frequency of the $1/f$ noise can vary form 10 Hz to 1 MHz.

3.2.8.2 Equivalent Noise Resistance and Noise Temperature

The noise property of a two-port element can be described by a noise current source connected in parallel to the output terminals as Figure 3.67a shows. Knowing that noise current can be expressed as the shot noise of the DC device current the two-port noise can be expressed by means of an equivalent DC noise current

$$I_{eq} = \frac{\overline{i_n^2}}{2q\Delta f} \tag{3.91}$$

Another way to model the two-port noise in the two-port is to use the thermal noise at the input. This can be done using an additional "noisy" resistor connected to the input as Figure 3.67b shows

$$R_n = \frac{\overline{v_{n1}^2}}{4kT\Delta f} = \frac{\overline{v_{n2}^2}}{A_v^2 4kT\Delta f} \tag{3.92}$$

where

A_V is the voltage gain of the two-port

v_{n1}^2 and v_{n2}^2 are equivalent noise voltage sources at the input and the output, respectively

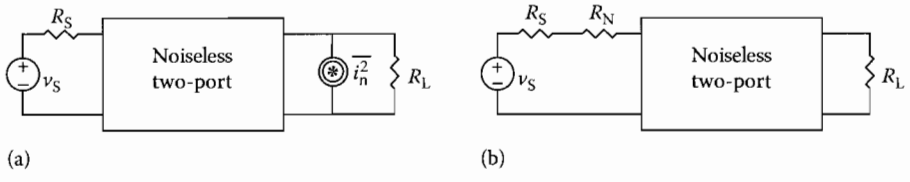

FIGURE 3.67 Noise characterization for two-ports, (a) using the noise source at the output, (b) using noise resistance R_n at the input.

The equivalent noise resistance is not a very convenient way to represent the noise property of the two-port. This additional resistance R_n must not be on the circuit diagram for small-signal analysis. To overcome this difficulty the concept of the equivalent noise temperature was introduced. This is a temperature increment of the source resistance required to obtain the same noise magnitude at the output if this source resistance is the only noise source. The noise temperature can be calculated from the simple formula

$$T_n = \frac{R_n}{R_s} 290^\circ \text{K} \tag{3.93}$$

where R_n and R_s are shown in Figure 3.67b. It is customary to use 290° K as the reference room temperature for the noise temperature calculations.

3.2.8.3 Noise Figure

The noise figure is the ratio of the output noise of the actual two-port to the output noise of the ideal noiseless two-port when the resistance of the signal source R_s is the only noise source.

$$F = 10 \log\left(\frac{\text{total output noise}}{\text{output noise due to the source resistance}}\right) \tag{3.94}$$

The noise figure F is related to the noise resistance and the noise temperature in the following way

$$F = 10 \log\left(1 + \frac{R_n}{R_s}\right) = 10 \log\left(1 + \frac{T_n}{290^\circ \text{K}}\right) \tag{3.95}$$

The noise figure F is the most common method of noise characterization.

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