A Tunable CMOS Resistor with Wide Tuning Range for Low Pass Filter Application

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Abstract- **In this paper, a new tunable CMOS resistor is proposed. The resistance is inversely proportional to bias current, to provide the resistor with a wider tuning range. And transistors, composing the active resistor, work at saturation region to achieve very large resistance within a small area. As an example, a low pass RC filter using tunable CMOS resistor realized in 0.5-µm CMOS technology is reported. The measured result shows that the cutoff frequency of low pass filter can be widely tuned from 5 kHz to 1.9 MHz. The total harmonic distortion (THD) stays lower than -40 dB for an input signal up to 100mV Vp-p at 500-kHz input frequency. The die area of the low-pass filter is 0.25×0.13 mm^2 and the maximum power consumption (at fc=1.9 MHZ) is 5.7mW with single 3.3-V power supply.**

I. INTRODUCTION

Despite the effort to build all circuits in digital, analog filters are still highly needed in many applications owing to its low power consumption and simplicity. Tunable filtering is one of the open problems where tunable components, just like tunable resistors and capacitors, are very hard to be integrated. Recently, tunable filter design with tunable active devices is attracted more and more attention due to its lower power cost, smaller size and needless to say, higher level of integration. [1][2]

Two widely used tuning technologies for analog filters with tunable active components are the MOSFET-C filters and the transconductance-C filters (Gm-C filters). The primary drawback in each is subtle: For MOSFET resistor, the transistor works at triode region, it is very hard to get large resistance. [3][4] For Gm-C filter, due to the reason that Gm is proportional to square root of bias current, it has a limited tuning range.[5] Typically, the tuning range is lower than tens times. This drawback makes it unsuitable for applications where wide tuning range is needed.

In this paper, we present an improved tunable CMOS resistor with large resistance. And also the resistance is inversely proportional to bias current instead of square root of the bias current. Thus, the tuning range of cutoff frequency is much wider than Gm cell in Gm-C filter. Analog filters utilize the tunable resistor we presented can overcome drawbacks stated above simultaneously. As an example, a second-order low pass RC filter using tunable CMOS resistor is proposed. The cutoff frequency can be widely tuned in the range of 5 kHz to 1.9MHz. The THD for a 500-kHz input signal is lower than -40dB up to 100mVpp input signal amplitude.

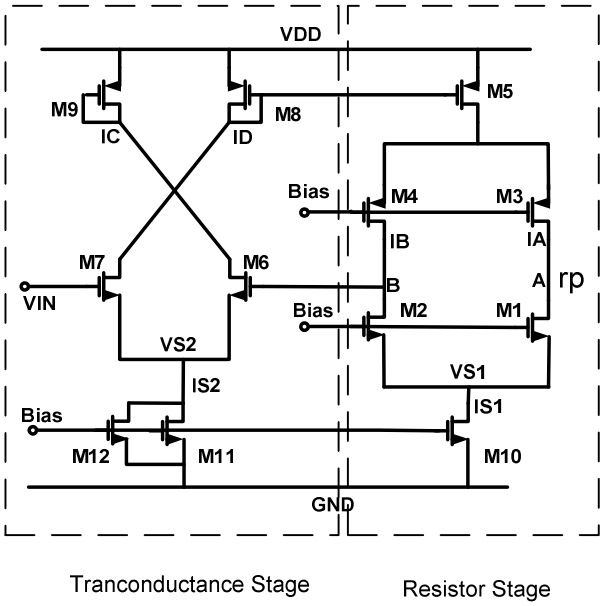

Fig. 1 Schematic of tunable resistor

II. OPERATION THEORY OF TUNABLE FILTER

A. Tunable CMOS resistor

Fig. 1 shows the conceptual schematic of tunable CMOS resistor. Tunable CMOS resistor can be seen as two parts: transconductance amplifier stage and resistor stage.

Differential pair M6 and M7 together with current mirror M9, M8, M5, and M10~12 constitute a transcondutance amplifier. This transconductance amplifier is loaded with internal cascade transistors. The gain can be described as follow:

$$A_V = \frac{r_{o4}\left(1+r_{o5}\times g_{m4}\right) \| \, r_{o4}\left(1+r_{o5}\times g_{m4}\right)}{\dfrac{1}{g_{m7}}+\dfrac{1}{g_{m6}}} \qquad (1)$$

where $r_{o4,5}$ are the output resistances of transistors M4 and M5. $g_{m4,6,7}$ are the equivalent transconductances of transistor M4, M6 and M7. As shown, the voltage gain of this amplifier is very large. By connecting one input of the amplifier (gate of transistor M6) with its output (drain of transistor M4), it acts like a voltage follower. In this way, the voltage on B follows input voltage. Then the desired tunable resistance from VIN to output A is equal to resistance between point A and B. The equivalent resistor model between point A and B is shown in Fig.2.

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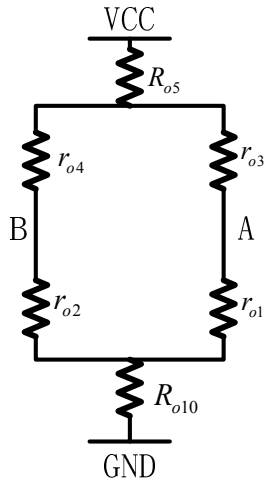


Fig. 2 Equivalent resistor model of resistor stage

To provide large resistance, transistor M1, M2, M3 and M4 work at saturation region in our design. As shown in Fig.2. Equivalent ground resistances R_{o10} and R_{o5} are very large compared to $r_{o1,2,3,4}$ and they can be neglected in the resistance calculation. Then the resistance between point A and B can be expressed as:

$$R_{AB} = \left(r_{o3} + r_{o4}\right) \| \left(r_{o1} + r_{o2}\right) = \frac{1}{I_{eff}\left(\lambda_n + \lambda_p\right)} \quad (2)$$

Where $r_{o1,2,3,4}$ is the output resistance of transistors M1, M2, M3 and M4. λ_n and λ_p are channel length modulation parameters . And I_{eff} can be expressed as:

$$I_{eff} = \frac{I_A \times I_B}{I_A + I_B}. \quad (3)$$

Due to symmetric design for the resistor stage, I_A and I_B are identical. Then the tunable CMOS resistor is achieved, the resistance equals to:

$$R = \frac{1}{I_{S1}\left(\frac{\lambda_n + \lambda_p}{2}\right)} \quad (4)$$

As shown in equation (4), the resistance is inversely proportional to bias current I_{S1}. It can be easily adjusted via changing transistor's bias current I_{S1} and I_{S2}. Sweeps of tunable resistor are shown in Fig.3. In Fig.3, V_T (x-axes) is the voltage adding on the tunable resistor and Iout (y-axis) is the current flow out from the tunable resistor. The bias current IS1 is shown on the top of Fig.3. The simulation result validates that the tunable resistance is inversely proportional to bias current. Fig 4 shows the resistance variation as bias current changing. Both resistance and bias current IS1 are in logarithm scale. As Fig.4 shown, the resistance can be tuned from 90K ohm to 40M ohm by

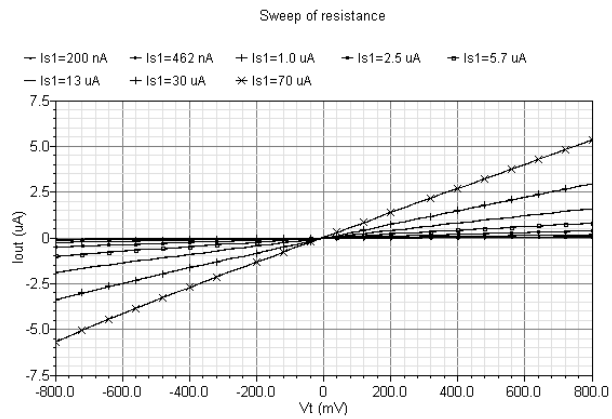


Fig. 3 Simulation result of sweeps of resistance

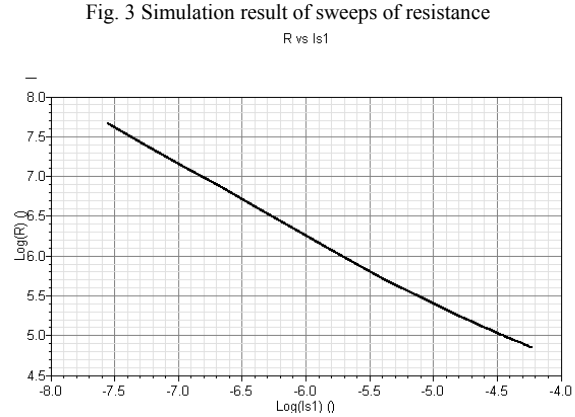
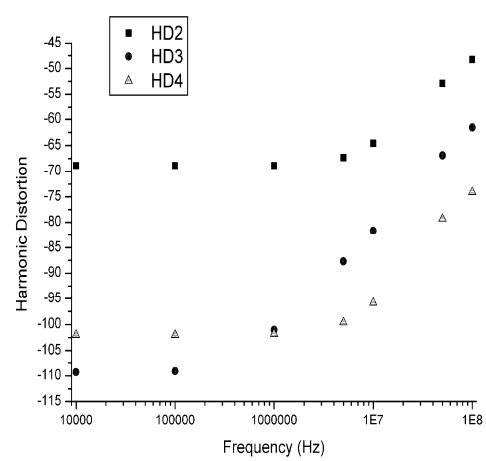


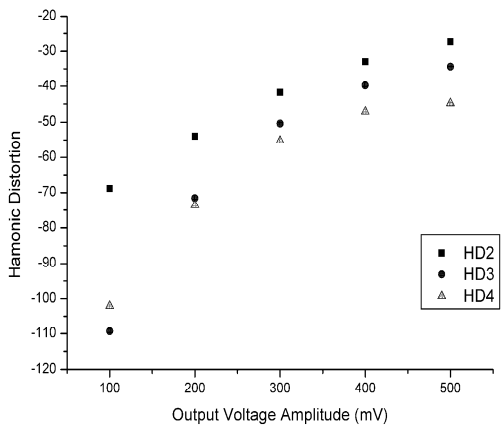
Fig. 4 Resistance variation as current changing (resistance and current are both in logarithm scale)

directly changing the bias current. Compared to traditional Gm cell, in which the tuning range is determined by square root of bias current, and MOSFET working in triode region to act as a resistor, the CMOS resistor in our design has much wider resistance tuning range and larger resistance.

Fig.5 shows the linearity performance of tunable resistor. Fig.5 (a) illustrates the harmonic distortion of tunable resistor under different frequency when output signal amplitude is held at 100mV. As shown, the second harmonic distortion determines the THD, which is below -48dB when frequency is lower than 50MHz. Fig.5 (b)



(a)



(b)

Fig.5. Experimental linearity results of tunable resistor for different frequency and different output power. (a) Harmonic distortion for different input signal frequency. (b) Harmonic distortion for different output signal amplitude

shows the harmonic distortion of tunable resistor as signal amplitude swept. The frequency of input signal is kept at 500 kHz. Both (a) and (b) show that second order harmonic distortion is the dominated nonlinearity factor. Thus, reduction of distortion can be obtained by using the tunable resistor in balanced structures.

B. Low Pass Filter

As mentioned above, the input impedance of the CMOS resistor is much larger than output impedance. Thus, they can be cascaded directly. A simple way to implement a second-order low-pass RC filter with proposed tunable resistor is shown in Fig.6. As shown, tunable resistors and capacitors are simply connected to compose a low-pass filter.

Since tunable resistor's pole frequency is far away from filter's pole frequency, its influence on low frequency pole can be neglected. Simple RC low-pass filter has a second order pole located at:

$$p = -\omega_c = -\frac{1}{RC} = -\frac{I_{S1}\left(\frac{\lambda_n + \lambda_p}{2}\right) I_{S1}}{C} \qquad (5)$$

As shown above, the cut-off frequency can be directly tuning via changing bias current.

III. Implementation of Tunable Filter In VLSI Technology

As an example, a second-order tunable low pass filter using the CMOS resistor as discussed above is implemented and measured. The circuit has been fabricated in 0.5-μm CMOS technology. The conceptual schematic of low pass filter is shown in Fig.6. The total filter block occupies 0.25mm×0.13mm^2 as shown in Fig.7. The tunable resistor block is as same as shown in Fig.1. Two tunable resistors in the filter are identical; differences will occur due to manufacturing tolerances. In case separate externally tuning is necessary.

To reduce influence of parasitic parameters and temperature, metal isolation metal (MIM) capacitor was chosen to implement capacitors Ce1 and Ce2.

IV. Measured Result

The filter was packaged in 2mm×2mm QFN package. Fig.8 shows the measured amplitude response of filter when input signal level is 300mV $V_{p\text{-}p}$. As shown, the cutoff frequency can be widely tuned from 5 kHz to 1.9 MHz as current control voltage changing from 0.75V to 0.95V. The cutoff frequency is a little bit lower than simulation result due to the influence from parasitic capacitor of package and PCB board.

The linearity performance of the low pass filter is shown in Fig.9. The input signal frequency is set at 500 kHz when cutoff frequency is at 1.5MHz. The THD of the tunablefilter is -40dB when input amplitude is 100mV $V_{p\text{-}p}$ and -34dB when input amplitude is 200mV $V_{p\text{-}p}$.

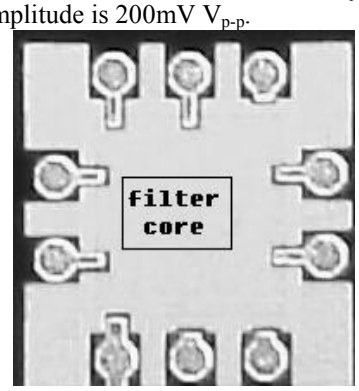


Fig. 7 Die photo of tunable low pass filter

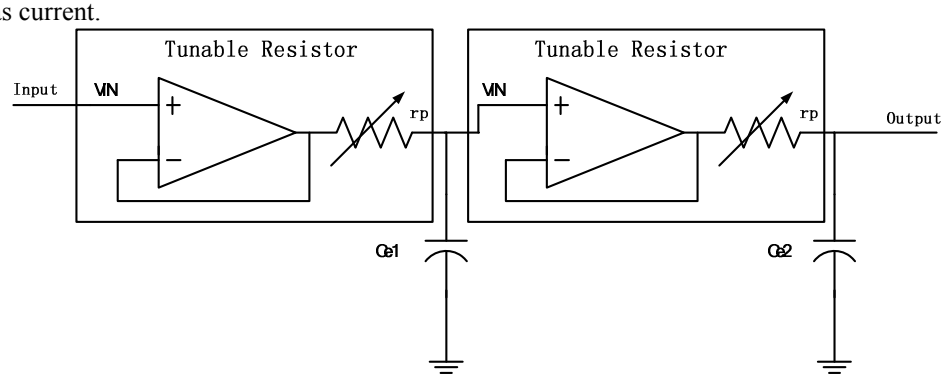


Fig.6 Simplify schematic of second-order low pass filter based on tunable resistor

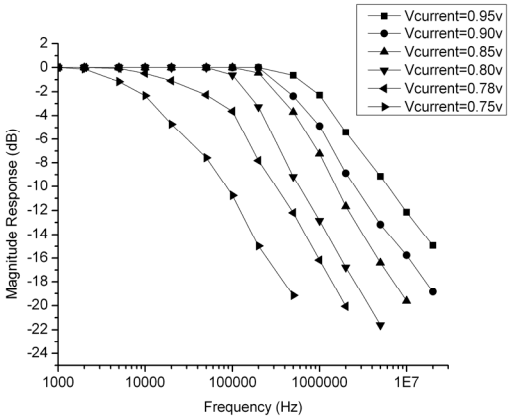
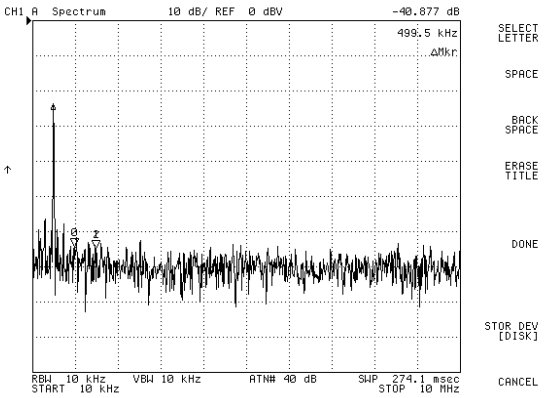
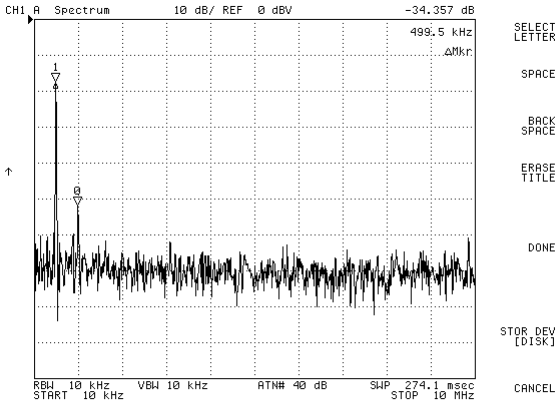


Fig.8. Measured amplitude response of tunable low pass



(a)



(b)

Fig.9. Measured output spectrum of the second-order low pass filter at: (a) input signal level of 100mV Vp-p (b) input signal level of 200mV Vp-p

A summary of the measured performance of the proposed filter is shown in Table I.

Table I. Summary of Measured Performance of the Proposed Filter

	This work	Ref [2]
Technology	0.5-µm CMOS	0.18-µm CMOS
Power Supply	3.3 V	1.8V
Cutoff frequency range	5k - 1.9M Hz	0.5M - 12MHz
Frequency tuning range Freq_max/Freq_min	380	24
Power Consumption (maximum cutoff frequency)	5.7mW	4.7mW
Power Consumption (minimum cutoff frequency)	2.8mW	1.1mW
f_{-3dB} variation for Vcc 3.1V-3.8V	±3.4%	--
Core Size	0.0325 mm^2	0.125 mm^2

V. Conclusion

In this paper, a new CMOS tunable resistor has been designed and analyzed. Its main characteristics are: wide resistance tuning range, large resistance, low power consumption, and small die size. The resistance can be tuned by directly changing bias current. The performance of the proposed tunable resistor has been demonstrated by realizing a second-order low-pass RC filter in 0.5-µm CMOS technology. The measured result shows that the cutoff frequency can be tuned from 5 kHz to 1.9 MHz. The THD is -40dB at an input signal level of 100mV V_{p-p}. Although no automatically tuning was addressed in this paper, it is emphasized that automatic tuning schemes for the CMOS resistor we discussed are unavoidable.

Acknowledgments

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