

Design and Optimization of PWL Circuits Used in Fuzzy Logic Hardware

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Abstract—This work is concerned with the design automation of analog circuits realizing piecewise linear functions (PWL) that may be used for fuzzy logic circuit design. There are several sources of systematic or random errors in the design of such functions. Various combinations of CMOS current mirror circuits are used to implement PWL functions. In order to simplify the optimization of implementation, PWL circuits are divided into smaller circuits which are assumed to be current mirrors in this work. This work presents a computer aided tool for calculation of optimized W and L values of current mirror transistors for various values of reference current within a specified error to find the best transistor parameters for possible minimum power dissipation. Results are tested on several applications to verify that the outputs of the computer aided system presented in this work match simulation results.

I. INTRODUCTION

Over the last few years, analog implementation of neural networks and fuzzy logic with CMOS technology has enjoyed a lot of interest. This is partly due to the expected area and power advantages of analog circuits over their digital counterparts for such soft computing applications. However, the design of analog circuits is more complex than digital circuits because analog design requires creativity and expertise.

This work presents a computer aided design tool for designing a surface approximation circuit with the help of piecewise linear functions (PWL) that are used for fuzzy logic surface approximation. Usage of piecewise circuits is a known method but diode-resistor networks are difficult to be implemented in CMOS integrated circuits. Some methods are proposed for the solution of this problem. One of them is the use of current mirrors to obtain diode like curves where slopes are defined by the W/L ratios. In this work, the optimization of low power, current mode CMOS circuits for synthesis of arbitrary nonlinear functions [1], is performed. Various combinations of CMOS current mirror circuits are used to realize PWL functions. There are several sources of errors in design of such functions. In order to simplify the

optimization of these error calculations, PWL circuits are divided into smaller circuits which are assumed to be current mirrors. Implementation error which is caused by deviation from the real solution surface and mismatch errors between current mirror transistors due to difference between threshold voltages (V_{TO}), oxide capacitance (C_{OX}), width and length of transistor values are considered as the main sources of errors in this paper. In this work each of these errors is calculated independently of the other errors and in the end all of the calculated errors are combined. This final error is regarded as the total error and the W and L values are calculated according to this total value.

This work will make the overall design easier for the developer to pass by some stages faster with better assumptions, when several constraints are taken into consideration. Results of the system defined here are tested on several applications to verify that the results of the design tool presented in this work match with the simulation results. EKV analytical models are used in both calculations and simulations. This approach has been observed as a viable alternative to manual design of PWL circuits.

II. DESIGN METHODOLOGY

In this work, power dissipation and area are the cost functions as long as the circuit remains within certain error bounds. Power optimization and area can be adjusted by varying C_{OX} , V_T , W/L , and input current of the system. Other parameters are considered to be fixed. Here, the aim is to discover the error caused by these differences mentioned, which are going to be called design errors, and adjusting this error to a defined value while minimizing the power dissipation. Proper W and L values will be defined for the possible best optimized design for the output of this process. Surface approximation error will be considered as the implementation error. In approximation to solution surface some breakpoints are selected according to certain constraints defined by the user. This constraint controls the amount of breakpoints to be selected and implementation error. For example, defining more breakpoints will increase the accuracy of the

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approximation while increasing the transistor count which means an increase in power dissipation. This trade off must be defined and determined by the designer. In this work MATLAB libraries and compiler is used for software development and modeling. Input and output of this process are defined as text files so that these files can be used as a source for different development environments. In this work, EKV model for MOS transistors was chosen to define mathematical solutions of the circuits. This model is a compact analytical model for MOS transistors [3].

The system developed consists of a linear approximation algorithm to discover the breakpoints, a W/L calculation algorithm to find the optimum device sizes, and a circuit creation algorithm that uses the outputs of these two blocks to design the required circuit. These blocks will be discussed in the following sections.

III. SURFACE APPROXIMATION

The approximation algorithm is designed for approximating the real solution surface with a minimum number of possible points. These points are regarded as the breakpoints and written to a file where they are going to be read to create a spice file. The algorithm is based on studying the variance of the output with respect to a pre specified threshold value. The second derivative is also used as a criterion. The output of this algorithm is the breakpoints and the total approximation error. Obviously, there is always going to be an error in approaching the desired function which can be decreased by increasing the number of breakpoints. This step is actually nothing but a simple PWL fit to an arbitrary nonlinear function.

IV. TRANSISTOR PARAMETER CALCULATION

The EKV MOSFET model is based on the $V_p - V_{ch}$ which is defined to be the inversion charge Q . V_p is the pinch-off voltage and V_{ch} is the channel voltage.

Since the EKV model is continuous in all regions of the transistor, it allows the designer to use the same I_D equation in all regions. I_D in the EKV MOSFET model is expressed as the difference between the forward current I_F and the reverse current I_R . EKV MOSFET model is derived from the charge-sheet formulation [3].

$$I_D = 2 \cdot N \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_i)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{V_G - V_T}{2U_i}} \right) - \ln^2 \left(1 + e^{\frac{V_G - V_T}{2U_i} - V_D} \right) \right] \quad (1)$$

where

$$V_p = \frac{V_G - V_{T0}}{N} \quad (2)$$

For a simple NMOS current mirror circuit, (1) can be evaluated for the reference transistor and the mirror transistor individually. The difference of the two currents yields the error due to variation in the drain potentials if both transistors are assumed to be equal. Another error source is the mismatch between the transistors. This can be defined as

having three components, one of them being the difference between C_{ox} values of each transistor, the second one being the difference between the V_T values, and the third one being the W and L value variations. It should be noted that these errors tend to work in opposite directions; that is, the V_T error effect is reduced with higher overdrive voltages (meaning narrower transistors or larger currents), whereas the W and L variations require larger transistors. Hence, an optimum design choice exists for a given error.

In calculation of transistor parameters, when short channel effects are taken into consideration, the simple models break down. Furthermore, minimum sized transistors cannot be used when matching is desired. Hence, $1\mu m$ was selected as the minimum size for both W and L values instead of the technology minimum. Therefore, in the rest of this work $1\mu m$ will be taken as the minimum size and calculations will be done for to this specification.

A sample input file for transistor parameter calculation contains information for the type of the MOSFET (n or p), the supply voltage, source potential of the transistors, the expected difference between C_{ox} values of current mirror transistors, the expected difference between V_{T0} values of current mirror transistors, step sizes and initial points for various design parameters, transistor parameters, and allowed total error. Based on these, the design tool will try to calculate the optimum transistor sizing. Please note that especially V_T mismatches are extremely sensitive to bias point and optimization for minimum power and minimum error is a must for best performance.

V. CIRCUIT CREATION

This algorithm is used for the creation of the spice output file in order to establish a circuit whose output will be the approximated surface. Therefore, the created circuit will be a power optimized circuit which supplies the defined solution surface. In this work, a fuzzy solution surface is used as an input to the algorithm but any kind of surface may be approached.

Circuit creation is done in one and two dimensional modes. The two dimensional mode is included as an illustration of the generality of the presented system. Thus, the extension of the work to multidimensional inputs with dimension higher than two is feasible. In any design, the worst path, which is the longest path from input node to output node, is calculated. The remaining error (which is obtained by subtracting the approximation error from the total allowable error as described above) is divided by the current mirror count on the worst case path and the remaining error range for each current mirror is obtained.

VI. APPLICATION EXAMPLES

A combination of circuits developed earlier [1] is used to approximate a surface. A sample curve to be approximated is shown in Figure 1. Breakpoint values are converted to actual current values by multiplying them with 10^{-5} .

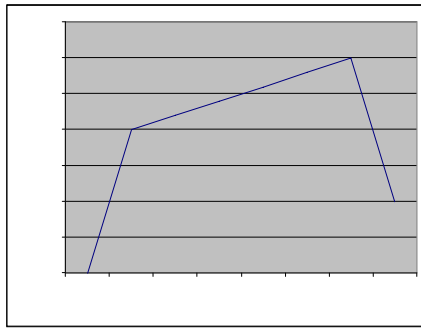


Figure 1. Expected solution surface

Circuit schematic of the automatically created and sized spice file is shown in Figure 2.

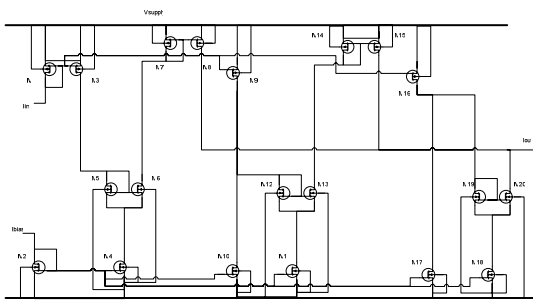


Figure 2. Circuit schematic of the sample circuit

The success of the approximation algorithm can be observed by inspecting Table 1.

Table 1. Breakpoints comparison of approximated and expected surface

Breakpoints	X ₁	Z ₁	X ₂	Z ₂	X ₃	Z ₃	X ₄	Z ₄	X ₅	Z ₅
Expected (10 ⁵ A)	0.00	0.00	1.00	2.00	6.00	3.00	7.00	1.00	7.00	1.00
Approximated (10 ⁵ A)	0.00	0.00	1.09	2.11	6.12	2.98	7.49	1.34	8.13	1.10

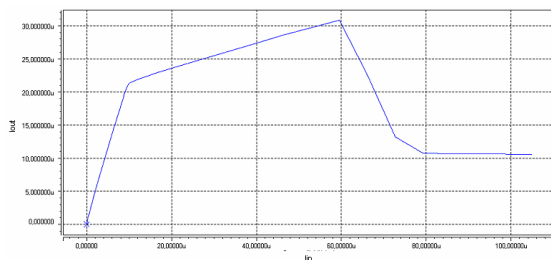


Figure 3. H-Spice simulation of the created circuit

Figure 3 shows the HSPICE simulation of the automatically designed circuit. This figure should be compared with Figure 1 which is the desired solution.

The purpose of the second example is to test the two dimensional approximation capabilities of the approach. Assuming the breakpoints given in Figure 4, where the first variable “xy” refers to the second input; “xx” refers to the

first input, and “xz” is the output, a circuit satisfying the desired criteria is automatically generated.

```
xy 1 xx 2 xz 0
xy 1 xx 3 xz 4
xy 1 xx 5 xz 3
xy 8 xx 4 xz 7
xy 8 xx 11 xz 9
```

Figure 4. Breakpoints of the two dimensional sample circuit
Two dimensional plots of the simulation outputs of the above design are shown in Figures 5 and 6. As it can easily be seen from these graphs, H-Spice simulations show perfect matching with the expected surface.

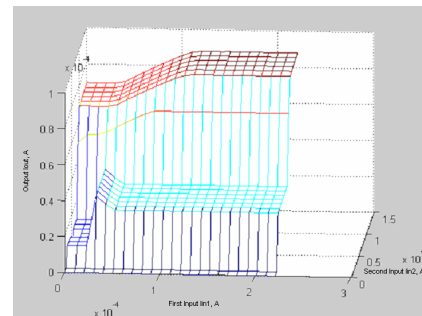


Figure 5. Sample two dimensional circuit two dimensional output graph-1

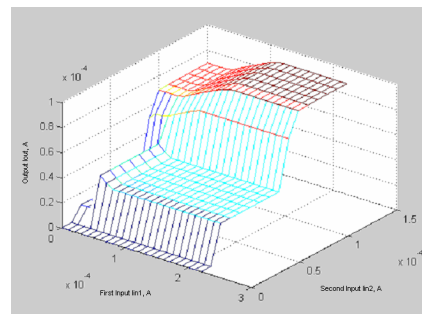


Figure 6. Sample two dimensional circuit two dimensional output graph-2

The third example presented is from the fuzzy logic demo represented in MATLAB R2006a library. This design will be constructed on the “Modeling Inverse Kinematics in a Robotic Arm” application. Kinematics is the science of motion. In a two-joint robotic arm, given the angles of the joints, the kinematics equations give the location of the tip of the arm. Inverse kinematics refers to the reverse process. Given a desired location for the tip of the robotic arm, what should the angles of the joints be so as to locate the tip of the arm at the desired location.

Since the scope of this work is not “Inverse Kinematics”, it is not going to be explained in this work. For more information on this topic, MATLAB demo file will be a good start point.

The surface that is going to be approximated in Modeling Inverse Kinematics in a Robotic Arm is shown in Figure 7.

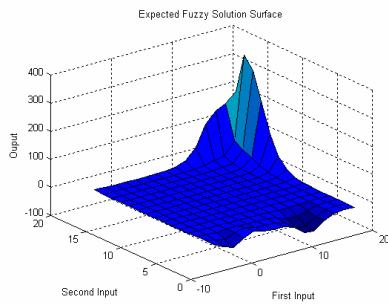


Figure 7. Fuzzy Solution Surface

The process of two dimensional surface approximation is the same as the process defined in the one dimensional mode. The only difference is that the second input is not fixed in this case. Solution surface defined in Figure 7 is the expected surface. Reconstructed surface created by the calculated breakpoints is normalized and the final output surface is shown in Figure 8.

The breakpoints are calculated and the remaining error for W and L calculations are the inputs of the Circuit Creation algorithm. In creation of two dimensional circuits, a kind of superposition is applied in that the output is created from two one dimensional designs. The output solution surface is shown in Figure 9. The actual generated circuit consists of more than 800 transistors. This circuit is optimum in terms of power and area as well as remaining within a predefined error bound. The creation time of the circuit is on the order of a few seconds.

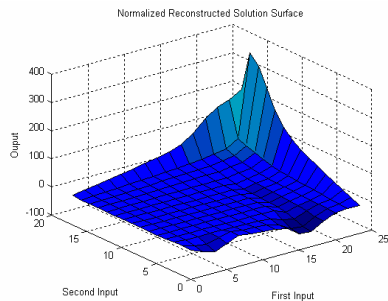


Figure 8. Normalized reconstructed two dimensional fuzzy solution surface

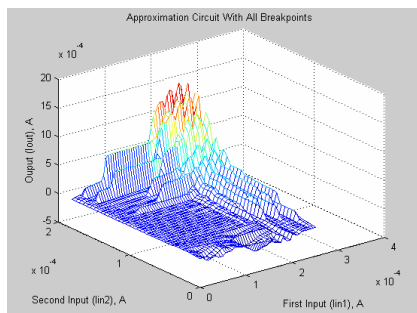


Figure 9. Fuzzy solution created by the Circuit Creation algorithm

VII. CONCLUSIONS

A design automation tool for the creation of one and two dimensional PWL response surfaces was described in this work. Performance specifications, constraints coming from the designer, and transistor model parameters are inputs of this tool. The success of the tool was demonstrated on three examples; namely, a one dimensional approximation problem, a two-dimensional approximation problem, and a fuzzy logic system. In all cases, the tool was able to generate circuits whose simulations fulfilled all the specifications.

Future work may progress in several directions. One direction will be the usage of this method in other blocks rather than current mirrors. Second direction is to take into consideration the gain bandwidth performance criteria in design of PWL circuits. Another possible direction is the integration of the tool defined in this work to other design tools to introduce a complete solution for fuzzy logic circuits. This work introduces a solution for two dimensional surfaces to show that n-dimensional solutions are possible. Extending this solution for n-dimensional surfaces may be another future research direction.

VIII. ACKNOWLEDGMENTS

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IX. REFERENCES

- [1] Wilamowski, B. M., E. S. Ferre-Pikal and O.Kaynak, "Low Power, Current Mode CMOS Circuits for Synthesis Of Arbitrary Nonlinear Functions", *9th NASA Symposium on VLSI Design*, 2000.
- [2] Ahmadi, S., L. Sellami and R. W. Newcomb, "A CMOS PWL Fuzzy Membership Function", *IEEE International Symposium on Circuits and Systems*, Seattle WA, Vol. 3, pp. 2321-2324, April 30-May 3 1995.
- [3] Christian C. E., F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid In All Regions of Operation and Dedicated To Low Voltage and Low Current Applications", *Analog Integrated Circuits And Signal Processing*, 8, 83-114, 1995.
- [4] Sasaki, M., T. Inoue, Y. Shirai and F. Ueno, "Fuzzy Multiple-Input Maximum and Minimum Circuits in Current Mode and Their Analyses Using Bounded- Difference Equations", *IEEE Transactions on Computers*, Vol. 39, No. 6, June 1990.
- [5] Wilamowski, B. M., R. C. Jager and O.Kaynak, "Neuro-Fuzzy Architecture for CMOS Implementation", *IEEE Transactions on Industrial Electronics*, Vol. 46, No. 6, December 1999.
- [6] Wilamowski, B. M., J. Binfet and O.Kaynak, "VLSI Implementation of Neural Networks", *Int. Journal of Neural Systems*, Vol. 10, No. 3, pp. 191-198, 2000.
- [7] Yamakawa, T., "A Fuzzy Interface Engine in Nonlinear Analog Mode and Its Applications to a Fuzzy Logic Control", *IEEE Transactions on Neural Networks*, Vol. 4, No. 3, May 1993.
- [8] Ota, Y. and B. M. Wilamowski, "Current-Mode CMOS Implementation of a Fuzzy Min-Max Network", *IEEE Transaction on Industrial Electronics*, Vol. 46, No. 6, pp. 1132-1136, Dec 1999.
- [9] Ahmadi, S., L. Sellami and R. W. Newcomb, "A CMOS WL Fuzzy Membership Function", *International Symposium on Circuits and Systems*, pp. 2321-2324, 1995.
- [10] Dharia, N., J. Gownipalli, B. M. Wilamowski and O. Kaynak, "Multi Dimensional Second Order Defuzzification Algorithm (M-SODA)", *The 28th Annual Conference Of The IEEE Industrial Electronics Society: IECON '02*, Nov. 5-8, 2002, Sevilla, Spain, pp.3215-3220, 2002.