Threshold Voltage Control for Deep Sub-micrometer Fully Depleted SOI MOSFET

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Abstract—In this paper, the threshold voltage of fully depleted silicon on insulator device with geometry scale down below 100nm is investigated deeply. All the device simulations are performed using SILVACO Atlas device simulator. Several ways to control the threshold voltage are proposed and simulated. Threshold voltage changing with the silicon film thickness, channel doping concentration, gate oxide thickness and gate electrode work function is simulated. One short channel NMOS and one PMOS FDSOI device structure with effective channel length 90nm and 30nm silicon film thickness are designed.

I. INTRODUCTION

In recent years, silicon-on insulator (SOI) has attracted considerable attention as a potential alternative substrate for low power application. [1] The most common approach for reducing the power is power supply scaling. Since power supply reduction below three times threshold voltage ($3V_t$) will degrade circuit speed significantly, scaling of the power supply should be accompanied by threshold voltage reduction. [2,3] However, the lower limit of the threshold voltage is set by the amount of off-state leakage current that can be tolerated, ideally should be no less than 0.4V. [2] The fully depleted silicon-on-insulator (FDSOI) has the advantages of lower parasitic junction capacitance and better sub-threshold swing, reduced short channel effects, and free of kink effect [4], [5], [9]. Especially with the geometry scaling down to deep sub-micron range, the threshold voltage also scales down, therefore, threshold voltage control is becoming more important for the future technology. In this paper, the devices with effective channel length 90nm, silicon film thickness changing from 10nm to 60nm, channel doping changing from $5E16\text{cm}^{-3}$ to $1E18\text{cm}^{-3}$ are simulated using SILVACO atlas device simulator. The threshold voltage changing with the silicon film thickness, channel doping concentration, gate oxide thickness, and gate work function are simulated in this paper.

II. PRINCIPLE OF FDSOI THRESHOLD VOLTAGE CONTROL

The analysis provided here is for NMOS, with its extension to PMOS device being straightforward. The threshold voltage of an n-channel MOSFET is classically given [5] by:

$$V_{th} = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\Phi_F + \frac{qN_a x_{d\max}}{C_{ox}} \quad (1)$$

where Φ_{MS} is the work function difference between the gate and the channel and equal to $\Phi_m - (\Phi_{Si} - \Phi_F)$. Q_{ss} is the surface state charge of the channel. C_{ox} is the gate capacitance and equals to $\frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$. t_{ox} is the gate oxide thickness. Φ_F is the Fermi potential, equal to $\frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$, where N_D is the channel doping concentration. $x_{d\max}$ is the maximum depletion width, for partially depleted device equal to $\sqrt{\frac{4\epsilon_{Si}\Phi_F}{qN_a}}$.

Equation (1) works well for NMOS device.

For the fully depleted silicon on insulator devices, the silicon film is very thin compared to the partially depleted devices. Under the thin silicon film, there is a very thick buried oxide. Similar to the gate oxide, there are some surface charges between the silicon film and the buried oxide. This surface charge varies with the technology. When the silicon film scale down below 100nm, this charges have effects to the threshold voltage. In this paper we model this effect as a capacitor. For the fully depleted devices $x_{d\max}$ is equal to the silicon film thickness t_{Si} . Then the threshold voltage for the fully depleted silicon on insulator devices change to:

$$V_{th} = \Phi_{MS} - \frac{Q_{ss}t_{ox}}{\epsilon_{ox}\epsilon_0} + 2\Phi_F + \frac{qN_a t_{Si}t_{ox}}{\epsilon_{ox}\epsilon_0} - Q_{ssb} \left(\frac{t_{ox}}{\epsilon_{ox}\epsilon_0} + \frac{t_{Si}}{\epsilon_{Si}\epsilon_0} \right) \quad (2)$$

where the Q_{ssb} is the surface charge between the silicon film and the buried oxide, t_{Si} is the silicon film thickness.

From the threshold voltage equation, it is observed that there are several factors to control the threshold voltage. The first one is the channel doping. The channel doping effects the Fermi potential Φ_F directly, with the channel doping increasing, the Fermi potential increases. Also with the channel doping concentration increasing, the depletion charge in the channel also increases. With the channel doping increasing, more effort is needed to invert the channel. Therefore, with adjusting the channel doping, different threshold voltages can be achieved. In normal technology, the ion implantation can increase or decrease the channel doping. This is a very effective way to adjust the threshold voltage in CMOS technology.

The second factor is the gate oxide thickness. The gate oxide thickness is a reverse proportion to the gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means that the gate has less control to the channel and threshold voltage will increase.

The third factor is the gate work function. The gate work function has direct control to the threshold voltage. This is a very attractive alternative approach to the threshold voltage control. Several metals have been considered as candidates for gate electrode (such as Ta and W). Another metal/polysilicon stacked gate structure was proposed. The gate electrode is comprised a thin (a few nm) layer of polysilicon and metal. By changing the thickness of the polysilicon layer, one can vary the effective work function of the gate from that of the metal to that of the polysilicon. [6] For the very thin body fully depleted SOI CMOS transistors, the required range of the work function for symmetric gate is 4.4–5.0V. [7]

When the geometry goes down to deep sub-micron level, the short channel effect will roll-off the threshold voltage. When the voltage between the drain and source increases, the high potential of the drain will lower the potential barrier, which called DIBL (Drain Induced barrier lowering). These DIBL phenomena also lead to threshold voltage reduction. Threshold voltage reduction with decreasing channel length and the increasing drain source voltage is a 2-D effect in short channel devices. [8]

III. THRESHOLD VOLTAGE SIMULATION AND OBSERVATION

Several NMOS SOI device structures with effective channel length (90nm) are simulated using SILVACO atlas device simulator.

Fig. 1 Threshold voltages changing with the silicon film thickness at different channel doping concentration level for NMOS SOI with effective channel length 90nm and gate oxide thickness is 2nm.

Fig. 2 Threshold voltages changing with the channel doping concentration at different silicon film thickness for NMOS SOI with effective channel length 90nm and gate oxide thickness is 2nm.

Fig.1 and Fig.2 show the NMOS SOI threshold voltage changing with silicon film thickness and the channel doping concentration. The silicon film thickness changes from 10nm to 60nm. The channel doping changes from $5E16\text{cm}^{-3}$ to $1E18\text{cm}^{-3}$. The gate work function (4.7V) is used in this simulation. Gate oxide thickness is 2nm.

From Fig.2 it is observed that with the channel doping increasing, the threshold voltage increases. This is quite reasonable. With the channel doping increasing, the Fermi potential increases; also channel depletion charge increasing, it takes more effort to deplete the whole channel. That's the cause that the threshold voltage goes up with the channel doping increasing. In Fig.1 and Fig.2 it is also can be seen that when the channel doping concentration goes up higher to $1E18\text{cm}^{-3}$, the threshold voltage does not grow up accordingly with the silicon film thickness (greater than 50nm). The reason is with this highly doped channel, when the silicon film goes up to 50nm, the device goes from fully depleted to nearly fully depleted and finally goes to partially depleted. When the device goes to partially depleted. The depletion charge of the channel is fixed and does not increase with silicon film thickness increasing. Then the threshold voltage goes to a fixed value. From Fig.1 and Fig.2, it also can be seen the threshold changes with the silicon film thickness. When the channel doping concentration is below $2E17\text{cm}^{-3}$, the threshold voltage goes down with the increasing of the silicon film thick. However, when the channel doping above the $2E17\text{cm}^{-3}$, the threshold goes up with the silicon film thickness.

Fig.3 shows the gate oxide thickness controlling the threshold voltage. From the simulation results, it can be drawn that with the gate oxide thickness increasing from 2nm to 4nm, the threshold voltage also increases. This means that with the gate oxide thickness increasing the gate capacitance decreases, and the gate has less control to the channel. In order to invert the channel, the threshold voltage will increase to compensate it.

Fig. 3 Threshold voltage changing with gate oxide thickness for NMOS SOI with effective channel length 90nm and channel doping is $3E17cm^{-3}$.

Fig. 4 Threshold voltages changing with different gate work function for NMOS and PMOS SOI with effective channel length 90nm, channel doping ($3E17cm^{-3}$), silicon film thickness 30nm and gate oxide thickness (2nm).

From the above simulation, changing the channel doping and gate oxide thickness, the threshold voltage can be controlled. But with the geometry goes down below 100nm, it is very difficult to control the channel doping. For example, when the device channel length is 100nm, silicon film thickness 50nm, channel width 1 μm , with this small geometry, the total volume is $5E-15cm^3$. In order to get the doping concentration $2E17cm^{-3}$, the total doping dose is 1000 atoms, which is a very small number. It is difficult to get the accurate channel doping concentration in the real technology. Random fluctuation of the doping concentration can lead to variations of the threshold voltage. An attractive alternative way to adjust the threshold voltage is the gate electrode work function engineering. [6] With the gate work function changing, the flat band voltage is changed and the threshold voltage is also changed. Fig. 4 shows the threshold voltage

changes at different gate work function. From Fig.4 it is observed that the gate electrode work function has the linear control to the threshold voltage.

IV. DEVICE SIMULATION RESULT

One very short channel NMOS FD-SOI device and one PMOS are fully simulated using SILVACO Atlas device simulator in this research. The effective channel length is 90nm, the silicon film thickness is 30 nm, the gate oxide thickness is 2 nm and the channel doping concentration is $3E17cm^{-3}$ for the NMOS and $2.5E17cm^{-3}$ for the PMOS. The gate work function 4.7V is used in this simulation. The device structure is shown in Fig.5.

Fig. 5 Device structure of the NMOS SOI with effective channel length 90nm, channel doping is $3E17cm^{-3}$, drain and source doping concentration is $1E20cm^{-3}$, gate oxide thickness is 2nm Silicon film thickness 30nm

Fig. 6 ID-VG characteristics NMOS and PMOS FDSOI in log scale. Both NMOS and PMOS with effective channel length 90nm, channel doping for NMOS is $3E17cm^{-3}$, $2.5E17cm^{-3}$ for PMOS.

Fig.6 shows ID-VG characteristics in log scale for NMOS and PMOS FDSOI. Fig. 7 shows square root of the drain current changing with the gate voltage at different drain voltage. The threshold voltage of this device is 0.41V, power supply voltage is 1.2V, and the off state leakage current for the NMOS is 1.5nA/um, which meets the requirement for the leakage current less than 3nA/um for the NMOS. The PMOS leakage current is 11.5nA/um. The sub-threshold slope is 95mV/dec and 100mV/dec for the PMOS.

From Fig. 7 it is observed that with the drain source voltage increasing, the threshold voltage is decreasing. This is the DIBL phenomenon. DIBL is very common for the very short channel devices. With the channel length scales down to 90nm or lower, the drain potential has very strong effect to the channel. This high drain to source voltage will roll off the threshold voltage. This is a 2-D effect.

Fig.7 square root drain current with gate voltage characteristics for the NMOS SOI device at different drain source bias

Fig.8 ID-VD characteristics NMOS FDSOI at different gate voltage

Fig. 8 shows the ID-VD characteristics for the designed NMOS and PMOS FDSOI. The drive current for the NMOS is 681uA/um and this meets the requirement for the drive current greater than 600uA/um for the NMOS. For the PMOS the drive current is 268uA/um.

V. DISCUSSION AND CONCLUSION

In this paper, all the device parameters are fully simulated using SILVACO Atlas device simulator. The threshold voltage of fully depleted silicon on insulator device with geometry scale down below 100nm is investigated deeply. Several ways to control the threshold voltage are proposed and simulated. All the devices are simulated using the classical method. When the device geometry goes down to nanometer, several quantum effects will happen, an increase of threshold voltage with reduced film thickness is expected [5]. But still the classical method can give valuable instructions on the very small geometry device design.

VI. ACKNOWLEDGEMENT

The authors gratefully acknowledge Idaho NASA ESPCoR for its support.

REFERENCES

- [1] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," 1994 IEEE International Electron Devices Meeting, San Francisco, CA, December 1994, pp. 809-812.
- [2] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI" IEEE transactions on electron device, Vol. 44, No. 3, pp414-422, Mar 1997
- [3] D. Liu and C. Svensson, "Trading speed for low-power by choice of supply and threshold voltage", IEEE J. Solid-State Circuit, Vol. 28, pp10-17, Jan 1993
- [4] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era", IEEE Electron Device Letters, vol. 21, no. 5, p. 254, 2000
- [5] Jean-Pierre Colinge, "Silicon-On-Insulator Technology: Materials to VLSI" 2nd edition, Kluwer, 1997
- [6] I. Polishchuk, C. Hu, "Polycrystalline Silicon/metal stacked gate for threshold voltage control in metal-oxide-semiconductor field effect transistors", Applied Physics Letters, Vol. 76, No. 14, pp1938-1940, Apr 2000
- [7] L. Chang et al., "Gate length scaling and threshold voltage control of double gate MOSFETs", IEDM Technical Digest, pp719-722, Dec 2000.
- [8] S.R. Banna, P.C.H. Chan, P.K. Ko, C.T. Nguyen, Mansun Chan, "Threshold voltage model for deep-submicrometer fully depleted SOI MOSFETs", IEEE Trans. Electron Devices, Vol. 42, No 11, pp1949-1955, Nov 1995.
- [9] P. Sivaram, B.Anand, and Madhav P. Desai, "Silicon Film Thickness Considerations in SOI-DTMOS", IEEE Electron Device Letters, Vol23, No. 5, pp276-278, May 2002.